JEPPIAAR ENGINEERING COLLEGE

Department of Electronics & Communication Engg

QUESTION BANK

EC-3552 – VLSI AND CHIP DESIGN

III Year V Semester ECE

NAME :_____

ROLLNO. :_____

REGNO. :_____

YEAR :_____

SECTION :_____

JEPPIAAR ENGINEERING COLLEGE		
Vision of the Institute	To build Jeppiaar Engineering College as an institution of academic excellence in technological and management education to become a world class University	
Mission of the Institute	**M1**	To excel in teaching and learning, research and innovation by promoting the principles of scientific analysis and creative thinking
	M2	To participate in the production, development and dissemination of knowledge and interact with national and international communities.
	M3	To equip students with values, ethics and life skills needed to enrich their lives and enable them to meaningfully contribute to the progress of society
	M4	To prepare students for higher studies and lifelong learning, enrich them with the practical and entrepreneurial skills necessary to excel as future professionals and contribute to Nation's economy
DEPARTMENT: ELECTRONICS AND COMMUNICATION ENGINEERING		
Vision of the Department	To become a centre of excellence to provide quality education and produce creative engineers in the field of Electronics and Communication Engineering to excel at international level.	
Mission of the Department	**M1**	Inculcate creative thinking and zeal for research to excel in teaching-learning process
	M2	Create and disseminate technical knowledge in collaboration with industries
	M3	Provide ethical and value based education by promoting activities for the betterment of the society
	M4	Encourage higher studies, employability skills, entrepreneurship and research to produce efficient

		professionals thereby adding value to the nation's economy
PROGRAM OUTCOMES (PO)	**PO 1**	**Engineering knowledge**: **Apply** the knowledge of mathematics, science, engineering fundamentals, and an engineering specialization to the solution of complex engineering problems.
	PO 2	**Problem analysis**: **Identify, formulate, review** research literature, and **analyze** complex engineering problems reaching substantiated conclusions using first principles of mathematics, natural sciences, and engineering sciences.
	PO 3	**Design/development of solutions**: **Design solutions** for complex engineering problems and **design** system components or processes that meet the specified needs with appropriate consideration for the public health and safety, and the cultural, societal, and environmental considerations
	PO 4	**Conduct investigations of complex problems**: **Use** research-based knowledge and research methods including **design** of experiments, **analysis** and **interpretation** of data, and **synthesis** of the information to provide valid conclusions.
	PO 5	**Modern tool usage**: **Create**, **select**, and **apply** appropriate techniques, resources, and modern engineering and IT tools including prediction and modeling to complex engineering activities with an understanding of the limitations.
	PO 6	**The engineer and society**: **Apply** reasoning informed by the contextual knowledge to assess societal, health, safety, legal and cultural issues and the consequent responsibilities relevant to the professional engineering practice.
	PO 7	**Environment and sustainability**: **Understand** the impact of the professional engineering solutions in societal and environmental contexts, and **demonstrate** the knowledge of, and need for sustainable development.
	PO 8	**Ethics**: **Apply** ethical principles and commit to professional ethics and responsibilities and norms of the engineering practice.
	PO 9	**Individual and team work**: **Function effectively** as an individual, and as a member or leader in diverse teams, and in multidisciplinary settings.
	PO 10	**Communication**: **Communicate effectively** on complex engineering activities with the engineering community and

		with society at large, such as, being able **to comprehend** and **write** effective reports and **design** documentation, **make** effective presentations, and **give** and **receive** clear instructions.
	PO 11	**Project management and finance**: **Demonstrate** knowledge and understanding of the engineering and management principles and **apply** these to one's own work, as a member and leader in a team, to **manage** projects and in multidisciplinary environments.
	PO 12	**Life-long learning**: **Recognize** the need for, and have the preparation and ability to **engage** in independent and life-long learning in the broadest context of technological change.
PROGRAM EDUCATIONAL OBJECTIVES (PEOS)	**PEO I**	Produce technically competent graduates with a solid foundation in the field of Electronics and Communication Engineering with the ability to analyze, design, develop, and implement electronic systems.
	PEO II	Motivate the students for choosing the successful career choices in both public and private sectors by imparting professional development activities.
	PEO III	Inculcate the ethical values, effective communication skills and develop the ability to integrate engineering skills to broader social needs to the students.
	PEO IV	Impart professional competence, desire for lifelong learning and leadership skills in the field of Electronics and Communication Engineering.
PROGRAM SPECIFIC OUTCOMES (PSOs)	**PSO 1**	Design, develop and analyze electronic systems through application of relevant electronics, mathematics and engineering principles.
	PSO 2	Design, develop and analyze communication systems through application of fundamentals from communication principles, signal processing, and RF System Design & Electromagnetics.
	PSO 3	Adapt to emerging electronics and communication technologies and develop innovative solutions for existing and newer problems.

COURSE OUTCOME:VLSI AND CHIP DESIGN

C302.1	In depth knowledge of MOS technology
C302.2	Understand Combinational Logic Circuits and Design Principles
C302.3	Understand Sequential Logic Circuits and Clocking Strategies
C302.4	Understand Memory architecture and building blocks
C302.5	Understand the ASIC Design Process and Testing.

PO: VLSI AND CHIP DESIGN

EC3552	PROGRAM OUTCOME											
	1	2	3	4	5	6	7	8	9	10	11	12
C302.1	1	1	-	-	-	-	-	-	-	-	-	-
C302.2	3	2	3	2	-	-	-	-	-	-	-	1
C302.3	2	3	2	3	1	1	-	-	-	-	-	2
C302.4	-	-	1	1	-	-	-	-	-	-	-	3
C302.5	-	-	-	-	-	2	-	-	-	-	1	-
Average Course Outcomes= **(max 3.00)**	2	2	2	2	1	1.5	-	-	-	-	1	2

PSO: VLSI AND CHIP DESIGN

EC3552	**PROGRAM SPECIFIC OUTCOME**		
	PSO1	**PSO2**	**PSO3**
C302.1	3	3	3
C302.2	3	3	3
C302.3	3	2	3
C302.4	3	3	2
C302.5	3	2	2
AVG=	3	3	3

EC3552 VLSI AND CHIP DESIGN L T P C

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OBJECTIVES:

- Understand the fundamentals of IC technology components and their characteristics.
- Understand combinational logic circuits and design principles.
- Understand sequential logic circuits and clocking strategies.
- Understand ASIC Design functioning and design.
- Understand Memory Architecture and building blocks

UNIT I MOS TRANSISTOR PRINCIPLES 9

MOS logic families (NMOS and CMOS), Ideal and Non Ideal IV Characteristics, CMOS devices. MOS(FET) Transistor Characteristic under Static and Dynamic Conditions, Technology Scaling, power consumption

UNIT II COMBINATIONAL LOGIC CIRCUITS 9

Propagation Delays, stick diagram, Layout diagrams, Examples of combinational logic design, Elmore's constant, Static Logic Gates,Dynamic Logic Gates, Pass Transistor Logic, Power Dissipation, Low Power Design principles.

UNIT III SEQUENTIAL LOGIC CIRCUITS AND CLOCKING STRATEGIES 9

Static Latches and Registers, Dynamic Latches and Registers, Pipelines, Nonbistable Sequential Circuits.Timing classification of Digital Systems, Synchronous Design, Self-Timed Circuit Design

UNIT IV INTERCONNECT , MEMORY ARCHITECTURE AND ARITHMETIC CIRCUITS 9

Interconnect Parameters – Capacitance, Resistance, and Inductance, Electrical WireModels, Sequential digital circuits: adders, multipliers, comparators, shift registers. Logic Implementation using Programmable Devices (ROM, PLA, FPGA), Memory Architecture and Building Blocks,Memory Core and Memory Peripherals Circuitry

UNIT V ASIC DESIGN AND TESTING 9

Introduction to wafer to chip fabrication process flow. Microchip design process & issues in test and verification of complex chips, embedded cores and SOCs, Fault models, Test coding. ASIC Design Flow, Introduction to ASICs, Introduction to test benches, Writing test benches in Verilog HDL, Automatic test pattern generation, Design for testability, Scan design: Test interface and boundary scan

COURSE OUTCOMES:

Upon successful completion of the course the student will be able to

CO1: In depth knowledge of MOS technology

CO2: Understand Combinational Logic Circuits and Design Principles

CO3: Understand Sequential Logic Circuits and Clocking Strategies

CO4: Understand Memory architecture and building blocks

CO5: Understand the ASIC Design Process and Testing.

TEXTBOOKS:

1. Jan D Rabaey, Anantha Chandrakasan, " Digital Integrated Circuits: A Design Perspective",PHI, 2016.(Units II, III and IV).

2. Neil H E Weste, Kamran Eshranghian, “ Principles of CMOS VLSI Design: A System Perspective,” Addison Wesley, 2009.(Units - I, IV).

3. Michael J Smith ,” Application Specific Integrated Circuits, Addison Wesley, (Unit - V)

4. Samir Palnitkar,” Verilog HDL:A guide to Digital Design and Synthesis”, Second Edition, Pearson Education,2003.(Unit - V)

5. Parag K.Lala,” Digital Circuit Testing and Testability”, Academic Press, 1997, (Unit - V)

REFERENCES

1. D.A. Hodges and H.G. Jackson, Analysis and Design of Digital Integrated Circuits, International Student Edition, McGraw Hill 1983

2. P. Rashinkar, Paterson and L. Singh, "System-on-a-Chip Verification-Methodology and Techniques", Kluwer Academic Publishers,2001

3. SamihaMourad and YervantZorian, “Principles of Testing Electronic Systems”, Wiley 2000

4. M. Bushnell and V. D. Agarwal, "Essentials of Electronic Testing for Digital, Memory and Mixed-Signal VLSI Circuits", Kluwer Academic Publishers,2000

UNIT I MOS TRANSISTOR PRINCIPLES

PART-A

1. What is CMOS technology?

Complementary Metal Oxide Semiconductor (CMOS) in which both n-channel MOS and p-channel MOS are fabricated in the same IC.

2. What are the advantages of CMOS over NMOS technology?

- In CMOS technology the aluminum gates of the transistors are replaced by poly silicon gate.
- The main advantage of CMOS over NMOS is low power consumption.

  In CMOS technology the device sizes can be easily scalable than NMOS.

3. What is mean by Body effect and body bias effect? (AU NOV/DEC– 16)

Body effect refers to the change in the transistor threshold voltage (VT) resulting from a voltage difference between the transistor source and body. Because the voltage difference between the source and body affects the VT, the body can be thought of as a second gate that helps determine how the transistor turns on and off.

Body bias involves connecting the transistor bodies to a bias network in the circuit layout rather than to power or ground. The body bias can be supplied from an external (off-chip) source or an internal (on-chip) source.

4. what is mean by NMOS transistor? (AU NOV/DEC– 17)

NMOS transistors operate by creating an inversion layer in a p-type transistor body. This inversion layer, called the n-channel, can conduct electrons between n-type "source" and "drain" terminals. The n-channel is created by applying voltage to the third terminal, called the gate. Like other MOSFETs, NMOS transistors have four modes of operation: cut-off (or sub threshold), triode, saturation (sometimes called active), and velocity saturation.

5.what is mean by process parameter?

Process parameter is the current status of a process under control. An example of this would be the temperature of a furnace. The current temperature is called the process variable, while the desired temperature is known as the set -point. Measurement of process variables are important in controlling a process. The process variable is a dynamic feature of the process which may change rapidly. Accurate measurement of process variables is important for the

maintenance of accuracy in a process. Process parameters such as oxide thickness and doping concentrations TOX, XJ, GAMMA1, NCH, NSUB

6.write the Electrical properties of CMOS circuits and device modeling?

- Resistance & Capacitance Estimation
- DC Responseo
- Logic Level and Noise Margins
- Transient Response
- Delay Estimationo Transistor Sizing
- Power Analysiso Scaling Theory

7. What are the advantages of CMOS technology?

- Low power consumption
- High performance
- Scalable threshold voltage
- High noise margin
- Low output drive current

8. What are the disadvantages of CMOS technology?

- Low resistance to process deviations and temperature changes.
- Low switching speed at large values of capacitive loads.

9. What is Design rule? (AU Nov – 2008)

Design rules are the communication link between the designer specifying requirements and the fabricator who materializes them. The design rule conform to a set of geometric constraints or rules specify the minimum allowable line widths for physical objects on-chip such as metal and poly silicon interconnects or diffusion area, minimum feature dimensions and minimum allowable separations between two layers.

10. What is stick diagram?

Stick diagram are the key element of designing a circuit used to convey layer

information through the use of a colour code.

11. What is micron design rule?

Micron rules specify the layout constraints such as minimum feature sizes and minimum allowable feature separations are stated in terms of absolute dimensions in micrometers.

12. What is Lambda design rule?

Lambda rules specify the layout constraints such as minimum feature sizes and Minimum allowable feature separation is stated in terms of a single parameter and thus Allow linear, proportional scaling of all geometrical constraints. is generally half of the Minimum drawn transistor channel length.

13. What is DRC?

Design rule check program looks for design rule violations in the layout. It checks for minimum spacing and minimum size and ensures that combinations of layers from legal components.

14. Mention MOS transistor characteristics?

Metal Oxide Semiconductor is a three terminal device having source, drain and gate. The resistance path between the drain and source is, controlled by applying a voltage to the gate.

The Normal conduction characteristics of an MOS transistor can be categorized as

i. Cut-off region

ii. Non saturated region

iii. Saturated region

15. Compare enhancement and depletion mode devices. (AU Nov – 07)

Enhancement Mode:

- No conducting channel between source and drain unless a positive voltage is applied
- Enhancement-mode device is equivalent to a normally open (off) switch

Depletion Mode:

- Channel exists even with zero voltage from gate to source. In order to control the channel a negative voltage is applied to the gate.
- Depletion-mode device is equivalent to a normally closed (on) switch

16. What is threshold voltage?

It is defined as the minimum voltage at which the device starts conduction (ie) turns on.

17. What is noise margin? (AU APRIL/MAY – 08)

The allowable noise voltage on the input of a gate so that that output will not be corrupted.

NML = VIL - VOL

NMH = VOH - VIH

where,

VIL – maximum HIGH input voltage

VOL - maximum LOW output voltage

VOH - minimum HIGH output voltage

18.Compare nMOS and pMOS. (AU Nov – 07)

NMOS	**PMOS**
The majority carriers are Electrons	The majority carriers are holes
Positive voltage is applied at the gate terminal	Negative voltage is applied at the gate terminal
nMOS conducts at logic 1	pMOS conducts at logic 0
Mobility of electron is high	Mobility of hole is low
Switching speed is high	Switching speed is low

19. What is Impact Ionization?

When the length of the gate is reduced, the electric field at the drain of a transistor in saturation increases. For submicron gate lengths, the field can become so high that electron is imparted with enough energy to become "hot". The hot electrons impact the drain, dislodging holes that are swept towards the negatively charged substrate and appear as a substrate current. This effect is known as impact ionization.

20. What is Moore's Law?

Moore's Law states that the number of transistor would double every 18 months.

21. What are the steps involved in IC fabrication?

(i) Wafer preparation.

(ii) Oxidation

(iii) Diffusion

(iv) Ion implantation

(v) Chemical Vapor deposition

(vi) Metallization

(vii) Photo lithography

(viii) Packaging

22. Mention MOS transistor characteristics?

- Metal Oxide Semiconductor is a three terminal device having source, drain and gate.
- The resistance path between the drain and source is controlled by applying a voltage to the gate.
- The Normal conduction characteristics of an MOS transistor can be categorized as

(i) Cut-off region

(ii) Non saturated region

(iii) Saturated region

23. What is the need of demarcation line? (AU NOV/DEC– 17)

In CMOS a demarcation line is drawn to avoid touching of p-diff with n-diff. All PMOS must lie on one side of the line and all NMOS will have to be on the other side

24. What are the two types of oxidation methods?

(i) Dry oxidation method

(ii) Wet oxidation method

In dry oxidation, the oxygen used in the reaction is introduced as a high-purity gas with silicon to form SiO2.

In wet oxidation, the oxygen used in the reaction is introduced as a steam with silicon to form SiO2

25. What is Diffusion?

Diffusion is the process by which atoms move from a high concentration region to a low concentration region through the semiconductor crystal. In fabrication, diffusion is a method to introduce impurity atoms into silicon to change its resistivity.

26. What is meant by Epitaxy?

Epitaxy is the process of depositing a thin layers (.05 to 20 microns) of single crystal material over a single crystal substrate usually through chemical vapor deposition.

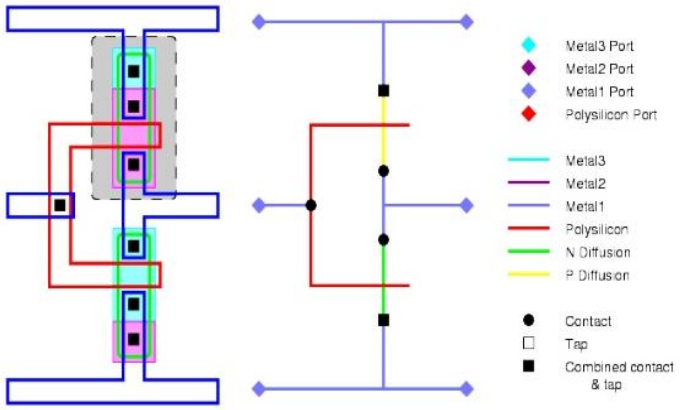
27. What are the materials used for masking?

Polysilicon, SiO2, Si3N4.

28. What is Design rule?

Design rules are the communication link between the designer specifying requirements and the fabricator who materializes them. The design rule conform to a set of geometric constraints or rules specify the minimum allowable line widths for physical objects on-chip such as metal and poly silicon interconnects or diffusion area, minimum feature dimensions and minimum allowable separations between two layers.

29. Draw stick and layout diagram CMOS INVERTER? (AU NOV/DEC– 16)



30. What is micron design rule?

Micron rules specify the layout constraints such as minimum feature sizes and minimum allowable feature separations are stated in terms of absolute dimensions in micrometers.

31. What is Lambda design rule?

Lambda rules specify the layout constraints such as minimum feature sizes and minimum allowable feature separations are stated in terms of a single parameter □□and thus allow linear, Proportional scaling of all geometrical constraints.

32. What is DRC?

Design rule check program looks for design rule violations in the layout. It checks for Minimum spacing and minimum size and ensures that combinations of layers from legal

Components.

33. What is meant channel length modulation in NMOS transistor? (AU APRIL/MAY – 17)

Ids is independent of Vds for a transistor in saturation, making the transistor a perfect current source. The p/n junction between the drain and body forms a depletion region with a width Ld that increases with Vdb . The depletion region effectively shortens the channel length to

$$Leff=L-Ld$$

34. What is circuit extraction?

Circuit extraction is a process to calculate the exact length and position of each interconnects, parasitic capacitance and resistance associated with each interconnect in order to determine the circuit behavior after fabricating the IC.

35. What is simulator?

Simulator is a tool used to predict the behavior of the circuit using set of equations or test vectors.

36. What are the different types of simulators?

(i) Circuit simulator

(ii) Timing simulator

(iii) Switch level simulator

(iv) System level simulator

37. What are the two types of design rules? (Apr/May 2010)

 Micron rules

 Lambda rules

38. What is body effect ?(Apr/May2010),(Nov/Dec 2010)

The resultant effect increases the channel substrate junction potential. This increases the rate-channel voltage drop. The overall effect is an increase in threshold voltage. This effort is called body effect.

39. What is body effect coefficient? (Apr/May 2011)

The potential difference between the source and body affects the threshold voltage. The threshold voltage can be modeled as

$Vt=Vt0+\gamma((\Phi s+Vsb)1/2-(\Phi s)1/2$

Where, Φs= surface potential at threshold

γ= body effect coefficient

40. What is the influence of voltage scaling on power and delay? (AprMay 2011)

Constant voltage scaling increased the electric field in devices. By the 1μm generation velocity saturation was severe enough that decreasing feature size no longer improved device current. Aggressive process achieve delays in the short end of the range by building transistors with effective channel length.

41. Determine whether an NMos transistor with a threshold voltage of 0.7v is operating in the saturation region if Vgs=2V and Vds=3V.(Nov/Dec 2011)

Vt=0.7 Vgs=2V Vd=3V

NMos transistor is in saturation region if

Vds > Vgs-Vt

3V > 2V-0.7V

3V > 1.3V

It is in saturation region

42. Write down the equation for describing the channel length modulation effect in NMos transistor. (MAY/JUN 2016)

o Ideally Ids is independent of Vds in saturation.

o The reverse biased p-n junction between the drain and body forms a depletion region with a width Ld that increases with Vdb.

o The depletion region effectively shortens the channel length to Leff =L-Ld.

o Imagine that the source voltage is close to the body voltage. Increasing Vds decreases the effective channel length. Ids=β(Vgs-Vt)2/2

43. Write the expression for the logical effort and parasitic delay of an input NOR gate. (Nov/Dec 2011)

Logical effort of n input Nor gate

G=(2n+1)/3

N=number of inputs

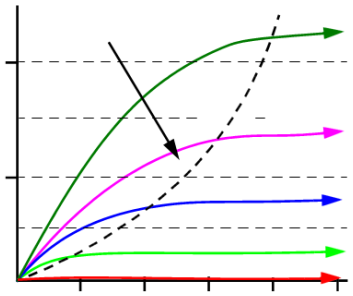
44. Why does interconnect increase the circuit delay? (Nov/Dec 2011)

The wire capacitance adds loading to each gate.

The long wire contributes RC delay or flight time.

Circuit delay can be increased by interconnect

45. Draw the IV characteristics of Mos transistors.(MayJun 2012)



46.. Brief the different operating regions of Mos system.(May/ Jun 2012)

Different operating regions of Mos syatem

- Cut off or suthreshold region
- Linear or non-saturation region
- Saturation region

47. Why the tunneling current is higher for NMos transistor than Pmos transistor with silica gate? (Nov/Dec 2012)

Tunneling current is an order of magnitude higher for nMos than PMos transistor with Sio2 gate dielectrics because the electrons tunnel from the conduction band while the holes tunnel from the valance band.

48. What is the objective of layout rules?

Layout design rule is examined and a scale parameter lambda is n defined as the halfwidth of a minimum width line or as a multiple of standard deviation of a process. Designing layouts in terms of lambda allows for future scaling makes the layout portable.

49. What are the advantages of CMOS technology ?(May 2013)

a. Low power consumption.

b. High performance.

c. Scalable threshold voltage.

d. High noise margin.

e. Low output drive current.

50. What is latch up? How to prevent latch up? (MAY/JUN 2016)

Latch up is a condition in which the parasitic components give rise to the establishment of low resistance conducting paths between VDD and VSS with disastrous results. Careful control during fabrication is necessary to avoid this problem.

PART-B

1.Explain about NMOS ,PMOS transistors steps involved in n-well fabrication process? (AU NOV/DEC– 16)

Refer page no.6-13, A.Pucknell, Kamran Eshraghian , "BASIC VLSI Design", Third Edition, Prentice Hall of India, 2007

2.Define the MOS logic families (NMOS and CMOS)?

Refer page no.14-22, A.Pucknell, Kamran Eshraghian , "BASIC VLSI Design", Third Edition, Prentice Hall of India, 2007

3.Write the Electrical properties of CMOS circuits and device modeling? (AU NOV/DEC– 17,APRIL/MAY – 17) (AU APRIL/MAY – 16)

Refer page no.25-34, A.Pucknell, Kamran Eshraghian , "BASIC VLSI Design", Third Edition, Prentice Hall of India, 2007

4.Basic principles Scaling and fundamental limits? (AU NOV/DEC– 17) (AU APRIL/MAY – 17) (AU APRIL/MAY – 16)

Refer page no.113-133, A.Pucknell, Kamran Eshraghian , "BASIC VLSI Design", Third Edition, Prentice Hall of India, 2007

5.Write the CMOS inverter scaling, propagation delays?

Refer page no.137-143, A.Pucknell, Kamran Eshraghian , "BASIC VLSI Design", Third Edition, Prentice Hall of India, 2007

6.Draw the basic gates Stick diagram, Layout diagrams?(AU NOV/DEC– 17,APRIL/MAY – 17) (AU NOV/DEC– 16)

Refer page no.57-69, A.Pucknell, Kamran Eshraghian , "BASIC VLSI Design", Third Edition, Prentice Hall of India, 2007

7. Explain in detail about Non-ideal I-V characeteristics of p-MoS and n-MoS Transistors (MAY/JUN 2016)

Refer page no.25-34, A.Pucknell, Kamran Eshraghian , "BASIC VLSI Design", Third Edition, Prentice Hall of India, 2007

8. Explain in detail about the ideal I-V characteristics of a nMOS and pMOS device (NOV/DEC 2013)(MAY/JUN 2013)(NOV/DEC 2014)

Refer page no.25-34, A.Pucknell, Kamran Eshraghian , “BASIC VLSI Design”, Third Edition, Prentice Hall of India, 2007

9. Explain in detail about DC characteristics of MoS transistor. (MAY/JUN 2016)

Refer page no.25-34, A.Pucknell, Kamran Eshraghian , “BASIC VLSI Design”, Third Edition, Prentice Hall of India, 2007

10. Explain about device modeling in detail.(MAY/JUN 2012)(MAY/JUN 2013).

Refer page no.435-446, A.Pucknell, Kamran Eshraghian , “BASIC VLSI Design”, Third Edition, Prentice Hall of India, 2007

11. Explain in detail about scaling concept, power consumption. (MAY/JUN 2016)

Refer page no.125-128, A.Pucknell, Kamran Eshraghian , “BASIC VLSI Design”, Third Edition, Prentice Hall of India, 2007

12. Explain the stick diagram and layout diagram with examples. May 11, May13, Nov/Dec10

Refer page no.57-69, A.Pucknell, Kamran Eshraghian , “BASIC VLSI Design”, Third Edition, Prentice Hall of India, 2007

13. Discuss in detail with a MOS(FET) Transistor Characteristic under Static and Dynamic Conditions**.**

Refer page no.72-78, A.Pucknell, Kamran Eshraghian , “BASIC VLSI Design”, Third Edition, Prentice Hall of India, 2007

14. Discuss in detail with necessary equation the operation of MOSFET and its current voltage characteristics.

Refer page no.29-32, A.Pucknell, Kamran Eshraghian , “BASIC VLSI Design”, Third Edition, Prentice Hall of India, 2007

15. Draw and explain the D.C and transfer characteristics of a CMOS inverter with a necessary conditions for the different regions of operation.

Refer page no.25-34, A.Pucknell, Kamran Eshraghian , “BASIC VLSI Design”, Third Edition, Prentice Hall of India, 2007

16. Discuss the principle of constant field scaling and also write its effect on device characteristics.

Refer page no. 125-128, A.Pucknell, Kamran Eshraghian , “BASIC VLSI Design”, Third Edition, Prentice Hall of India, 2007

17. Explain the small signal model of MOS transistors with neat diagram and expression.

Refer page no.52-58, A.Pucknell, Kamran Eshraghian , “BASIC VLSI Design”, Third Edition, Prentice Hall of India, 2007

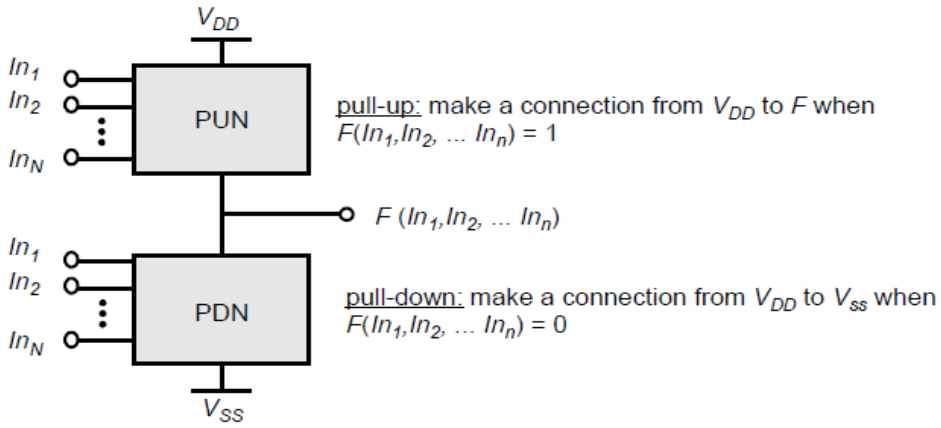
UNIT II COMBINATIONAL LOGIC CIRCUITS

Part-A

1.Define Static CMOS Design?

The most widely used logic style is static complementary CMOS. The static CMOS style is really an extension of the static CMOS inverter to multiple inputs. In review, the primary advantage of the CMOS structure is robustness (i.e, low sensitivity to noise), good performance, and low power consumption with no static power dissipation. Most of those properties are carried over to large fan-in logic gates implemented using a similar circuit topology.

2.Draw Complementary logic gate as a combination of a PUN (pull-up network) and a PDN (pull-down network).



3. Define Propagation Delay of Complementary CMOS Gates? (AU APRIL/MAY – 17)

The computation of propagation delay proceeds in a fashion similar to the static inverter.For the purpose of delay analysis, each transistor is modeled as a resistor in series with an ideal switch. The value of the resistance is dependent on the power supply voltage and an equivalent large signal resistance, scaled by the ratio of device width over length, must be used. The logic is transformed into an equivalent RC network that includes the effect of internal node capacitances

4. Define Transistor Sizing?

The most obvious solution is to increase the overall transistor size. This lowers the resistance of devices in series and lowers the time constant. However, increasing the transistor size, results in larger parasitic capacitors, which do not only affect the propagation delay of the gate in question, but also present a larger load to the preceding gate. This technique should, therefore, be used with caution. If the

load capacitance is dominated by the intrinsic capacitance of the gate, widening the device only creates a “self-loading” effect, and the propagation delay is unaffected.

5. Define Power Consumption in CMOS Logic Gates?

Many of these issues apply directly to complex CMOS gates. The power dissipation is a strong function of transistor sizing (which affects physical capacitance),input and output rise/fall times (which affects the short-circuit power), device thresholds and temperature (which affect leakage power), and switching activity. The dynamic power dissipation is given by a0®1 CL VDD 2 f. Making a gate more complex

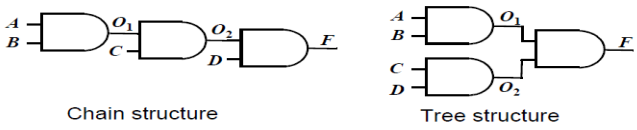
mostly affects the switching activity a0®1, which has two components: a static component that is only a function of the topology of the logic network, and a dynamic one that results from the timing behavior of the circuit—the latter factor is also called glitching.

6. Design Techniques to Reduce Switching Activity?

The dynamic power of a logic gate can be reduced by minimizing the physical capacitance and the switching activity. The physical capacitance can be minimized in a number ways, including circuit style selection, transistor sizing, placement and routing, and architectural optimizations.The switching activity, on the other hand, can be minimized at all level of the design abstraction,and is the focus of this section. Logic structures can be optimized to minimize both the fundamental transitions required to implement a given function, and the spurious transitions

7.Define Logic Restructuring?

Changing the topology of a logic network may reduce its power dissipation. Consider for instance two alternate implementations of F = A · B · C · D,



8. What is ratioed circuits?

Ratioed logic is an attempt to reduce the number of transistors required to implement a given logic function, often at the cost of reduced robustness and extra power dissipation.

9. What is CPL?

The main concept behind complementary pass transistor logic (CPL) is the use of only an nMOS network for the implementation of logic functions. It consists of nMOS pass transistor logic network driven by two sets of complementary inputs and CMOS inverter used as buffers.

10What are the advantages of pseudo-nMOS logic?

1. Reduce the number of transistors to implement a given logic function.

2. Pseudo-nMOS logic uses (N + 1) transistor ver sus 2N for complementary CMOS.

3. Have smaller area and reduced input capacitance.

11. What are the disadvantages of pseudo-nMOS logic.

1. Reduced output voltage swing and gain, which makes the gate more susceptible to noise.

2. As the p-load is always turned on, when the n pull-down is on, current flows in the gate structure.

3. The main problem with pseudo-nMOS logic is the static power dissipation that occurs whenever the pull-down chain is turned on.

12. What is pass transistor.

It is a MOS transistor, in which gate is driven by a control signal, the source (out), the drain of the transistor is called constant or variable voltage potential (in) when the control signal is high, input is passed to the output and when the control signal is low, the output is floating such topology circuits is called pass transistor.

13. List the advantages of pass transistor.

1. Pass-transistor logic (PTL) circuits are often superior to standard CMOS circuits in terms of layout density, circuit delay and power consumption.

2. They do not have a path VDD to GND and do not dissipate standby power (static power dissipation).

14. Define threshold drop.

In pass transistor logic, the source terminal of MOS device can rise to the lower of the two potentials VD (drain voltage) and Vgs -Vtn. If potentials at drain terminal and gate terminal are same (ie VDD) the source output will be (Vgs -Vt) since the source terminal can only rise to threshold voltage below the gate. This is called as threshold drop.

15. What is transmission gate?

The circuit constructed with the parallel connection of pMOS and nMOS with shorted drain and source terminals. The gate terminal uses two select signals s and s, when s is high then the transmission gate passes the signal on the input. The main advantage of transmission gate is that it eliminates the threshold voltage drop.

16.Define Differential Pass Transistor Logic?

High performance design, a differential pass-transistor logic family, called CPL or DPL, is commonly used. The basic idea (similar to DCVSL) is to accept true and complementary inputs and produce true and complementary outputs. A number of CPL gates (AND/NAND, OR/NOR, and XOR/NXOR)

17.Define Dynamic CMOS Design?

static CMOS logic with a fan-in of N requires 2N devices. A variety of approaches were presented to reduce the number of transistors required to implement a given logic function including pseudo-NMOS, pass transistor logic, etc. The pseudo-NMOS logic style requires only N + 1 transistors to implement an N input logic gate, but unfortunately it has static power dissipation. In this section, an alternate logic style called dynamic logic is presented that obtains a similar result, while avoiding static power consumption. With the addition of a clock input, it uses a sequence of precharge and conditional evaluation phases.

18.Define Issues in Dynamic Design?

Dynamic logic clearly can result in high performance solutions compared to static circuits. However, there are several important considerations that must be taken into account if one wants dynamic circuits to function properly. This include charge leakage, charge sharing, back gate (and in general capacitive) coupling, and clock feed through

19.Define Charge Leakage?

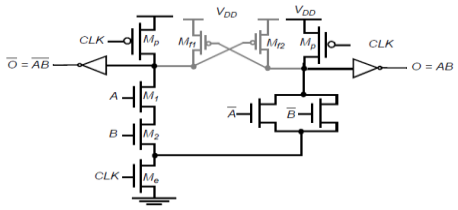
Dynamic gate relies on the dynamic storage of the output value on a capacitor. If the pull-down network is off, the output should ideally remain at the precharged state of VDD during the evaluation phase. However, this charge gradually leaks away due to leakage currents, eventually resulting in a alfunctioning of the gate

20.Define Domino Logic?

A Domino logic module [Krambeck82] consists of an n-type dynamic logic block followed by a static inverter During precharge, the output of the ntype dynamic gate is charged up to VDD, and the output of the inverter is set to 0. During evaluation, the dynamic gate conditionally discharges, and the output of the inverter makes a conditional transition from 0 ® 1. If one assumes that all the inputs of a Domino gate are outputs of other Domino gates3, then it is ensured that all inputs are set to 0 at the end of the precharge phase, and that the only transitions during evaluation are 0 ® 1 transitions. The formulated rule is hence obeyed. The introduction of the static inverter has the additional advantage that the fan-out of the gate is driven by a static inverter with a lowimpedance output, which increases noise immunity. The

buffer furthermore reduces the capacitance of the dynamic output node by separating internal and load capacitances

21.Draw Simple dual rail (differential) Domino logic gate? (AU NOV/DEC– 17)



22. Define Noise margin?

The allowable noise voltage on the input of a gate so that the output will not be affected is called noise margin.

23. What is transmission Gate? (AU NOV/DEC– 17)

The parallel connection of p and n-channel MOSFET is called transmission gate. The transmission gates are used to transmit the logical values without any degradation.

24. Why don't we use just one nMOS or pMOS transistor as a transmission gate?

Normally transmission gates are used to eliminate the undesirable threshold voltage effects which give rise to the loss of logic levels in transistors. In nMOS it passes logic0 and degrades logic1, while in pMOS it passes logic1 and degrades logic0. to avoid these degradation the transmission gates are implemented with both nMOS and pMOS.

25. Write the applications of transmission gate? (AU APRIL/MAY – 17)

□□Multiplexing element or path selector

□□A latch element

□□An analog switch

4.□Act as a voltage controlled resistor connecting the input and output.

26. What is tristate inverter?

Tristate inverter produces restored output - violates conduction complement rule because to get the high impedance state. The inverter has input terminal, output terminal and a controlled enabled line depending upon this select enable line, the output is produced as 1 or 0 or Z.

27. Define pseudo-nMOS logic?

It is ratioed logic, the entire pMOS (pull-up network) is replaced with a single load device that is the gate terminal of pMOS is normally grounded and the nMOS (pull-down network) realizes the logic function such topology are called as pseudo-nMOS

28What is MTCMOS?

Multi-threshold CMOS (MTCMOS) utilized transistors with multiple threshold voltage □□to optimize delay or power. Normally transistors designed with MTCMOS have low and high threshold voltages. Lower voltage devices are used on critical delay paths to minimize clock periods. Higher voltage devices are used on non-critical paths to reduce static leakage power without incurring a delay penalty.

29. What are the two categories of SOI devices?

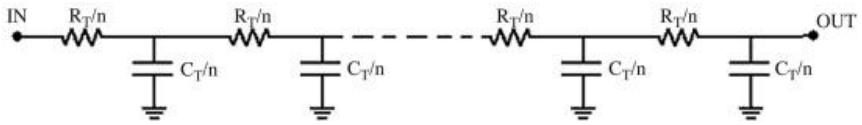
1. Fully depleted (FD) SOI
2. Partially depleted (PD) SOI

30. What is fully depleted SOI?

In an nMOS transistor, applying a positive voltage to the gate depletes the body of p-type carriers and induces an n-type inversion channel on the surface of the body. If the insulated layer of silicon is made very thin, the layer fills the full depth of the body. A technology designed to operate this way is called a fully depleted SOI.

31. Define Elmore Constant? (AU APRIL/MAY – 17) (AU NOV/DEC– 17) (AU APRIL/MAY – 16)

A typical approach for modeling a VLSI interconnect is to use the distributed equivalent RC circuit of fig



The Elmore delay model explains the delay from input to output of the input signal, which is of a step function type. If the step response of the RC circuit is h(t), 50% point delay of the monotonic step response is the time TD that satisfies the following equation

Equation

$$\int_0^{T_D} h(t)\mathrm{d}t = 0.5.$$

32. Define floating body?

In SOI process technology, the source, body, and drain regions of transistors are insulated from the substrate. The body of each transistor is typically left unconnected and that results in floating body.

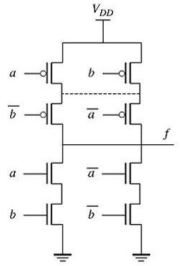
33. What is history effect?

In SOI process the body of nMOS and pMOS are floating instead of connecting to GND (nMOS) or VDD (pMOS) as in bulk CMOS. This floating body can change the MOS transistor threshold voltage due to differences in the body voltages. As the SOI circuit switches, the body voltages of the switching transistors will change from their previous steady state condition. This is called the History effect.

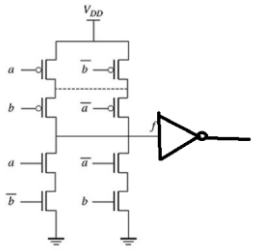
34. What is bubble pushing?

CMoS gates are inherently inverting, so AND and OR functions must be built from NAND and NOR gates. Demorgans law helps with this conversion. A NAND gate is equivalent to an OR of inverter inputs. A NOR gate is equivalent to an AND gate of inverter inputs. The same relationship applies to gates with more inputs switching between these representation is easy to do and is often called bubble pushing.

35. Draw XOR gate and XNOR gate using transmission gates.



XOR gate



XNOR

36. Write a note on CMoS transmission gate logic.(APRMAY 2011)

The transmission gate acts as voltage controlled resistor connecting the input and the output. It can be used as logic structure, switch, latch element etc,

37. What are the factors that cause static power dissipation in CMoS circuits? (Nov/Dec 2012)

Static power dissipation due to:

- Sub threshold conduction through OFF transistor.
- Tunneling current through gate oxide.
- Leakage through reverse biased diodes.

38. List the various power losses in CMoS circuits. (Nov/Dec 2013)

Static power dissipation

Dynamic power dissipation

 Charging and discharging of load capacitance

 Short circuit curerent while both PMoS and nMoS networks are partially ON

39. State types of power dissipation .(APR/MAY 2015)

 Static power dissipation

 Dynamic power dissipation

40. Give the expression for Elmore delay and state the various parameters associated with it.(NOV/DEC 2014) (MAY/JUN 2016)

Viewing on transistors as resistors a chain of transistors as an RC ladder. The Elmore model estimates the delay of an RC ladder as the sum over each node in the ladder of the resistance between that node and a supply multiplied by the capacitance on the node.

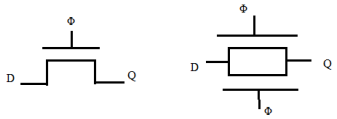
41. Define power dissipation.(NOV/DEC 2013)

The instantaneous power p(t) drawn from the power supply is proportional to the supply current iDD(t) and the supply voltage Vdd. The energy consumed over sometime interval T is the integral of the instantaneous power.

42. Implement a 2:1 multiplier using pass transistor(NOVDEC 2013)(APR/MAY 2015).

When an nMoS or pMoS is used alone as an imperfect switch, it is called as a pass transistor. By combining a nMoS and a pMoS transistor in parallel a switch is obtained that turns on when a 1 is applied to g in which 0's are passed in an acceptable fashion. this is a transmission gate or pass gate.

43. Design a 1-bit dynamic register using pass transistor.(NOV/DEC 2013)



The fig 1 shows a very simple transparent latch built from a single transistor it is compact and fast but suffers four limitations. Fig 2 uses a CMoS transmission gate in place of the sinlge nMoS pass transistor to offer rail-rail output swings.

44. Why single phase dynamic logic structure cannot be caed. justify(MAY/JUN 2016)

In dynamic logic, a problem arises when caing one gate to the next. The precharge "1" state of the first gate may cause the second gate to discharge prematurely, before the first gate has reached its correct state. This uses up the "precharge" of the second gate, which cannot be restored until the next clock cycle, so there is no recovery from this error

45. What is mean by power and power dissipation?

Power is the rate at which energy is delivered or exchanged; power dissipation is the rate at which energy is taken from the source (VDD) and converted into heat (electrical energy is converted into heat energy during operation).

46. What is mean by PDP?

Power delay product (PDP) = Pav * t p = (CL VDD 2)/2

PDP is the average energy consumed per switching event (watts * sec = joule).

47. What is EDP?

Energy delay product (EDP) = PDP* tp = Pav *tp2

EDP is the average energy consumed multiplied by the computation time required.

48. What are two types of power dissipation?

i) Static dissipation due to leakage current or other current drawn continuously from the power supply.

ii) Dynamic dissipation due to

a) Switching transient current.

b) Charging and discharging of load capacitances.

49. Define elmore delay model.

It is an analytical method used to estimate the RC delay in a network. Elmore delay model estimates the delay of a RC ladder as the sum over each node in the ladder of the resistance Rn-1 between that node and a supply multiplied by the capacitor on the nodes.

50. What are the general properties of elmore delay model?

General property of Elmore delay model network has Single input node All the capacitors are between a node and ground Network does not contain any resistive loop

PART –B

1.Explain the Examples of Combinational Logic Design?

Refer page no.230-240, Jan Rabaey, Anantha Chandrakasan, B.Nikolic, "Digital Integrated Circuits: A Design Perspective", Second Edition, Prentice Hall of India, 2003.

2.Explain the Elmore's constant & Pass transistor Logic? (AU NOV/DEC– 17)

Refer page no.259-264, Jan Rabaey, Anantha Chandrakasan, B.Nikolic, "Digital Integrated Circuits: A Design Perspective", Second Edition, Prentice Hall of India, 2003.

3.Define Transmission gates? (AU NOV/DEC– 17) (AU APRIL/MAY – 17) (AU APRIL/MAY – 16)

Refer page no.267-272, Jan Rabaey, Anantha Chandrakasan, B.Nikolic, "Digital Integrated Circuits: A Design Perspective", Second Edition, Prentice Hall of India, 2003.

4.Explain the static CMOS design? (AU NOV/DEC– 17) (AU APRIL/MAY – 16)

Refer page no.230-235, Jan Rabaey, Anantha Chandrakasan, B.Nikolic, "Digital Integrated Circuits: A Design Perspective", Second Edition, Prentice Hall of India, 2003.

5.Explain the dynamic CMOS design? (AU APRIL/MAY – 17) (AU NOV/DEC– 16)

Refer page no.272-280, Jan Rabaey, Anantha Chandrakasan, B.Nikolic, "Digital Integrated Circuits: A Design Perspective", Second Edition, Prentice Hall of India, 2003

6.Explain the Power dissipation? (AU NOV/DEC– 17) (AU APRIL/MAY – 17) (AU NOV/DEC– 16) (AU APRIL/MAY – 16)

Refer page no.186-190, N.Weste, K.Eshraghian, "Principles of CMOS VLSI Design", Second Edition, Addision Wesley 1993

7.Define the Low power design principles? (AU NOV/DEC– 17)

Refer page no.191-194, N.Weste, K.Eshraghian, "Principles of CMOS VLSI Design", Second Edition, Addision Wesley 1993\

8.Write short notes on Static CMOS Design. (MAY'11, MAY'13)

Refer page no.230-235, Jan Rabaey, Anantha Chandrakasan, B.Nikolic, "Digital Integrated Circuits: A Design Perspective", Second Edition, Prentice Hall of India, 2003.

9.Discuss in detail about the Dynamic CMOS design. (MAY'11)

Refer page no. 272-280, Jan Rabaey, Anantha Chandrakasan, B.Nikolic, "Digital Integrated Circuits: A Design Perspective", Second Edition, Prentice Hall of India, 2003.

10.Write a brief note on pass Transistor circuits also explain about CMOS with Transmission gates. (may 2011,2013) (MAY/JUN 2016)

Refer page no.267-272, Jan Rabaey, Anantha Chandrakasan, B.Nikolic, "Digital Integrated Circuits: A Design Perspective", Second Edition, Prentice Hall of India, 2003.

11.Explain about Pass-Transistor Logic. (MAY'13)

Refer page no.267-272, Jan Rabaey, Anantha Chandrakasan, B.Nikolic, "Digital Integrated Circuits: A Design Perspective", Second Edition, Prentice Hall of India, 2003

12.Explain the power dissipation present in VLSI circuits (Apr/May 2010) (Mayjun 2014)(Apr/May 2015) (May/Jun 2016)

Refer page no.186-190, N.Weste, K.Eshraghian, "Principles of CMOS VLSI Design", Second Edition, Addision Wesley 1993

13. Discuss in detail about the Propagation Delays, stick diagram, Layout diagrams

Refer page no.230-235, Jan Rabaey, Anantha Chandrakasan, B.Nikolic, "Digital Integrated Circuits: A Design Perspective", Second Edition, Prentice Hall of India, 2003.

14. Describe the basic principle of operation of dynamic CMOS ,domino and NP domino logic with neat diagrams.

Refer page no.160 - 172, Jan Rabaey, Anantha Chandrakasan, B.Nikolic, "Digital Integrated Circuits: A Design Perspective", Second Edition, Prentice Hall of India, 2003.

15. Explain the static and dynamic power dissipation in CMOS circuits with necessary diagrams and expressions.

Refer page no.120-133, Jan Rabaey, Anantha Chandrakasan, B.Nikolic, "Digital Integrated Circuits: A Design Perspective", Second Edition, Prentice Hall of India, 2003.

16. Briefly discuss about the classification of circuit families and comparison of circuit families.

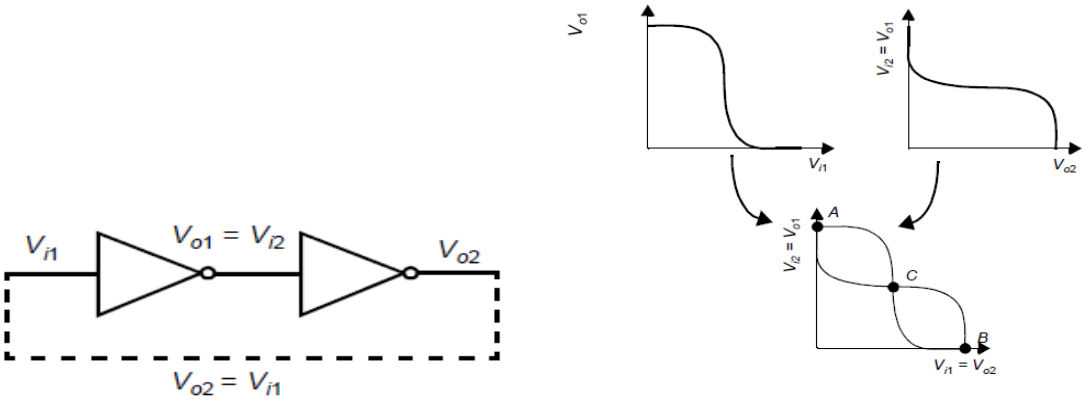
Refer page no.230-235, Jan Rabaey, Anantha Chandrakasan, B.Nikolic, "Digital Integrated Circuits: A Design Perspective", Second Edition, Prentice Hall of India, 2003.

UNIT III SEQUENTIAL LOGIC CIRCUITS AND CLOCKING STRATEGIES

Part-A

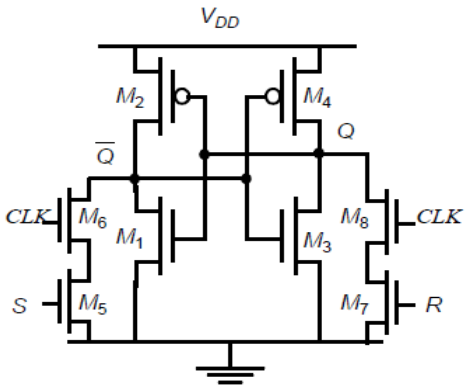
1.what is mean by Bistability Principle?

Static memories use positive feedback to create a bistable circuit — a circuit having two stable states that represent 0 and 1. which shows two inverters connected in cascade along with a voltage-transfer characteristic typical of such a circuit. Also plotted are the VTCs of the first inverter, that is, Vo1 versus Vi1, and the second inverter (Vo2 versus Vo1). The latter plot is rotated to accentuate that Vi2 = Vo1. Assume now that the output of the second inverter Vo2 is connected to the input of the first Vi1, as shown by the dotted lines in Figure. The resulting circuit has only three possible operation points (A, B, and C), as demonstrated on the combined VTC.



Two cascaded inverters

2.Draw the diagram of CMOS clocked SR flip-flop? (AU APRIL/MAY – 16)

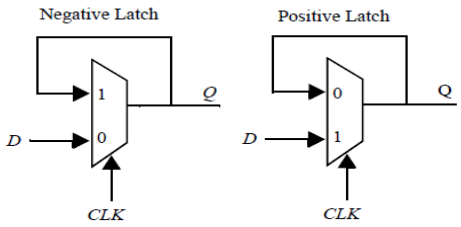


3.Define the Multiplexer-Based Latches?

One very common technique involves the use of transmission gate multiplexers. Multiplexer based latches can provide similar functionality to the SR latch, but has the important added advantage that the sizing of devices only affects performance and is not critical to the functionality.

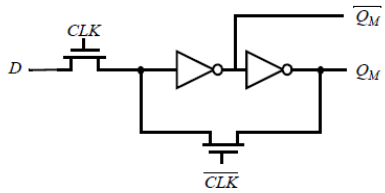
4. Define the Negative and positive latches based on multiplexers?

static positive and negative latches based on multiplexers. For a negative latch, when the clock signal is low, the input 0 of the multiplexer is selected, and the D input is passed to the output. When the clock signal is high, the input 1 of the multiplexer, which connects to the output of the latch, is selected. The feedback holds the output stable while the clock signal is high. Similarly in the positive latch, the D input is selected when clock is high, and the output is held (using feedback)when clock is low.

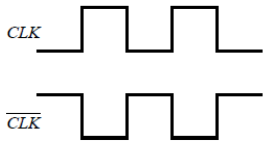


5. Define the Master-Slave Edge-Triggered Register? (AU APRIL/MAY – 16)

The most common approach for constructing an edge-triggered register is to use a masterslave configuration, as shown in Figure The register consists of cascading a negative latch (master stage) with a positive latch (slave stage). A multiplexer-based latch is used in this particular implementation, although any latch could be used. On the low phase of the clock, the master stage is transparent, and the D input is passed to the master stage output,



(a) Schematic diagram



(b) Non-overlapping clocks

6. Define clock jitter? (AU NOV/DEC– 17)

Clock jitter is the deviation of a clock edge from its ideal position in time. Simply speaking, it is the inability of a clock source to produce a clock with clean edges. As the clock edge can arrive within a range, the difference between two successive clock edges will determine the instantaneous period for that cycle. So, clock jitter is of importance while talking about timing analysis. There are many causes of jitter including PLL loop noise, power supply ripples, thermal noise, crosstalk between signals etc.

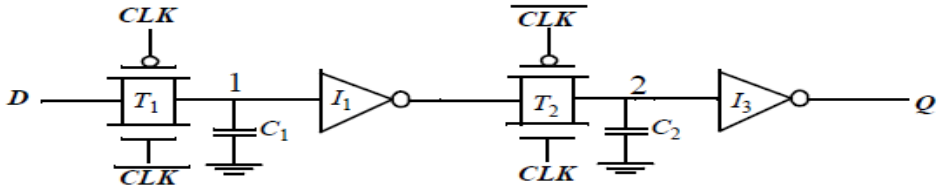
7. Define the Low-Voltage Static Latches?

The scaling of supply voltages is critical for low power operation. Unfortunately,certain latch structures don't function at reduced supply voltages. For example, without the scaling of device thresholds, NMOS only pass transistors don't scale well with supply voltage due to its inherent threshold drop. At very low power supply oltages, the input to the inverter cannot be raised above the switching threshold, resulting in incorrect evaluation. Even with the use of transmission gates, performance degrades significantly at reduced supply voltages.

8. What is mean Dynamic Latches and Registers?

Storage in a static sequential circuit relies on the concept that a cross-coupled inverter pair produces a bistable element and can thus be used to memorize binary values. This approach has the useful property that a stored value remains valid as long as the supply voltage is applied to the circuit, hence the name static. The major disadvantage of the static gate, however, is its complexity. When registers are used in computational structures that are constantly clocked such as pipelined datapath, the requirement that the memory should hold state for extended periods of time can be significantly relaxed.

9.Draw the Dynamic edge-triggered register?



10.Define The C2MOS Register?

positive edge-triggered register, based on a master-slave concept insensitive to clock overlap. This circuit is called the C2MOS.

11. Define the Sense-Amplifier Based Registers?

Sense-amplifier circuits accept small input signals and amplify them to generate rail-to-rail swings. As we will see, sense amplifier circuits are used extensively in memory cores and in low swing bus drivers to amplify small voltage swings present in heavily loaded wires. There are many techniques to construct these amplifiers, with the use of feedback

12.Define the Pipelining? (AU APRIL/MAY – 17) (AU NOV/DEC– 16)

Pipelining is a popular design technique often used to accelerate the operation of the datapaths

in digital processors.

13.write The Schmitt Trigger properties?

A Schmitt trigger is a device with two important properties:

1. It responds to a slowly changing input waveform with a fast transition time at the output.

2. The voltage-transfer characteristic of the device displays different switching thresholds for positive- and negative-going input signals. This is demonstrated where a typical voltage-transfer characteristic of the Schmitt trigger is shown (and its schematics symbol). The switching thresholds for the low-to-high and high to-low transitions are called VM+ and VM-, respectively. The hysteresis voltage is

defined as the difference between the two.

14.what is the Monostable Sequential Circuits?

A monostable element is a circuit that generates a pulse of a predetermined width every time the quiescent circuit is triggered by a pulse or transition event. It is called monostable because it has only one stable state (the quiescent one). A trigger event, which is either a signal transition or a pulse, causes the circuit to go temporarily into another quasi-stable state. This means that it eventually returns to its original state after a time period determined by the circuit parameters. This circuit, also called a one-shot

15.Define the Latches versus Registers?

• Latch: Level sensitive – transparent latch, D latch

• Flip-flop: edge triggered – master-slave flip-flop, D flip-flop, D register

16. List the methods of sequencing static circuits.

The three most widely used methods of sequencing static circuits

(i) Flip-flops

(ii) 2-Phase transparent latches

(iii) Pulsed latches

17. What is called pulsed latch?

The latch that has short clock-to-*Q* delay and a long hold time is called pulsed latch or single-phase level triggered latch.

18. Define propagation delay.

Upper bound on interval between valid inputs and valid outputs (or) the required interval times to change the output after applying the input signal is called propagation delay.

19. Define contamination delay.

It is the lower bound on interval between invalid inputs and invalid output is called the contamination delay.

20. What is pulsed latch?

Pulsed latch consisting of the set of pass gates that define the transparency window, buffer inverters, and weak feedback path to keep the value stored in the PL output at the end of transparency window.

21. What are the two types of reset?

The two types of reset are

1. Synchronous
2. Asynchronous

In synchronous reset, the flip-flop changes with synchronous control inputs and clock signal.

In asynchronous reset, the output is independent of the synchronous input and the clock input.

22. What is Differential flip-flops?

Differential flip-flops accept true and complementary inputs and produce true and complementary outputs. They are build from a clocked sense amplifier so they can rapidly respond to small differential input voltages

23. What is synchronizers? (AU APRIL/MAY – 17)

A synchronizer is a circuit that accepts an input that can change at arbitrary times and produces an output aligned to the synchronizer's clock. Because the input can change during the synchronizer's aperture, the synchronizer has a non zero probability of producing a metastable output

24. What is CMOS Domino logic?

A static CMOS inverter placed between dynamic gates which eliminate the monotonicity problem in dynamic circuits are called CMOS domino logic.

25. What are the properties of domino logic?

1. Only non-inverting logic can be implemented.
2. Very high speed having *tpHL* □□0
3. Eliminates the monotonicity problem.

26. What is Dual-rail domino logic

A circuit is said to be Dual-rail domino if each logical variable is represented by two wires, one that goes high if the signal is false, with this encoding, an input variable going true can cause an output variable to go true or false.

27. Define contamination delay.

It is the lower bound on interval between invalid inputs and invalid output is called the contamination delay.

28.Define Memory architecture ?

Memory architecture describes the methods used to implement electronic computer data storage in a manner that is a combination of the fastest, most reliable, most durable, and least expensive way to store and retrieve information. Depending on the specific application

29. Define dynamic memory?

Dynamic memory is commonly used for primary data storage due to its fast access speed. However dynamic memory must be repeatedly refreshed with a surge of current millions of time per second, or the stored data will decay and be lost. Flash memory allows for long-term storage over a period of years, but it is much slower than dynamic memory, and the static memory storage cells wear out with frequent use.

30. What is Differential flip-flops?

Differential flip-flops accept true and complementary inputs and produce true and complementary outputs. They are build from a clocked sense amplifier so they can rapidly respond to small differential input voltages.

31. Compare and contrast synchronous design and asynchronous design? (AU APRIL/MAY – 17)

Synchronous Sequential Circuit	Asynchronous Sequential Circuit
It is easy to design.	It is difficult to design.
A clocked flip flop acts as memory element.	An unclocked flip flop or time delay is used as memory element.
They are slower as clock is involved.	They are comparatively faster as no clock is used here.
The states of memory element is affected only at active edge of clock, if input is changed.	The states of memory element will change any time as soon as input is changed.

33. What is synchronous sequential circuit?

If all the registers are controlled by clock signal, then the circuit is called synchronous sequential logic circuit.

34. What is bistability principle?

Bistable state has two stable states. The two stable states are o and one.

35. What is metastable?

If the cross coupled inverter pair is biased at point **C** and small deviation at this point caused by noise is amplified and regenerated around the circuit loop. This small deviation is amplified by both the inverters and the bias point **C** moves the operation points A and B. so the bias point is unstable. This property is called metastable.

36. List the timing parameters of registers.

1. Set up time
2. Propagation delay
3. Hold time

37. What is race condition?

During the 0-0 overlap period, NMOS of t1 and PMOS t2 are simultaneously ON. This creates a direct path for data to flow from D input of the register to the Q output. This is called race condition.

38. List the drawbacks of static latches and registers.

The drawbacks of static latches and registers are

1. Stored value remains valid as long as supply voltage is available.
2. Complexity

39. Define global clock.

In synchronous circuits all the memory elements have a globally distributed periodic synchronous signal called global clock.

40. What is clock skew?

Clock skew is defined as the spatial variation in arrival time of clock transition on an integrated circuit. The clock skew between two points i and j on an IC.

41. What is clock jitter?

Clock jitter is defined as the temporal variation of the clock period at a given point on the chip. The clock period can reduce or expand on a cycle –by- cycle basis.

42. Define pipelining.

Pipelining is a designing technique used to increase the operation of datapaths in digital processor.

43. Define Propagation delay (tpd)?

This value indicates the amount of time needed for a change in a logic input to result in a **permanent** change at an output. Combinational logic is guaranteed not to show any further output changes in response to an input change **after** tpd time units have passed.

44. Define Contamination delay (tcd)?

This value indicates the amount of time needed for a change in a logic input to result in an **initial** change at an output. Combinational logic is guaranteed not to show any output change in response to an input change **before** tcd time units have passed.

45. What do you mean by Setup time (ts)?

This value indicates the amount of time before the clock edge that data input D must be stable. As shown in Figure 4, D is stable ts time units before the rising clock edge.

46. What do you mean by Hold time (th)?

This value indicates the amount of time after the clock edge that data input D must be held stable. As shown in Figure 4, the hold time is always measured from the rising clock edge (for positive edge-triggered) to a point after the edge.

47. What is Time Borrowing?

If one half-cycle or stage of a pipeline has too much logic, it can borrow time into the next half-cycle or stage. Time borrowing can accumulate across multiple cycles.

48. What is clocked CMoS register? (MAY/JUN 2016)

In integrated circuit design, **dynamic logic** (or sometimes **clocked logic**) is a design methodology in combinatory logic circuits, particularly those implemented in MOS technology.

49. Define contamination delay.

It is the lower bound on interval between invalid inputs and invalid output is called the contamination delay.

50.Define Memory architecture ?

Memory architecture describes the methods used to implement electronic computer data storage in a manner that is a combination of the fastest, most reliable, most durable, and least expensive way to store and retrieve information. Depending on the specific application

Part-B

1.Explain the Static and Dynamic Latches and Registers? TSPC register/NORA-CMOS latches (AU APRIL/MAY – 17) (AU NOV/DEC– 16) (AU APRIL/MAY – 16)

Refer page no.300-319, Jan Rabaey, Anantha Chandrakasan, B.Nikolic, "Digital Integrated Circuits: A Design Perspective", Second Edition, Prentice Hall of India, 2003

2.Define timing issues,pipe line and clock strategies? (AU NOV/DEC– 17) (AU APRIL/MAY – 17) (AU APRIL/MAY – 16)

Refer page no.325-337, Jan Rabaey, Anantha Chandrakasan, B.Nikolic, "Digital Integrated Circuits: A Design Perspective", Second Edition, Prentice Hall of India, 2003

3. Explain the Memory architecture ?

Refer page no.627-634, Jan Rabaey, Anantha Chandrakasan, B.Nikolic, "Digital Integrated Circuits: A Design Perspective", Second Edition, Prentice Hall of India, 2003

4.Briefly explain memory control circuits?

Refer page no.634-670, Jan Rabaey, Anantha Chandrakasan, B.Nikolic, "Digital Integrated Circuits: A Design Perspective", Second Edition, Prentice Hall of India, 2003

5.Explain the Low power memory circuits?

Refer page no.701-704, Jan Rabaey, Anantha Chandrakasan, B.Nikolic, "Digital Integrated Circuits: A Design Perspective", Second Edition, Prentice Hall of India, 2003

6.What is the Synchronous? Give example. (AU NOV/DEC– 17)

Refer page no.46-67(Section 10.3), Jan Rabaey, Anantha Chandrakasan, B.Nikolic, "Digital Integrated Circuits: A Design Perspective", Second Edition, Prentice Hall of India, 2003

7.What is the Asynchronous? Give example

Refer page no.67-81(Section 10.4), Jan Rabaey, Anantha Chandrakasan, B.Nikolic, "Digital Integrated Circuits: A Design Perspective", Second Edition, Prentice Hall of India, 2003

8. Explain about static latches in detail.

Refer page no.300-319, Jan Rabaey, Anantha Chandrakasan, B.Nikolic, "Digital Integrated Circuits: A Design Perspective", Second Edition, Prentice Hall of India, 2003

9. Explain about the concept of pipelining Non bistable Sequential Circuits.Timing classification of Digital Systems in detail (Dec-2012, May2014) (MAY/JUN 2016)

Refer page no.325-337, Jan Rabaey, Anantha Chandrakasan, B.Nikolic, “Digital Integrated Circuits: A Design Perspective”, Second Edition, Prentice Hall of India, 2003

10. Explain about Dynamic latches in detail. (MAY/JUN 2016)

Refer page no.300-319, Jan Rabaey, Anantha Chandrakasan, B.Nikolic, “Digital Integrated Circuits: A Design Perspective”, Second Edition, Prentice Hall of India, 2003

11. Explain the memory architecture in detail. Memory Classification

Refer page no.627-634, Jan Rabaey, Anantha Chandrakasan, B.Nikolic, “Digital Integrated Circuits: A Design Perspective”, Second Edition, Prentice Hall of India, 2003

12. Explain in detail about synchronous circuit design.

Refer page no.46-67(Section 10.3), Jan Rabaey, Anantha Chandrakasan, B.Nikolic, “Digital Integrated Circuits: A Design Perspective”, Second Edition, Prentice Hall of India, 2003

13. Write a brief note on sequencing dynamic circuits.

Refer page no.80-87(Section 10.3), Jan Rabaey, Anantha Chandrakasan, B.Nikolic, “Digital Integrated Circuits: A Design Perspective”, Second Edition, Prentice Hall of India, 2003

14. Explain in detail about the principle concepts used in sequential circuits.

Refer page no.80-87(Section 10.3), Jan Rabaey, Anantha Chandrakasan, B.Nikolic, “Digital Integrated Circuits: A Design Perspective”, Second Edition, Prentice Hall of India, 2003

15. Discuss in detail about dynamic RAM.

Refer page no.634-670, Jan Rabaey, Anantha Chandrakasan, B.Nikolic, “Digital Integrated Circuits: A Design Perspective”, Second Edition, Prentice Hall of India, 2003

UNIT IV INTERCONNECT , MEMORY ARCHITECTURE AND ARITHMETIC CIRCUITS

Part-A

1. What is Verilog HDL?

Verilog HDL is a Hardware description language that can be used to model a digital system at many levels of abstraction ranging from the algorithmic level to the gate level to the switch level.

2. What are the major capabilities of Verilog HDL?

- The language has in-built primitive logic gates, such as AND, OR and NAND etc.,
- The language allows flexibility for creating user defined primitives (UDP)
- Verilog HDL is non-proprietary and is an IEEE standard (IEEE 1076)
- The digital circuit can be modeled in four different styles. These styles are gate level, dataflow level, switch level and behavioral level.
- Two data types supported are net and register data type.

3. What is Design Methodology?

Identifying the primitive gates, sub blocks and macros required to implement a logic circuit is called Design Methodology.

4. What are the types of Design methodology?

(i) Top-down methodology

(ii) Bottom-up methodology

5. What is gate level modeling?

Design the logic circuit in terms of basic gates. All the basic gates are available as ready modules called “primitives”. Each such primitives is defined in terms of its inputs and outputs is called gate level modeling.

6. What is dataflow modeling?

Dataflow modeling provides the means of describing combinational circuits by their function rather than by their gate structure. Dataflow modeling uses a number of operators that act on operands to produce the desired results. Dataflow modeling uses continuous assignment statements.

7. What is Behavioral level modeling?

Behavioral modeling represents digital circuits at a functional and algorithmic level. It is used mostly to describe sequential circuits, as well as combinational circuits. Behavioral description use the keyword always and initial followed by a list of procedural assignment statements.

8. What is Test Bench?

A test bench is a virtual environment used to verify the correctness or soundness of a design or model.

9. What is a Module?

The basic unit of description in verilog is the module. A module describes the functionality or structure of a design and also describes the ports through which it communicates externally with other modules.

10. What is the difference between a module and instance?

A module can be an element or a collection of lower level design blocks, were as instances are the templates or the objects to a module.

11. Write the syntax of a module

module module_name (port_list);
//declaration
endmodule

12. What is a Port?

Ports provide the interface by which a module can communicate with its environment. For example, the input/output pins of an IC chip are its ports.

13. What are the different types of port in verilog HDL?

- Input port
- Output port
- Bidirectional port

14. What is an Identifier?

Identifiers are names given to objects so that they can be referenced in the design. An identifier in verilog HDL is any sequence of letters, digits, $ character and the underscore.

15. Give the application of High speed adder? (AU APRIL/MAY – 17)

- The carry lookahead adder is a faster circuit for adding binary numbers because it reduces the propagation time of carry values.

- Doing more work does not necessarily make a circuit slower. Circuits are inherently parallel, and you only count serial operations when discussing speed.
- Designing circuits involves trade-offs among speed, complexity, size and power.

16. What is Net data type?

A net data type represents a physical connection between structural elements. Its value is determined from the value of its drivers such as a continuous assignment or a gate output.

17. Give some examples for system task in verilog.

- $display
- $time
- $monitor
- $stop

18. What is complier directive?

A complier directive, when complied, remains in effect through the entire compilation process until a different complier directive specifies otherwise

19. What are the different types operators in verilog HDL?

1. Arithmetic
2. Logical
3. Relational
4. Equality
5. Bitwise
6. Reduction
7. Shift
8. Concatenation
9. Conditional

20. What is an initial statement?

An initial statement executes only once. It begins its execution at start of simulation which is at time zero. The syntax for the initial statement is :

initial

[timing_control] procedural_statement

21. What is an always statement?

An always statement executes repeatedly. It begins its execution at start of simulation which is at time zero. The syntax for the initial statement is :

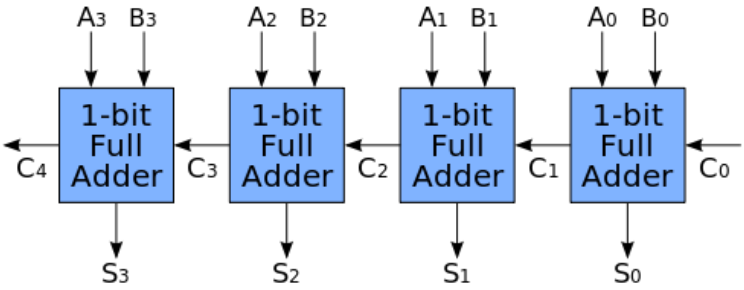
always

[timing_control] procedural_statement

22.Define the latency? (AU NOV/DEC– 17)

In computing, "latency" describes some type of delay. It typically refers to delays in transmitting or processing data, which can be caused by a wide variety of reasons. Two examples of latency are network latency and disk latency

23.Draw 4bit ripple carry adder ?



It is possible to create a logical circuit using multiple full adders to add N-bit numbers. Each full adder inputs a Cin, which is the Cout of the previous adder. This kind of adder is called a ripple-carry adder, since each carry bit "ripples" to the next full adder. Note that the first (and only the first) full adder may be replaced by a half adder (under the assumption that Cin = 0).

24.Define Lookahead carry unit?

By combining multiple carry lookahead adders even larger adders can be created. This can be used at multiple levels to make even larger adders. For example, the following adder is a 64-bit adder that uses four 16-bit CLAs with two levels of LCUs

25.Define Carry-save adders?

If an adding circuit is to compute the sum of three or more numbers it can be advantageous to not propagate the carry result. Instead, three input adders are used, generating two results: a sum and a carry. The sum and the carry may be fed into two inputs of the subsequent 3-number adder without having to wait for propagation of a carry signal. After all stages of addition, however, a conventional adder (such as the ripple carry or the lookahead) must be used to combine the final sum and carry results.

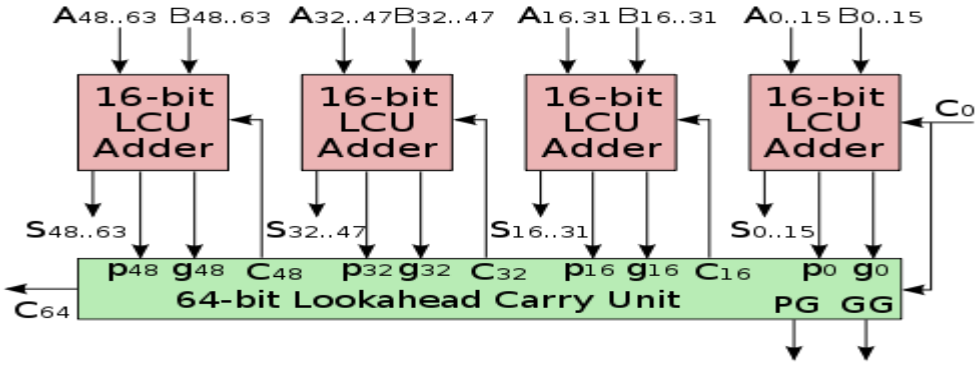
26.Define Carry – Skip Adder

A carry-skip adder (also known as a carry-bypass adder) is an adder implementation that improves on the delay of a ripple-carry adder with little effort compared to other adders. The improvement of the worst-case delay is achieved by using several carry-skip adders to form a block-carry-skip adder.

28.Define carry select adder?

The carry-select adder generally consists of two ripple carry adders and a multiplexer. Adding two n-bit numbers with a carry-select adder is done with two adders (therefore two ripple carry adders) in order to perform the calculation twice, one time with the assumption of the carry being zero and the other assuming one. After the two results are calculated, the correct sum, as well as the correct carry, is then selected with the multiplexer once the correct carry is known carry select adder

27.Draw Lookahead carry unit?



29.Define Carry – Save Adder?

A carry-save adder[1][2] is a type of digital adder, used in computer microarchitecture to compute the sum of three or more n-bit numbers in binary. It differs from other digital adders in that it outputs two numbers of the same dimensions as the inputs, one which is a sequence of partial sum bits and another which is a sequence of carry bits.

30.Define multiplier? (AU NOV/DEC– 16)

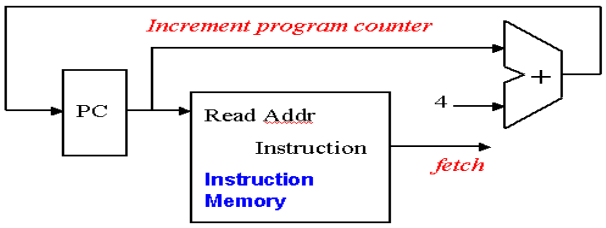
The common multiplication method is "add and shift" algorithm. In parallel multipliers number of partial products to be added is the main parameter that determines the performance of the multiplier. To reduce the number of partial products to be added, Modified Booth algorithm is one of the most popular algorithms. To achieve speed improvements Wallace Tree algorithm can be used to reduce the number of sequential adding stages.

31.Define barrel shifter? (AU NOV/DEC– 16)

A barrel shifter is a digital circuit that can shift a data word by a specified number of bits in oneclock cycle. It can be implemented as a sequence of multiplexers (mux.), and in such an implementation the output of one mux is connected to the input of the next mux in a way that depends on the shift distance.

32. List out the components of data path(AU APR/MAY– 17)

Data path components include memory (stores the current instruction), PC or program counter (stores the address of current instruction), and ALU(executes current instruction). The interconnection of these simple components to form a basic data path is illustrated in Figure Note that the register file is written to by the output of the ALU.



33. Define datapath circuits.

Datapath circuits use N identical circuits to process N-bit data. Related data operators are placed physically adjacent to each other to reduce wire length and delay.

34. What is ripple carry adder?

An N-bit adder can be constructed by caing N full adders. This is calleda carry-ripple adder (or ripple-carry adder). The carry-out of bit i, Ci is the carry-in to bit I + 1. This carry has twice the weight of the sum Si. The delay of the adder is set by the time for the carries to ripple through the N stages, so the delay is minimized.

35. What is the need of carry lookahead adder?

The carry-look ahead adder (CLA) computes group generate signals as well as group propagate signals to avoid waiting for a ripple to determine if the first group generates a carry.

36. List some high speed adders.

- Carry-skip adder
- Carry-select adder
- Carry-save adder

37. Give an example of binary multiplication

```
    011001 : 25₁₀      multiplicand
  × 100111 : 39₁₀      multiplier
    011001
   011001
  011001                partial
 000000                 products
000000
+011001
001111001111 : 975₁₀    product
```

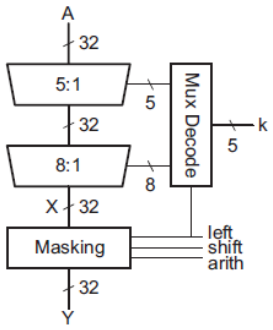
38. Define Booth encoding.

The speed of the multiplication can be increased by using a special encoding called booth encoding of the multiplier word that reduces the number of required addition stages. Instead of traditional binary encoding the multiplier word is recoded into radix-4 scheme.

39. What are the two types of dividers?

- Serial divider
- Parallel divider

40. Draw the schematic diagram of logarithmic barrel shifter.



41. What is the advantage of a carry-skip adder?

Carry-skip adder speeds up a wide adder by aiding the propagation of a carry bit around a portion of the entire adder.

42. What is the disadvantage of ripple-carry adder?

In ripple carry adder, every full-adder cell has to wait for the incoming carry before an outgoing carry is generated. This creates a linear dependency.

43. How to overcome the disadvantage of ripple-carry adder?

The disadvantage of ripple-carry adder is eliminated by the use of carryselect adder. It anticipates both possible values of the carry input and evaluates the result for both possibilities in advance. Once the real value of the incoming carry is known, the correct result is easily selected with a multiplexer.

44. What is meant by bit sliced data path organization? (MAY/JUN 2016)

A data path circuit is a circuit that combines two functions to a single logic cell. For instance, consider to design a full adder: ADD is a function that combines two inputs. Therefore in general, the layout of buswide logic that operates on data signals is called as a data path. The module add in a full adder is a data path.

45. Determine the propagation delay of n-bit carry select adder. (MAY/JUN 2016)

The propagation delay of N.bit carry select adder is given by Tp=tsetup+Mtcarry+(N/M)tmux+tsum

tsetup = Initial time taken to create the propagate and generate signals.

tcarry = defines the propagation delay through the single bit

tmux = delay incurred multiplexer for a single stage

tsum = defines the total time to generate the sum of the final stage

46. What are the various shift operations available?

Logical left shift

Logical right shift

Arithmetic left shift

Arithmetic right shift

47. What is the output after two arithmetic right shift for A=1001?

Input = 1001

After first arithmetic right shift = 1100

After second arithmetic right shift = 1110

48. What is a Manjestor carry chain adder?

It uses a cascade of pass transistors to implement the carry chain. Propogate & generate signals are generated using pass transistor logic. The capacitance per node on the carry chain is very small & equals only 4 diffusion capacitances.

49. Why is carry bypass Adder called so?

When the bypass control signal is set to '1', the incoming carry is forwarded immediately to the next block through a bypass transistor.

50. What is the importance of linear carry select Adder?

The linear dependencies present in a ripple carry adder is avoided in linear carry select adder, by anticipating both possible values of the carry i/p and evaluate the result for both possibilities in advance.

51. Why is the propagation delay in a carry select Adder is linearly proportional to N?

It is because the block select signal that selects between 0&1 solutions still has to ripple through all stages in worst case.

Part -B

1.Explain the Data path circuits ? (AU APRIL/MAY – 17)

Refer page no.560-561, Jan Rabaey, Anantha Chandrakasan, B.Nikolic, "Digital Integrated Circuits: A Design Perspective", Second Edition, Prentice Hall of India, 2003

2.Explain the Architectures for ripple carry adders?example. (AU NOV/DEC– 17) (AU NOV/DEC– 16)

Refer page no.561-568, Jan Rabaey, Anantha Chandrakasan, B.Nikolic, "Digital Integrated Circuits: A Design Perspective", Second Edition, Prentice Hall of India, 2003

3.Explain the Interconnect Parameters – Capacitance, Resistance, and Inductance, Electrical WireModels, Sequential digital circuits?

Refer page no.578-586, Jan Rabaey, Anantha Chandrakasan, B.Nikolic, "Digital Integrated Circuits: A Design Perspective", Second Edition, Prentice Hall of India, 2003

4.write the High speed adders? (AU NOV/DEC– 17) (AU APRIL/MAY – 16)

Refer page no.561-586, Jan Rabaey, Anantha Chandrakasan, B.Nikolic, "Digital Integrated Circuits: A Design Perspective", Second Edition, Prentice Hall of India, 2003

5.Define the accumulators program?

Refer page no.236-241, A.Pucknell, Kamran Eshraghian , "BASIC VLSI Design", Third Edition, Prentice Hall of India, 2007

6.Define Multipliers and give example? (AU NOV/DEC– 17) (AU APRIL/MAY – 17) (AU NOV/DEC– 16) (AU APRIL/MAY – 16)

Refer page no.586-594, Jan Rabaey, Anantha Chandrakasan, B.Nikolic, "Digital Integrated Circuits: A Design Perspective", Second Edition, Prentice Hall of India, 2003

7.what is mean by dividers and explain?

Refer page no.78-81(Section 10.4), Jan Rabaey, Anantha Chandrakasan, B.Nikolic, "Digital Integrated Circuits: A Design Perspective", Second Edition, Prentice Hall of India, 2003

8.Explain the Barrel shifters? (AU NOV/DEC– 16)

Refer page no.595-596, Jan Rabaey, Anantha Chandrakasan, B.Nikolic, "Digital Integrated Circuits: A Design Perspective", Second Edition, Prentice Hall of India, 2003

9.Explain speed and area tradeoff? (AU APRIL/MAY – 17)

Refer page no.600-619, Jan Rabaey, Anantha Chandrakasan, B.Nikolic, "Digital Integrated Circuits: A Design Perspective", Second Edition, Prentice Hall of India, 2003

10. Describe about carry look-ahead adder and its carry generation and propagation

Refer page no.578-586, Jan Rabaey, Anantha Chandrakasan, B.Nikolic, "Digital Integrated Circuits: A Design Perspective", Second Edition, Prentice Hall of India, 2003

11. Explain with neat diagram baugh-wooley multiplier

Refer page no.586-594, Jan Rabaey, Anantha Chandrakasan, B.Nikolic, "Digital Integrated Circuits: A Design Perspective", Second Edition, Prentice Hall of India, 2003

12. Explain multiplication with an example and discuss the different types of multipliers. (Nov-2010) (MAY/JUN 2016)

Refer page no.586-594, Jan Rabaey, Anantha Chandrakasan, B.Nikolic, "Digital Integrated Circuits: A Design Perspective", Second Edition, Prentice Hall of India, 2003

13. Explain the following circuits 1. Data path circuit 2. Any one adder circuit

Refer page no.560-561, Jan Rabaey, Anantha Chandrakasan, B.Nikolic, "Digital Integrated Circuits: A Design Perspective", Second Edition, Prentice Hall of India, 2003

14. What is mean by the Memory Architecture and Building Blocks, Memory Core and Memory Peripherals Circuitry.

Refer page no.78-81(Section 10.4), Jan Rabaey, Anantha Chandrakasan, B.Nikolic, "Digital Integrated Circuits: A Design Perspective", Second Edition, Prentice Hall of India, 2003

15. Design a 16 bit carry by pass and carry select addersand discuss their Features. (MAYJUN 2016)

Refer page no.578-586, Jan Rabaey, Anantha Chandrakasan, B.Nikolic, "Digital Integrated Circuits: A Design Perspective", Second Edition, Prentice Hall of India, 2003

16. Explain the Logic Implementation using Programmable Devices (ROM, PLA, FPGA).

Refer page no.586-594, Jan Rabaey, Anantha Chandrakasan, B.Nikolic, "Digital Integrated Circuits: A Design Perspective", Second Edition, Prentice Hall of India, 2003

17. Design a 3 bit barrel shifter

Refer page no.595-596, Jan Rabaey, Anantha Chandrakasan, B.Nikolic, "Digital Integrated Circuits: A Design Perspective", Second Edition, Prentice Hall of India, 2003

UNIT V ASIC DESIGN AND TESTING

Part-A

1. What is mean by full custom?

Full-custom design is a methodology for designing integrated circuits by specifying the layout of each individual transistor and the interconnections between them. Alternatives to full-custom design include various forms of semi-custom design, such as the repetition of small transistor sub circuits one such methodology is the use of standard cell libraries (standard cell libraries are themselves designed using full-custom design techniques).

Full-custom design potentially maximizes the performance of the chip, and minimizes its area, but is extremely labor-intensive to implement. Full-custom design is limited to ICs that are to be fabricated in extremely high volumes, notably certain microprocessors and a small number of ASICs.

2.Give the different types of ASIC?

1. Full custom ASICs

2. Semi-custom ASICs

* standard cell based ASICs

* gate-array based ASICs

3. Programmable ASICs

* Programmable Logic Device (PLD)

* Field Programmable Gate Array (FPGA).

3. What is the full custom ASIC design? (AU APRIL/MAY – 16)

In a full custom ASIC, an engineer designs some or all of the logic cells, circuits or layout specifically for one ASIC. It makes sense to take this approach only if there are no suitable existing cell libraries available that can be used for the entire design.

4. What is the standard cell-based ASIC design? (AU APRIL/MAY – 17) (AU NOV/DEC– 16)

A cell-based ASIC (CBIC) uses predesigned logic cells known as standard cells. The standard cell areas also called flexible block sin a CBIC are built of rows of standard cells. The ASIC designer defines only the placement of standard cells and the interconnecting a CBIC. All the mask layers of a CBIC are customized and are unique to a particular customer.

5. Differentiate between channeled & channel less gate array.

Channeled Gate Array:

Only the interconnect is customized. The interconnect uses predefined spaces between rows of base cells. Routing is done using the spaces. Logic density is less

Channel less Gate Array:

Only the top few mask layers are customized. No predefined areas are set aside for routing between cells. Routing is done using the area of transistors unused. Logic density is higher.

6. What is a FPGA?

A field programmable gate array (FPGA) is a programmable logic device that supports implementation of relatively large logic circuits. FPGAs can be used to implement a logic circuit with more than 20,000 gates whereas a CPLD can implement circuits of uptoabout 20,000 equivalent gates.

7. What are the different methods of programming of PALs?

The programming of PALs is done in three main ways:

•Fusible links

•UV – erasable EPROM

•EEPROM (E2PROM) – Electrically Erasable Programmable ROM

8. What are the different levels of design abstraction at physical design?

•Architectural or functional level

•Register Transfer-level (RTL)

•Logic level

•Circuit level

9.What is an anti fuse? (AU NOV/DEC– 17)

A programmable chip technology that creates permanent, conductive paths between transistors. In contrast to "blowing fuses" in the fusible link method, which opens a circuit by breaking apart a conductive path, the anti fuse method closes the circuit by "growing" a conductive

PLDs have advantages over SRAM based PLDs in that like ASICs, they do not need to be configured each time power is applied. They may be less susceptible to alpha particles which can cause circuits to malfunction.

.10. What are Programmable Interconnects?macros

In a PAL, the device is programmed by changing the characteristics if the switching element. An alternative would be to program the routing.

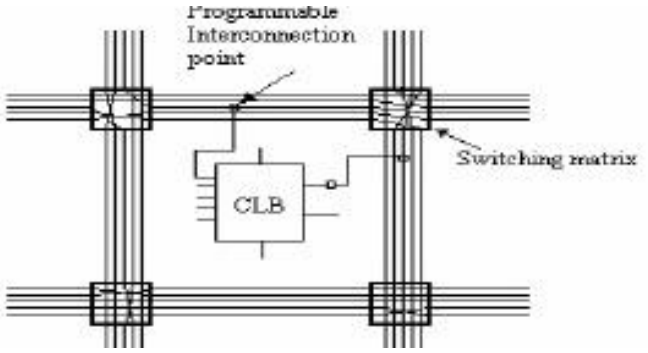
Macros:

The logic cells in a gate-array library are often called macros

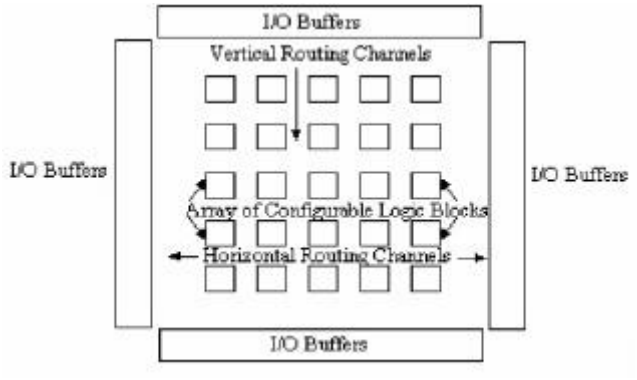
11. Give the steps in ASIC design flow.

- Design entry
- Logic synthesis System partitioning
- Pre layout simulation.
- Floor planning
- Placement
- Routing
- Extraction
- Post layout simulation

12.Give the XILINX Configurable Logic Block ? (AU APRIL/MAY – 17)



13.Give the XILINX FPGA architecture?



14.Define standard cell based IC vs custom design IC?

Standard cell based IC:

Design using standard cells

Standard cells come from library provider

Many different choices for cell size, delay, leakage power

Many EDA tools to automate this flow „ Shorter design time

Custom design IC:

Design all by yourself

Higher performance

15. Define Standard cells design flow?

FRONT END

System specification and architecture

HDL coding & behavioral simulation

Synthesis & gate level simulation

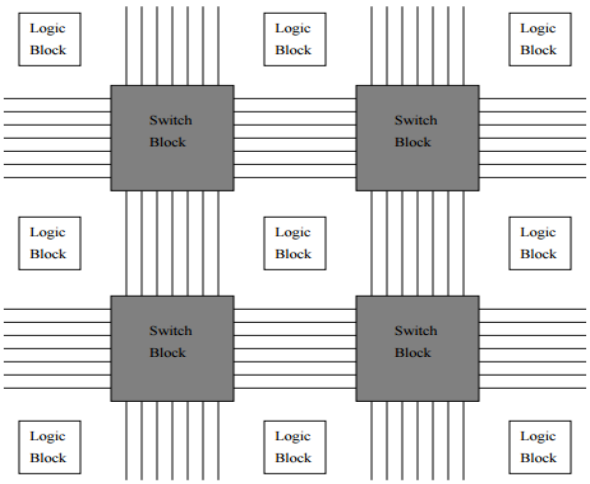
BACK END

Placement and routing

DRC (Design Rule Check), LVS (Layout vs Schematic)

dynamic simulation and static analysis

16.Draw Island-Style FPGA?



17.How Logic blocks of an FPGA can be implemented?

1. Transistor pairs

2. combinational gates like basic NAND gates or XOR gates

3. n-input Lookup tables

4. Multiplexers

5. Wide fan-in And-OR structure.

18.Define SSI, MSI, LSI and VLSI.

SSI: Small scale Integration where the no of transistor fabricated in an IC is less than 10.

MSI: Medium scale Integration where the no of transistor fabricated in an IC is approximately 10 to 1000 gates.

LSI: Large Scale Integration where the no of transistor fabricated in an IC is thousands of gates.

VLSI: Very large Scale Integration where the no of transistor fabricated in an IC is hundreds of thousands of gates.

19. What are the different tools available in a typical CAD tool set.

Design rule checker (DRC)

Layout versus Schematic (LVS)

Circuit Extractor

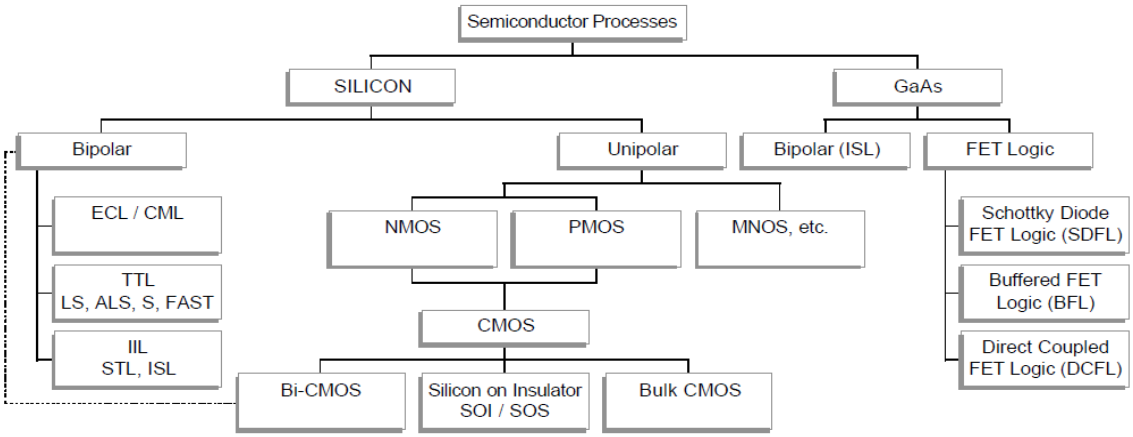
Circuit simulators

Orcad

Simucad

PALASM

20.Types of IC Fabrication Technologies?



21.What is DFT?

Design for Testability (DFT) is set of design rules and guidance for controllability and Observability to facilitate the testing of a circuit. Design for testability (DFT) refers to those design techniques that make test generation and test application cost-effective

22. What is Built-in Self-Test?

Built-in Self-Test are used to determine the correctness of a circuit by examining a signature, which is some statistical property of the circuit.

23. What are the types of testing carry out in Built-in Self-Test?

- Single combinational / sequential stuck-at faults
- Delay faults
- Single stuck-at faults in BIST hardware

24. What is LFSR?

LFSR – Linear feedback shift register, hardware that generates pseudo-random pattern sequence.

25. What is Pseudo-random testing?

Pseudo-random testing – Algorithmic pattern generator that produces a subset of all possible tests with most of the properties of randomly-generated patterns.

26. What is Boundary scan testing?

Boundary scan is a methodology allowing complete controllability and observability of the boundary pins of a JTAG compatible device via software control. This capability enables in-circuit testing without the need of bed-of-nail in-circuit test equipment. Boundary scan provides the following major modes of operation

- In non-invasive mode
- The pin-permission mode

27.Define Design for Testability?

Design-for-Test-the action of placing features in a chip design during the design process to enhance the ability to generate vectors, achieve a measured quality level,
or reduce the cost of - test.

There are two key concepts underlying all considerations for testability.

They are:

1. Controllability
2. Observability

28. Define Scan Design Techniques?

The implementation of a scan architecture consisting of using scan able sequential elements, and including the scan data and control connections that lead to a structured approach to testability.

29.Define Scan Design Rules?

A circuit is design to meet its functional requirements. After the functional correctness of the design is verified, it is modified to include the scan function. In order to be able to make it scan-testable, the designer must adhere to certain rules during the functional design.

The following four rules must be followed:

1. Only D-type master-slave flip-flops should be used.
2. At least one primary input pin must be available for test.
3. All flip-flops clocks must be controllable from primary inputs.
4. Clocks must not feed data inputs of flip-flop.

30.What is Boundary scan testing?

Boundary scan is a methodology allowing complete controllability and observability of the boundary pins of a JTAG compatible device via software control. This capability enables in-circuit testing without the need of bed-of-nail in-circuit test equipment. Boundary scan provides the following major modes of operation:

□□In non-invasive mode

□□The pin-permission mode

31. What is Testers?

A tester is a device which is used to drive the inputs and to monitor the outputs of a device-under-test. Testers are popularly known as ATE [Automatic Test Equipment].

32. What is test fixtures?

A socket for transmitting electrical signals from the test signal generation [IC tester] to an IC device-under-test (DUT) is called test fixtures.

33. What is shmooing?

Shmooing is the ability to vary the voltage and timing on a per-pin basis with a tester. Schmoo plot gives the speed sensitivity of that part with respect to voltage. Schmoo test is the skew timing on the inputs with respect to chip clock to look for setup and hold variation

34. What is ULSI? (AU NOV/DEC– 17)

Ultra large-scale integration (ULSI) is the process of integrating or embedding millions of transistors on a single silicon semiconductor microchip. ULSI technology was conceived during the late 1980s when superior computer processor microchips, specifically for the Intel 8086 series, were under development. ULSI is a successor to large-scale integration (LSI) and very large-scale integration (VLSI) technologies but is in the same category as VLSI.

35. What is an interconnect?

The last half dozen or so layers define metal wires between the transistors are called interconnect.

36. Define Manufacturing lead time

It is defined as the time it takes to make am IC not including the design time.

37. Define Flexible blocks.

The predefined logic cells are known as standard cells. The standard cell areas are called flexible blocks.

40. Define Mega cells

The flexible blocks used in combination with larger predesigned cells, like micro controllers and micro processors, these are called mega cells.

41. List the advantages of CBIC(Nov-2009)

 Less cost

 Less time

 Reduced Risk

 Transistor operates at maximum speed.

42. What are primitive cells?

The predefined pattern of transistors on a gate array is the base array. The base array is made up of a smallest element called primitive cell.

43. Define Customer owned tooling.

If an ASIC design is completed using cell library we own the mask that are used to manufacture the ASIC. This is called Customer owned tooling.

44. Write the features of Xilinx LCA.(April 2008)

1. Vertical lines and horizontal lines run between CLB's
2. Long lines run across the entire chip to form internal buses
3. Direction connection bypasses the switch matrices and directly connects adjacent CLB
4. General purpose interconnect joins switch boxes or magic boxes or switching matrices.

45. Write the advantages of altera max 5000 and 7000?

1. It uses a fixed no. of connections.
2. Fixed routing delay
3. Simple and improved speed in placement and routing software

46. Write about FPGA routing techniques.

 Comprises of programmable switches and wires

 Provides connection between I/O blocks, Logic blocks, etc.

 Routing decides logic block density and area consumed. Different routing techniques are

 Xilinx routing architecture

 Actel routing methodology

 Altera routing methodology

47. Give the different types of ASIC.

1. Full custom ASICs

2. Semi-custom ASICs

* Standard cell based ASICs

* Gate-array based ASICs

3. Programmable ASICs

* Programmable Logic Device (PLD)

* Field Programmable Gate Array (FPGA).

48. What is the full custom ASIC design? (May 2008,May 2009)

In a full custom ASIC, an engineer designs some or all of the logic cells, circuits or layout specifically for one ASIC. It makes sense to take this approach only if there are no suitable existing cell libraries available that can be used for the entire design.

49. What is the standard cell-based ASIC design? (May 2008)

A cell-based ASIC (CBIC) uses predesigned logic cells known as standard cells. The standard cell areas also called fle4xible blocks in a CBIC are built of rows of standard cells. The ASIC designer defines only the placement of standard cells and the interconnect in a CBIC. All the mask layers of a CBIC are customized and are unique to a particular customer.

50. Differentiate between channeled & channel less gate array.

Channeled Gate Array	**Channel less Gate Array**
1. Only the interconnect is customized layers customized.	Only the top few mask
2. The interconnect uses predefined spaces between rows of base cells.	No predefined areas are set aside For routing between
3. Routing is done using the cells. spaces transist unused.	Routing is done using the area
4. Logic density is less	Logic density is higher.

51. What is a FPGA?

A field programmable gate array (FPGA) is a programmable logic device that supports implementation of relatively large logic circuits. FPGAs can be used to implement a logic circuit

with more than 20,000 gates whereas a CPLD can implement circuits of upto about 20,000 equivalent gates.

52. What are the types of programmable device?

 Programmable logic structure

 Interconnect

 Reprogrammable gate array

53. What are the essential characteristics of an FPGA?

 None of the mask layers are customized.

 A method for programming the basic logic cells and the interconnect.

 The core is a regular array of programmable basic logic cells that can implement combinational as well as sequential logic (flip-flops).

 A matrix of programmable interconnect surrounds the basic logic cells.

54. State the features of full custom ASIC Design. (MAY/JUN 2016)

Full Custom ASIC:

 Full custom includes all possible logic cells and mask layers that are customized.

 These are very expensive to manufacture and design.

 Example is microprocessor.

 In full custom ASIC an engineer design some or all logic cells ,circuits, or layout specifically for one ASIC.

55.What are feed through cells? State their uses.(MAY/JUN 2016)

A feedthrough is a conductor used to carry a signal through an enclosure or printed circuit board. Like any conductor, it has a small amount of capacitance. A "feedthrough capacitor" has a guaranteed minimum value of shunt capacitance built in it and is used for bypass purposes in ultra-high-frequency applications.

Part-B

1.Explain the Introduction to wafer to chip fabrication process flow? (AU NOV/DEC– 17) (AU APRIL/MAY – 17) (AU APRIL/MAY – 16)

Refer page no.19-20, Michael John Sebastian Smith, "Application-Specific Integrated Circuits", Second Edition, Addison Wesley Professional 1997.

2.Explain the Microchip design process & issues in test and verification of complex chips, embedded cores and SOCs, Fault models**? (AU NOV/DEC– 17) (AU NOV/DEC– 16) (AU APRIL/MAY – 16)**

Refer page no.19-20, Michael John Sebastian Smith, "Application-Specific Integrated Circuits", Second Edition, Addison Wesley Professional 1997.

3.Explain the Standard cell design and cell libraries?

Refer page no.20-28, Michael John Sebastian Smith, "Application-Specific Integrated Circuits", Second Edition, Addison Wesley Professional 1997.

4.Explain the Fault models, Test coding? (AU NOV/DEC– 17) (AU APRIL/MAY – 17) (AU NOV/DEC– 16)

Refer page no.30-31, Michael John Sebastian Smith, "Application-Specific Integrated Circuits", Second Edition, Addison Wesley Professional 1997.

5.Explain the FPGA interconnect routing procedures? (AU NOV/DEC– 17) (AU APRIL/MAY – 17) (AU APRIL/MAY – 16)

Refer page no.184-186, Michael John Sebastian Smith, "Application-Specific Integrated Circuits", Second Edition, Addison Wesley Professional 1997.

6.Explain the general architecture of FPGA and bring about different programmable blocks used.

Refer page no.30-31, Michael John Sebastian Smith, "Application-Specific Integrated Circuits", Second Edition, Addison Wesley Professional 1997.

7.Discuss in detail ASIC Design Flow, Introduction to ASICs?

Refer page no.19-20, Michael John Sebastian Smith, "Application-Specific Integrated Circuits", Second Edition, Addison Wesley Professional 1997.

8.Describe about the Introduction to test benches

Refer page no.20-28, Michael John Sebastian Smith, "Application-Specific Integrated Circuits", Second Edition, Addison Wesley Professional 1997.

9.write short note on test benches in Verilog HDL

Refer page no.184-186, Michael John Sebastian Smith, "Application-Specific Integrated Circuits", Second Edition, Addison Wesley Professional 1997.

10.Write short notes on , Automatic test pattern generation?

Refer page no.20-28, Michael John Sebastian Smith, "Application-Specific Integrated Circuits", Second Edition, Addison Wesley Professional 1997.

11.Write the significance of Design for testability, Scan design?

Refer page no.28-32, Michael John Sebastian Smith, "Application-Specific Integrated Circuits", Second Edition, Addison Wesley Professional 1997.

12.Explain the Test interface and boundary scan.

Refer page no.184-186, Michael John Sebastian Smith, "Application-Specific Integrated Circuits", Second Edition, Addison Wesley Professional 1997.

13. Explain about the classification of ASIC. (Nov 2007, Nov 2008, May 2008, May 2009, May 2010) (MAY/JUN2016)

Refer page no.20-28, Michael John Sebastian Smith, "Application-Specific Integrated Circuits", Second Edition, Addison Wesley Professional 1997.

14. Explain about ASIC Design Flow

Refer page no.20-28, Michael John Sebastian Smith, "Application-Specific Integrated Circuits", Second Edition, Addison Wesley Professional 1997.

15. Explain about ASIC cell library in detail

Refer page no.20-28, Michael John Sebastian Smith, "Application-Specific Integrated Circuits", Second Edition, Addison Wesley Professional 1997.

16. Explain in detail about FPGA Interconnecting Procedure.(MAY/JUN 2016)

Refer page no.184-186, Michael John Sebastian Smith, "Application-Specific Integrated Circuits", Second Edition, Addison Wesley Professional 1997.

17. Explain about XILINX in detail. (MAY/JUN2016)

Refer page no.30-31, Michael John Sebastian Smith, "Application-Specific Integrated Circuits", Second Edition, Addison Wesley Professional 1997.

JEPPIAAR ENGINEERING COLLEGE

Department of ECE

Anna University Question Paper code :57297

B.E/B.TECH.DEGREE EXAMINATION, May/June 2016

Sixth Semester

EC 6601 – VLSI DESIGN

Part-A

1. **State channel length Modulation .Write down the equation for describing the channel length modulation effect in NMOS transistors?**

Ideally, Ids is independent of Vds for a transistor in saturation region, making the transistor a perfect current source. For non-ideal transistor, the actual length of the inverted channel gradually decreases as the potential difference between the gate and the drain increases. This effect is called the channel length modulation. The channel length modulation effect typically increases in small devices with low-doped substrates. An extreme case of channel length modulation is punch through where the channel length reduces to zero.

2. **What is Latch up? How to prevent latch up?**

- Latch is the generation of a low-impedance path in CMOS chips between the power supply and the ground rails due to interaction of parasitic pnp and npn bipolar transistors. These BJTs for a silicon-controlled rectifier with positive feedback and virtually short circuit the power and the ground rail.
- This causes excessive current flows and potential permanent damage to the devices.
- Analysis of the a CMOS Inverter CMOS depicting the parasitics.

Preventing Latch-Up:

It is possible to design chips to be resistant to latch-up by adding a layer of insulating oxide (called a trench) that surrounds both the NMOS and the PMOS transistors. This breaks the parasitic SCR structure between these transistors. Such parts are important in the cases where the proper sequencing of power and signals cannot be guaranteed, such as hot swap devices.

Devices fabricated in lightly doped epitaxial layers grown on heavily doped substrates are also less susceptible to latch-up. The heavily doped layer acts as a current sink where excess minority carriers can quickly recombine.

3. **Give Elmore Delay expression for propagation delay of an inverter**

Elmore Delay MOS equations

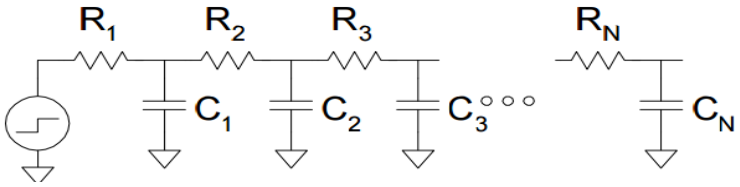
ON transistors look like resistors

Pullup or pulldown network modeled as RC ladder

Elmore delay of RC ladder

$$t_{pd} \approx \sum_{\text{nodes } i} R_{i-to-source} C_i$$

$$= R_1 C_1 + (R_1 + R_2) C_2 + \ldots + (R_1 + R_2 + \ldots + R_N) C_N$$



A. Introduction

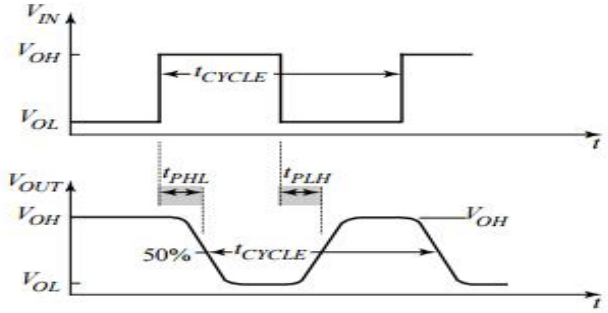
- Propagation delays t_{PHL} and t_{PLH} define ultimate speed of logic
- Define Average Propagation Delay

$$t_p = \frac{(t_{PHL} + t_{PLH})}{2}$$

- Typical complex system has 20-50 propagation delays per clock cycle.
- Typical propagation delays < 1nsec

B. Hand Calculation

- Use an input signal that has t_r=0 and t_f=0 for hand calculation
- Calculate current drive
- Calculate capacitance being driven



4. **why single phase dynamic logic structure cannot be cascaded? Justify**

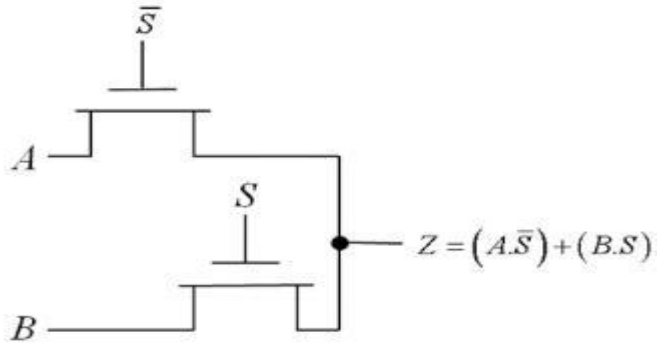
In dynamic logic, a problem arises when cascading one gate to the next. The precharge "1" state of the first gate may cause the second gate to discharge prematurely, before the first gate has reached its correct state. This uses up the "precharge" of the second gate, which cannot be restored until the next clock cycle, so there is no recovery from this error.[1]

In order to cascade dynamic logic gates, one solution is Domino Logic, which inserts an ordinary static inverter between stages. While this might seem to defeat the point of dynamic logic, since the inverter has a pFET (one of the main goals of Dynamic Logic is to avoidpFETs where possible, due to speed), there are two reasons it works well. First, there is no fanout to multiple pFETs; the dynamic gate connects to exactly one inverter, so the gate is still very fast. Furthermore, since the inverter connects to only nFETs in dynamic logic gates, it too is very fast. Second, the pFET in an inverter can be made smaller than in some types of logic gates.

In Domino logic cascade structure of several stages, the evaluation of each stage ripples the next stage evaluation, similar to a domino falling one after the other. Once fallen, the node states cannot return to "1" (until the next clock cycle) just as dominos, once fallen, cannot stand up, justifying the name Domino CMOS Logic. It contrasts with other solutions to the cascade problem in which cascading is interrupted by clocks or other means.

5. Draw the switch level schematic of multiplexer based nmos latch using nmos only pass transistors for multiplexers

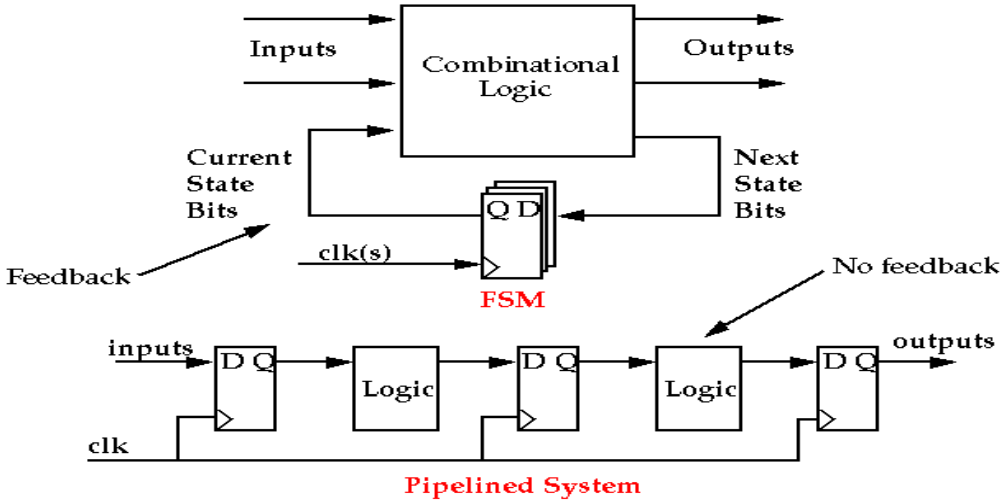
A multiplexer can be designed using various logics. Fig shows how a 2:1 MUX is implemented using a pass-transistor logic.



The pass-transistor logic attempts to reduce the number of transistors to implement a logic by allowing the primary inputs to drive gate terminals as well as source-drain terminals. The implementation of a 2:1 MUX requires 4 transistors (including the inverter required to invert S), while a complementary CMOS implementation would require 6 transistors. The reduced number of devices has the additional advantage of lower capacitance.

6. **What is clocked Cmos Register?**

- Majority of VLSI systems are Finite State machines and Pipelined machines:



7. What is meant by bit sliced data path organization?

Bit sliced is a technique for constructing a processor from modules of smaller bit width. Each of these components processes one bit field or "slice" of an operand. The grouped processing components would then have the capability to process the chosen full word-length of a particular software design

8. **Determine propagation delay of n-bit carry select adder**

The carry-select adder generally consists of two ripple carry adders and a multiplexer. Adding two n-bit numbers with a carry-select adder is done with two adders (therefore two ripple carry adders) in order to perform the calculation twice, one time with the assumption of the carry-in being zero and the other assuming it will be one. After the two results are calculated, the correct sum, as well as the correct carry-out, is then selected with the multiplexer once the correct carry

9. **What are feed through cells? State their uses**

A "feedthrough capacitor" has a guaranteed minimum value of shunt capacitance built in it and is used for bypass purposes in ultra-high-frequency applications. Feedthroughs can be divided into power and instrumentation categories. Power feedthroughs are used to carry either high current or high voltage. Instrumentation feedthroughs are used to carry electrical signals (including thermocouples) which are normally low current or voltage. Another special type is what is commonly known as RF-feedthrough, specifically designed to carry very high frequency RF or microwave electrical signals.

10. **State the Features of Full custom Design**

A full-custom IC includes some (possibly all) logic cells that are customized and all mask layers that are customized. A microprocessor is an example of a full-custom IC—designers spend many hours squeezing the most out of every last square micron of microprocessor chip space by hand. Customizing all of the IC features in this way allows designers to include analog circuits, optimized memory cells, or mechanical structures on an IC, for example. Full-custom ICs are the most expensive to manufacture and to design

PART-B

11.(a)(i)Describe the equation for source to drain current in the three region of operation of a MOS transistor and draw the VI characteristics (8)

Refer page no.25-34, A.Pucknell, Kamran Eshraghian , “BASIC VLSI Design”, Third Edition, Prentice Hall of India, 2007

(ii) Explain in detail about the body effect and its effect in MOS device(8)

Refer page no.14-22, A.Pucknell, Kamran Eshraghian , “BASIC VLSI Design”, Third Edition, Prentice Hall of India, 2007

(or)

(b)(i) Explain the DC transfer characteristics of a CMOS inverter with necessary conditions for the different Regions of operation(8)

Refer page no.30-34, A.Pucknell, Kamran Eshraghian , “BASIC VLSI Design”, Third Edition, Prentice Hall of India, 2007

(ii)Discuss the principle of Constant field and lateral scaling .Write effect of the above scaling methods on the device characteristics (8)

Refer page no.125-128, A.Pucknell, Kamran Eshraghian , "BASIC VLSI Design", Third Edition, Prentice Hall of India, 2007

12.(a)(i) Draw the static CMOS logic circuit for the following expression (8)

(a) $Y=\overline{(A.B.C.D)}$

(b) $Y=\overline{D(A+BC)}$

(ii)Discuss in detail the characteristics of CMOS transmission gate?(8)

Refer page no.267-272, Jan Rabaey, Anantha Chandrakasan, B.Nikolic, "Digital Integrated Circuits: A Design Perspective", Second Edition, Prentice Hall of India, 2003.

(OR)

(b) What are the sources of power dissipation in CMOS and discuss various design techniques to reduce power dissipation in CMOS

Refer page no.186-190, N.Weste, K.Eshraghian, "Principles of CMOS VLSI Design", Second Edition, Addision Wesley 1993

13.(a) Explain the operation of master slave based edge triggered register(16)

Refer page no.634-670, Jan Rabaey, Anantha Chandrakasan, B.Nikolic, "Digital Integrated Circuits: A Design Perspective", Second Edition, Prentice Hall of India, 2003

(or)

(b)Discuss in detail various pipelining approaches to optimize sequential circuits(16)

Refer page no.325-337, Jan Rabaey, Anantha Chandrakasan, B.Nikolic, "Digital Integrated Circuits: A Design Perspective", Second Edition, Prentice Hall of India, 2003

14.(a) Design a 16 bit carry by pass and carry select adder and discuss their features?(8+8)

Refer page no.578-586, Jan Rabaey, Anantha Chandrakasan, B.Nikolic, “Digital Integrated Circuits: A Design Perspective”, Second Edition, Prentice Hall of India, 2003

(or)

(b)Design a 4 X 4 array multiplier and write down the equation for delay?

Refer page no.586-594, Jan Rabaey, Anantha Chandrakasan, B.Nikolic, “Digital Integrated Circuits: A Design Perspective”, Second Edition, Prentice Hall of India, 2003

15.(a) With neat sketch explain the CLB,IOB and programmable interconnects of an FPGA device(16)

Refer page no.184-186, Michael John Sebastian Smith, “Application-Specific Integrated Circuits”, Second Edition, Addison Wesley Professional 1997.

(or)

(b) Write brief notes on

(a)Full custom ASIC (b)Semi custom ASIC

Refer page no.19-20, Michael John Sebastian Smith, “Application-Specific Integrated Circuits”, Second Edition, Addison Wesley Professional 1997.

JEPPIAAR ENGINEERING COLLEGE

Department of ECE

Anna University Question Paper code :71738

B.E/B.TECH.DEGREE EXAMINATION, May/June 2017

Sixth Semester

EC 6601 – VLSI DESIGN

PART-A

1. What is meant chennal length modulation in NMOS transistor?

Ids is independent of Vds for a transistor in saturation, making the transistor a perfect current source. The p/n junction between the drain and body forms a depletion region with a width Ld that increases with Vdb . The depletion region effectively shortens the channel length to

$$Leff=L-Ld$$

2. Define propagation delay of a CMOS inverter

The computation of propagation delay proceeds in a fashion similar to the static inverter.For the purpose of delay analysis, each transistor is modeled as a resistor in series with an ideal switch. The value of the resistance is dependent on the power supply voltage and an equivalent large signal resistance, scaled by the ratio of device width over length, must be used. The logic is transformed into an equivalent RC network that includes the effect of internal node capacitances

3. Define Elmore Constant

A typical approach for modeling a VLSI interconnect is to use the distributed equivalent RC circuit of fig

The Elmore delay model explains the delay from input to output of the input signal, which is of a step function type. If the step response of the RC circuit is h(t), 50% point delay of the monotonic step response is the time TD that satisfies the following equation

equation

$$\int_0^{T_D} h(t)\mathrm{d}t = 0.5.$$

4. State advantages of transmission gates

Complex gates can be implemented using minimum number of transistors, which also reduces parasitic The combination of both an PMOS and NMOS in Transmission Gate arrangement avoids the problem of reduced noise margin, increase switching resistance and increased static power dissipation (caused by increased Threshold Voltage), but requires that the control and its complement be available.

Disadvantages:

1. Time-skew problems can lead to short circuits.

2. Slower speed.

3. Due to charge sharing problem, not more than 3 TG can be connected in cascade. After 3 TG a buffer circuit is required.

5. What is meant by pipelining?

Pipelining is a popular design technique often used to accelerate the operation of the datapath s in digital processors.

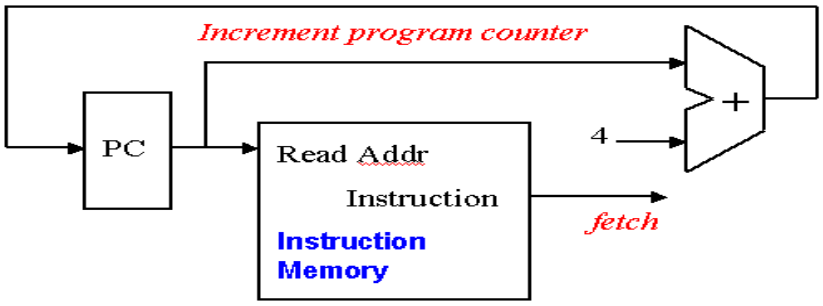
6. Compare and contrast synchronous design and asynchronous design

Synchronous Sequential Circuit	Asynchronous Sequential Circuit
It is easy to design.	It is difficult to design.
A clocked flip flop acts as memory element.	An unclocked flip flop or time delay is used as memory element.
They are slower as clock is involved.	They are comparatively faster as no clock is used here.
The states of memory element is affected only at active edge of clock, if input is changed.	The states of memory element will change any time as soon as input is changed.

- design(all memory elements in the system are simultaneously updated using a globally distributed periodic synchronization signal (that is, a global clock signal), represents an effective and popular way to enforce this ordering.
- Functionality is ensured by imposing some strict constraints on the generation of the clock signals and their distribution to the memory elements distributed over the chip
- Asynchronous designs are advantageous because computations are performed at the native speed of the logic, where block computations occur whenever data becomes available. There is no need to manage clock skew, and the design methodology leads to a very modular approach where interaction between blocks simply occur through a handshaking procedure
- It avoids the problem of clock uncertainty all-together by eliminating the need for globally-distributed clocks. A signal that can transition at arbitrary times is considered asynchronous

7. List out the components of data path

Data path components include memory (stores the current instruction), PC or program counter (stores the address of current instruction), and ALU(executes current instruction). The interconnection of these simple components to form a basic data path is illustrated in Figure Note that the register file is written to by the output of the ALU.



8. Give the application of High speed adder?

- The carry lookahead adder is a faster circuit for adding binary numbers because it reduces the propagation time of carry values.
- Doing more work does not necessarily make a circuit slower. Circuits are inherently parallel, and you only count serial operations when discussing speed.
- Designing circuits involves trade-offs among speed, complexity, size and power.

9. What is meant by CBIC?

A cell-based ASIC (CBIC) uses predesigned logic cells known as standard cells. The standard cell areas also called fle4xible block sin a CBIC are built of rows of standard cells. The ASIC designer defines only the placement of standard cells and the interconnecting a CBIC. All the mask layers of a CBIC are customized and are unique to a particular customer.

10. Name the elements in a Configuration Block?

The FPGA architecture consists of three types of configurable elements-

(i) IOBs – a perimeter of input/output blocks

(ii) CLBs- a core array of configurable logic blocks

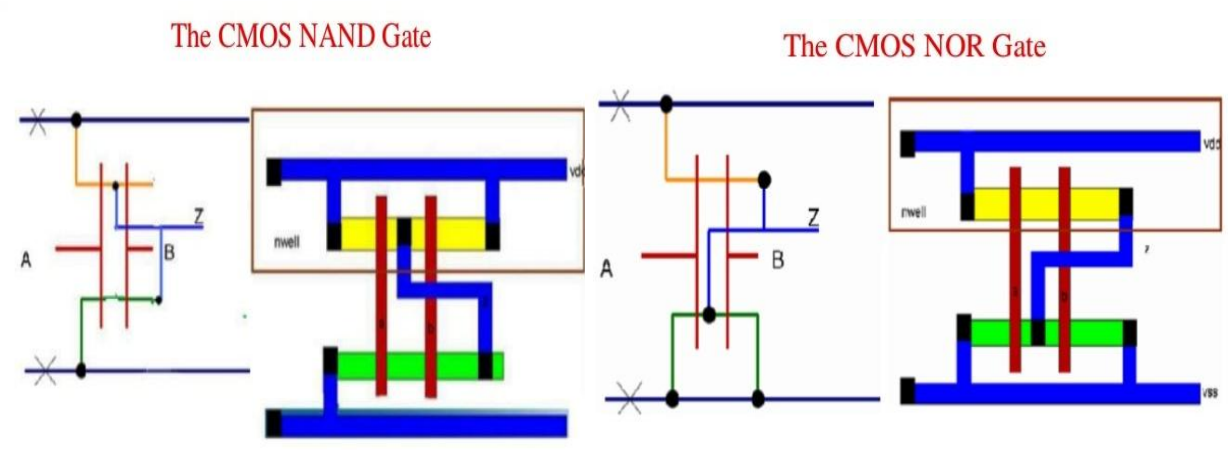
(iii) Resources for interconnection

Part –B

11.(a) (i) Draw the explain the DC and transfer characteristics of a CMOS inverter with necessary conditions for the different regions of operation (8)

Refer page no.25-34, A.Pucknell, Kamran Eshraghian , "BASIC VLSI Design", Third Edition, Prentice Hall of India, 2007

(ii) Draw the layout diagram for NAND and NOR gate. (8)



(Or)

(b) Explain the need of Scaling, scaling principle and fundamental unit of CMOS inverter.(16)

Refer page no.125-128, A.Pucknell, Kamran Eshraghian , “BASIC VLSI Design”, Third Edition, Prentice Hall of India, 2007

12.(a) (i)Explain about DCVSL logic with suitable example (10)

Refer page no.230-235, Jan Rabaey, Anantha Chandrakasan, B.Nikolic, “Digital Integrated Circuits: A Design Perspective”, Second Edition, Prentice Hall of India, 2003.

(ii) What is transmission Gate? Explain the use of transmission gate (6)

Refer page no.267-272, Jan Rabaey, Anantha Chandrakasan, B.Nikolic, “Digital Integrated Circuits: A Design Perspective”, Second Edition, Prentice Hall of India, 2003.

(Or)

(b)Explain the static and dynamic power dissipation in CMOS circuits with necessary diagrams and expressions (16)

Refer page no.186-190, N.Weste, K.Eshraghian, “Principles of CMOS VLSI Design”, Second Edition, Addision Wesley 1993

13.(a) (i) Explain the operation of True single phase clocked register (8)

Refer page no.300-319, Jan Rabaey, Anantha Chandrakasan, B.Nikolic, “Digital Integrated Circuits: A Design Perspective”, Second Edition, Prentice Hall of India, 2003

(ii) Draw and explain the operation conventional, pulsed and resettable latches (8)

Refer page no.395-398, N.Weste, K.Eshraghian, “Principles of CMOS VLSI Design”, Second Edition, Addision Wesley 1993

(Or)

(a) Explain the concept of timing issues and pipelining (16)

Refer page no.325-337, Jan Rabaey, Anantha Chandrakasan, B.Nikolic, “Digital Integrated Circuits: A Design Perspective”, Second Edition, Prentice Hall of India, 2003

14.(a) (i) Explain the concept of carry look ahead adder with neat diagram (10)

Refer page no.578-586, Jan Rabaey, Anantha Chandrakasan, B.Nikolic, "Digital Integrated Circuits: A Design Perspective", Second Edition, Prentice Hall of India, 2003

(ii) Discuss the details about speed and area trade off. (6)

Refer page no.600-619, Jan Rabaey, Anantha Chandrakasan, B.Nikolic, "Digital Integrated Circuits: A Design Perspective", Second Edition, Prentice Hall of India, 2003

(Or)

(b) Explain the concept of modified Booth multiplier with suitable example (16)

Refer page no.586-594, Jan Rabaey, Anantha Chandrakasan, B.Nikolic, "Digital Integrated Circuits: A Design Perspective", Second Edition, Prentice Hall of India, 2003

15.(a) Explain about different types of ASIC with neat diagram (16)

Refer page no.19-20, Michael John Sebastian Smith, "Application-Specific Integrated Circuits", Second Edition, Addison Wesley Professional 1997.

(Or)

(b) (i) Explain about building block architecture of FPGA (10)

Refer page no.30-31, Michael John Sebastian Smith, "Application-Specific Integrated Circuits", Second Edition, Addison Wesley Professional 1997.

(ii) Write short notes on routing procedures involved in FPGA interconnect (6)

Refer page no.184-186, Michael John Sebastian Smith, "Application-Specific Integrated Circuits", Second Edition, Addison Wesley Professional 1997.

JEPPIAAR ENGINEERING COLLEGE

Department of ECE

Anna University Question Paper code : 20421

B.E/B.TECH.DEGREE EXAMINATION, NOV/DEC 2018

Sixth Semester

EC 6601 – VLSI DESIGN

PART-A

1. 1. Why NMOS device conducts strong zero and weak one?
2. Draw the stick diagram of static CMOS 2-input NAND gate.
3. Determine the discharging time of the circuit shown in Figure-1. when switch

'A' is closed. Assume Ct and internal capacitances C: and C2 are charged initially. Let C, =C,=C, =C. , a Ra "TC, Cl. ; _t Rag ae Bl ae RZ IC2 10.

4. Realize X= B+ C and Y= (A(B+ C))using multiple output domino stages.
5. List out the advantages and limitations of 3 T DRAM over 1 T DRAM
6. List out the advantage of C^2MOS logic based register over pass-transistor logic based master-slave register

7.The circuit in Fig.2 shows a carry propagation path in an adder circuit. Let A,B.Ci are the inputs to adder circuit and g is the clock signal. Write the logic expressions for the signal X, Y to generate output carry.

8. Draw a 4-bit ripple carry adder and find its critical path delay.

9. Compare between Xilinx CLB interconnect and Alter a LAB interconnect.

10. Differentiate between full custom design and semi custom design

PART-B (5*16=80MARKS)

11.a) i) List out the goals of CMOS technology scaling. Explain How common electric field scaling is superior than constant voltage? (7)

Refer page no.25-34, A.Pucknell, Kamran Eshraghian , "BASIC VLSI Design", Third Edition, Prentice Hall of India, 2007

ii) Derive the expression to obtain the minimum delay through the chain of CMOS inverter? (6)

Refer page no.113-133, A.Pucknell, Kamran Eshraghian , “BASIC VLSI Design”, Third Edition, Prentice Hall of India, 2007

(OR)

b) (i)Explain the design techniques that are used for larger fan-in devices to reduce delay (8)

Refer page no.57-69, A.Pucknell, Kamran Eshraghian , “BASIC VLSI Design”, Third Edition, Prentice Hall of India, 2007

(ii) Draw the small signal model of device during cut-off, linear and saturation region(5)

(i) 12.a) i) Implement the equation X =(A+B)CD using complementary CMOS logic.

(1) Size the devices so that the output resistance is the same as that of i i = was inverter with an NMOS W/L = 4 and PMOS

(2) What are the input patterns that give the worst case tp,, and . PHL tery . Consider the éffect of the capacitances at the internal nodes. .

(8)

Refer page no.230-240, Jan Rabaey, Anantha Chandrakasan, B.Nikolic, “Digital Integrated Circuits: A Design Perspective”, Second Edition, Prentice Hall of India, 2003.

ii) If P(A=1)=0.5, P(B=1)=0.2, P(C=1)=03,P(D=1)=1, determine the power dissipation in the logic gate. Assume Vpp = 2.5V, C,,, =30 fF and Fy, = 250 MHz. (7)

(ii) List out the limitations of pass transistor logic. Explain any two techniques used to overcome the drawback of pass transistor logic . (8)

Refer page no.267-272, Jan Rabaey, Anantha Chandrakasan, B.Nikolic, “Digital Integrated Circuits: A Design Perspective”, Second Edition, Prentice Hall of India, 2003.

(OR)

b) i) Explain in detail the signal integrity issues in dynamic logic design. propose any two solutions to overcome it. (7) (ii) (1) Determine the truth table for the circuit shown Figure-3.

What logic function does it implement? (4)

If the PMOS were removed, would the circuit still function correctly? Does the PMOS transistor serve any useful purpose? (2)

(8)

Refer page no.230-235, Jan Rabaey, Anantha Chandrakasan, B.Nikolic, "Digital Integrated Circuits: A Design Perspective", Second Edition, Prentice Hall of India, 2003.

13. a) ()Identify the type of register for the circuit shown in figure 4 and express set up time, hold time and propagation delay of register in terms of the propagation delay of inverters and transmission gates.input_T7>0-T = = -? oo (16)

(ii)Implement the register of question 13(i) using C2MOS logic and explain how 0-0 and 1-1 overlap of clock signals are eliminated

Refer page no.300-319, Jan Rabaey, Anantha Chandrakasan, B.Nikolic, "Digital Integrated Circuits: A Design Perspective", Second Edition, Prentice Hall of India, 2003

(OR)

(b) b) Construct 6T based SRAM cell. Explain its read and write operations. What is the importance of Cell ratio and Pull up ratio in

6T SRAM cell? ; (8)

Gi) Analyze the impact of spatial variations of clock signal on edge-

triggered sequential logic circuits. ' (5)

Refer page no.325-337, Jan Rabaey, Anantha Chandrakasan, B.Nikolic, "Digital Integrated Circuits: A Design Perspective", Second Edition, Prentice Hall of India, 2003

14.a) (i)Design an 8-bit Brent-Kung Adder (5)

Refer page no.561-568, Jan Rabaey, Anantha Chandrakasan, B.Nikolic, "Digital Integrated Circuits: A Design Perspective", Second Edition, Prentice Hall of India, 2003

(OR)

(ii) b) Construct 4 x 4 Array type multiplier and find its critical path

delay.(8)

Refer page no.586-594, Jan Rabaey, Anantha Chandrakasan, B.Nikolic, “Digital Integrated Circuits: A Design Perspective”, Second Edition, Prentice Hall of India, 2003

(iii) Design 4-input and 4-output barrel shift adder using NMOS logic.(5)

15. a) Explain CLB of Xilinx 4000 architecture (13)

Refer page no.19-20, Michael John Sebastian Smith, “Application-Specific Integrated Circuits”, Second Edition, Addison Wesley Professional 1997.

(OR)

(iii) b) Realize the function, F = A.B+(B'C)+Dusing ACTEL (ACT-1)

FPGA. (5)

(iv) Draw the flow chart of digital circuit design techniques. (4)

(v) Differentiate between Hard Macro and Soft Macro. . (4)

Refer page no.30-31, Michael John Sebastian Smith, “Application-Specific Integrated Circuits”, Second Edition, Addison Wesley Professional 1997.

PART C — (1 x 15 = 15 marks)

16.a) Derive an expression to show the drain current of MOS for various

“operating region. Explain one non-ideality for each operating region that

changes the drain current. (15)

(OR)

16.b)Explain in detail the CMOS manufacturing process. (15)