JEPPIAAR
ENGINEERING COLLEGE

DEPARTMENT OF ELECTRONICS AND COMMUNICATION ENGINEERING

EC3462 – LINEAR INTEGRATED CIRCUITS LAB

LAB MANUAL

II - YEAR IV SEM ECE

ACADEMIC YEAR:2021-2025

NAME : _____

ROLL NO. : _____

REG NO. : _____

YEAR : _____

SECTION : _____

JEPPIAAR ENGINEERING COLLEGE		
Vision of the Institute	To build Jeppiaar Engineering College as an institution of academic excellence in technological and management education to become a world class University	
Mission of the Institute	**M1**	To excel in teaching and learning, research and innovation by promoting the principles of scientific analysis and creative thinking
	M2	To participate in the production, development and dissemination of knowledge and interact with national and international communities.
	M3	To equip students with values, ethics and life skills needed to enrich their lives and enable them to meaningfully contribute to the progress of society
	M4	To prepare students for higher studies and lifelong learning, enrich them with the practical and entrepreneurial skills necessary to excel as future professionals and contribute to Nation's economy
DEPARTMENT: ELECTRONICS AND COMMUNICATION ENGINEERING		
Vision of the Department	To become a centre of excellence to provide quality education and produce creative engineers in the field of Electronics and Communication Engineering to excel at international level.	
Mission of the Department	**M1**	Inculcate creative thinking and zeal for research to excel in teaching-learning process
	M2	Create and disseminate technical knowledge in collaboration with industries
	M3	Provide ethical and value based education by promoting activities for the betterment of the society
	M4	Encourage higher studies, employability skills, entrepreneurship and research to produce efficient professionals thereby adding value to the nation's economy

PROGRAM OUTCOMES (PO)	**PO 1**	**Engineering knowledge**: **Apply** the knowledge of mathematics, science, engineering fundamentals, and an engineering specialization to the solution of complex engineering problems.
	PO 2	**Problem analysis**: **Identify, formulate, review** research literature, and **analyze** complex engineering problems reaching substantiated conclusions using first principles of mathematics, natural sciences, and engineering sciences.
	PO 3	**Design/development of solutions**: **Design solutions** for complex engineering problems and **design** system components or processes that meet the specified needs with appropriate consideration for the public health and safety, and the cultural, societal, and environmental considerations
	PO 4	**Conduct investigations of complex problems**: **Use** research-based knowledge and research methods including **design** of experiments, **analysis** and **interpretation** of data, and **synthesis** of the information to provide valid conclusions.
	PO 5	**Modern tool usage**: **Create**, **select**, and **apply** appropriate techniques, resources, and modern engineering and IT tools including prediction and modeling to complex engineering activities with an understanding of the limitations.
	PO 6	**The engineer and society**: **Apply** reasoning informed by the contextual knowledge to assess societal, health, safety, legal and cultural issues and the consequent responsibilities relevant to the professional engineering practice.
	PO 7	**Environment and sustainability**: **Understand** the impact of the professional engineering solutions in societal and environmental contexts, and **demonstrate** the knowledge of, and need for sustainable development.
	PO 8	**Ethics**: **Apply** ethical principles and commit to professional ethics and responsibilities and norms of the engineering practice.
	PO 9	**Individual and team work**: **Function effectively** as an individual, and as a member or leader in diverse teams, and in multidisciplinary settings.
	PO 10	**Communication**: **Communicate effectively** on complex engineering activities with the engineering community and with society at large, such as, being able **to comprehend** and **write** effective reports and **design** documentation, **make** effective presentations, and **give** and **receive** clear instructions.
	PO 11	**Project management and finance**: **Demonstrate** knowledge and understanding of the engineering and management principles and **apply** these to one's own work, as a member and leader in a team, to **manage** projects and in multidisciplinary environments.
	PO 12	**Life-long learning**: **Recognize** the need for, and have the preparation and ability to **engage** in independent and life-long learning in the broadest context of technological change.

PROGRAM EDUCATIONAL OBJECTIVES (PEOS)	**PEO I**	Produce technically competent graduates with a solid foundation in the field of Electronics and Communication Engineering with the ability to analyze, design, develop, and implement electronic systems.
	PEO II	Motivate the students for choosing the successful career choices in both public and private sectors by imparting professional development activities.
	PEO III	Inculcate the ethical values, effective communication skills and develop the ability to integrate engineering skills to broader social needs to the students.
	PEO IV	Impart professional competence, desire for lifelong learning and leadership skills in the field of Electronics and Communication Engineering.
PROGRAM SPECIFIC OUTCOMES (PSOs)	**PSO 1**	Design, develop and analyze electronic systems through application of relevant electronics, mathematics and engineering principles.
	PSO 2	Design, develop and analyze communication systems through application of fundamentals from communication principles, signal processing, and RF System Design & Electromagnetics.
	PSO 3	Adapt to emerging electronics and communication technologies and develop innovative solutions for existing and newer problems.

INSTRUCTIONS

The students are requested to

- **Use this lab manual as observation notebook.**
- **Bring the lab manual compulsorily for all lab classes.**
- **Get the verified signature from the staff in charge, once the experiment is completed and output seal should be endorsed and get the staff signature on that lab class itself.**
- **Get the record correction for the experiment, before entering the next lab class otherwise entry will be denied.**
- **"Get completed signature in the index page of the record from the staff-in charge" after the completion of all experiments**
- **Before entering the university practical examinations, the students must get the bonafide signature in the observation and record notebook.**

INDEX

S.No.	Date	Name of the Experiment	Page No.	Date of submission	Marks	Sign.

S.No	Date	Name of the Experiment	Page No.	Date of submission	Marks	Sign.

JEPPIAAR ENGINEERING COLLEGE

DEPARTMENT OF ELECTRONICS AND COMMUNICATIONS ENGINEERING

EC 3462– LINEAR INTEGRATED CIRCUITS LAB

SYLLABUS

LIST OF EXPERIMENTS:

DESIGN AND ANALYSIS OF THE FOLLOWING CIRCUITS

1. Series and Shunt feedback amplifiers-Frequency response, Input and output impedance
2. RC Phase shift oscillator and Wien Bridge Oscillator
3. Hartley Oscillator and Colpitts Oscillator
4. RC Integrator and Differentiator circuits using Op-Amp
5. Clippers and Clampers
6. Instrumentation amplifier
7. Active low-pass, High pass & Band pass filters
8. PLL Characteristics and its use as frequency multiplier, clock synchronization
9. R-2R ladder type D-A converter using Op-Amp

SIMULATION USING SPICE (Using Transistor):

1. Tuned Collector Oscillator
2. Twin -T Oscillator / Wein Bridge Oscillator
3. Double and Stagger tuned Amplifiers
4. Bistable Multivibrator
5. Schmitt Trigger circuit with Predictable hysteresis
6. Analysis of power amplifier

COURSE OBJECTIVES:

- To gain hands on experience in designing electronic circuits
- To learn simulation software used in circuit design 85
- To learn the fundamental principles of amplifier circuits
- To differentiate feedback amplifiers and oscillators.
- To differentiate the operation of various multivibrators

COURSE OUTCOMES:

At the end of the course the students will be able to

- Analyze various types of feedback amplifiers
- Design oscillators, tuned amplifiers, wave-shaping circuits and multivibrators
- Design and simulate feedback amplifiers,oscillators, tuned amplifiers, waveshaping circuits and multivibrators, filters using SPICE Tool.
- Design amplifiers, oscillators, D-A converters using operational amplifiers.
- Design filters using op-amp and perform an experiment on frequency response

LIST OF EXPERIMENS:

CYCLE I:

1. Series and Shunt feedback amplifiers
2. RC Phase shift oscillator
3. Wien Bridge Oscillator
4. Hartley Oscillator
5. Colpitts Oscillator

CYCLE II:

6. RC Integrator and Differentiator circuits using Op-Amp
7. Clippers and Clampers
8. Instrumentation amplifier
9. Active low-pass using Op-Amp
10. Active High pass using Op-Amp
11. Active Band pass filters using Op-Amp
12. PLL Characteristics and its use as frequency multiplier, clock synchronization
13. R-2R ladder type D-A converter using Op-Amp

CYCLE III: SIMULATION USING SPICE (Using Transistor):

14. Tuned Collector Oscillator
15. Twin -T Oscillator / Wein Bridge Oscillator
16. Double and Stagger tuned Amplifiers
17. Bistable Multivibrator
18. Schmitt Trigger circuit with Predictable hysteresis
19. Analysis of power amplifier

Ex. No:	SERIES AND SHUNT FEEDBACK AMPLIFIER
DATE:	

AIM:

To design and test the current series and voltage shunt Feedback Amplifier and to compare its frequency response with and without feedback.

APPARATUS REQUIRED:

S.NO	COMPONENTS	RANGE	QTY
1	Transistor	BC107	
2	Resistors	10kΩ, 47kΩ, 60kΩ, 1.2kΩ, 1kΩ, 4.7kΩ	2 1 2
3	Capacitor	10µf,5µf, 47µf,	**2**
4	CRO	(0-30)MHz	1
5	RPS	(0-30)V	1
6	Function generator	-	1
7	Breadboard	-	1
8	Connecting wires	--	-

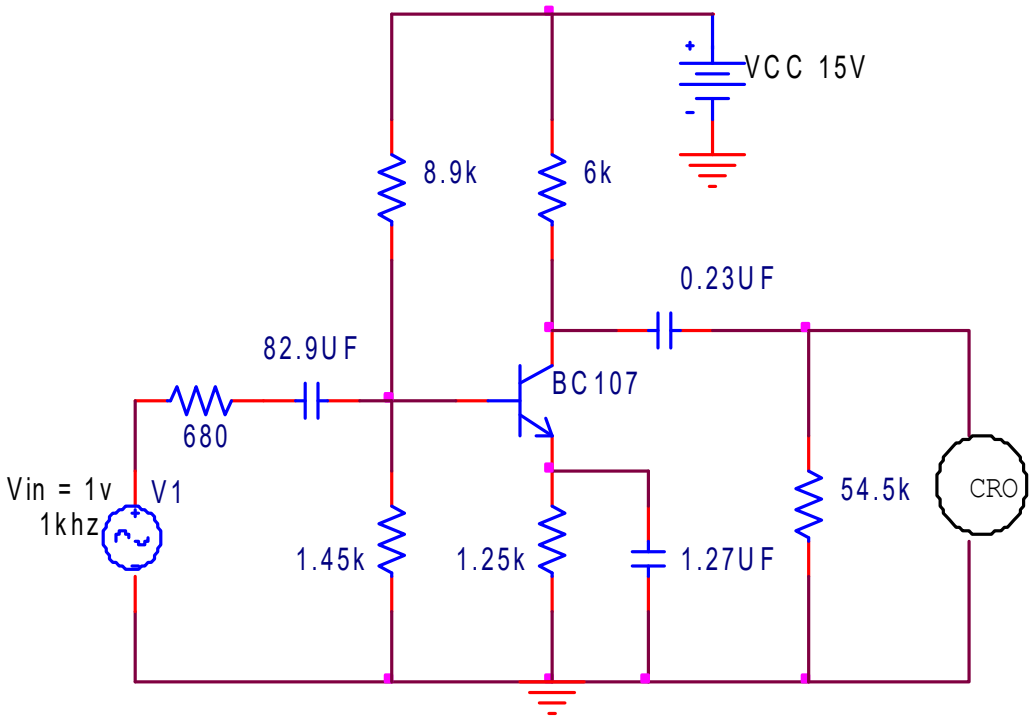
THEORY:

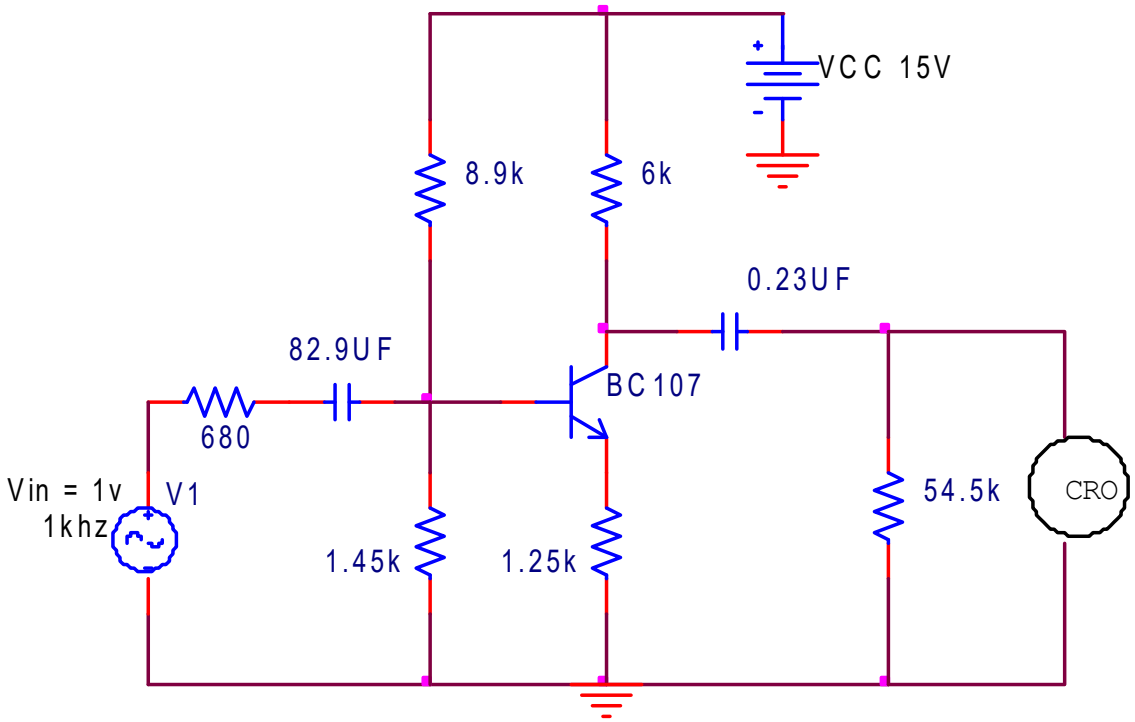
An amplifier whose function fraction of output is fed back to the input is called feedback amplifier. Depending upon whether the input is in phase or out of phase with the feedback signal, they are classified in to positive feedback and negative feedback. If the feedback signal is in phase with the input, then the wave will have positive gain. Then the amplifier is said to have a positive feedback.If the feedback signal is out of phase with the input, then the wave will have a negative gain. The amplifier is said to have a negative feedback. The values of voltage gain and bandwidth without feedback.

PROCEDURE:

The connections are made as shown in the circuit. The amplifier is checked for its correct operation .Set the input voltage to a fixed value. Keeping the input voltage Vary the input frequency from 0Hz to 1MHz and note down the corresponding output voltage. plot the graph : gain (dB) vs frequency .Find the input and output impedances. Calculate the bandwidth from the graph. Remove RE and follow the same procedure.

CURRENT SERIES:
CIRCUIT DIAGRAM:





Observation:

CURRENT SERIES:

With Out Feedback **Vin = ---------- Volts**

S.No	Frequency	O/P voltage Vo	Gain Av=20 log Vo/Vi

With Feedback **Vin = ---------- Volts**

S.No	Frequency	O/P voltage Vo	Gain Av=20 log Vo/Vi

DESIGN SPECIFICATION:

Vcc=12v Ic =1mA Av_F =100 Vc_E = 6v f=50H_z

Selection of R_E & R_C:

$$V_{CC} = I_C(R_C + R_E) + V_{CE}$$

$$R_C + R_E = \frac{V_{CC} - V_{CE}}{I_C}$$

$$= \frac{12-5}{2\times10^{-3}} = 3.5K\Omega$$

$$A_{VF} = -R_C / R_E$$

$$\therefore R_C = -A_{VF} R_E$$

$$= -5R_E$$

$$-5R_E + R_E = 3.5K\Omega$$

$$-4R_E = 3.5K\Omega$$

$$\therefore R_E = 875\Omega$$

Choose $R_E = 1K\Omega$

$$R_C = -5 \times 1 \times 10^3 = 5K\Omega$$

Choose $R_C = 4.7K\Omega$

Choose $C_E = 47\mu F$

$$X_{CC} \leq 0.1R_C$$

$$C_C \geq \frac{1}{2\pi F\, R_C \times 0.1}$$

$$C_C \geq \frac{1}{2\pi\times50\times4.7\times10^3\times0.1}$$

$$C_C \geq 6.77\mu F$$

Choose $C_C = 10\mu F$

Selection of R_1&R_2:

$$V_{R2} = V_{BE} + V_{RE} = V_{BE} + I_C R_E$$

$$= 0.6 + 2\times10^{-3}\times1\times10^3$$

$$= 2.6V$$

$$V_{R1} = V_{CC} - V_{R2}$$

$$= 12 - 2.6 = 9.4V$$

$$\frac{V_{R1}}{V_{R2}} = R1/R2 \quad = 9.4/2.6 = 3.615$$

Choose $R_2 = 10K\Omega$

$$R_1 = 3.615 \times 10 \times 10^3$$

$$= 36.15K\Omega$$

Choose $R_1 = 47K\Omega$

Selection of Cc & C_E

$$X_{CC} \leq 0.1R_E$$

$$C_E \geq \frac{1}{2\pi F\, R_E \times 0.1}$$

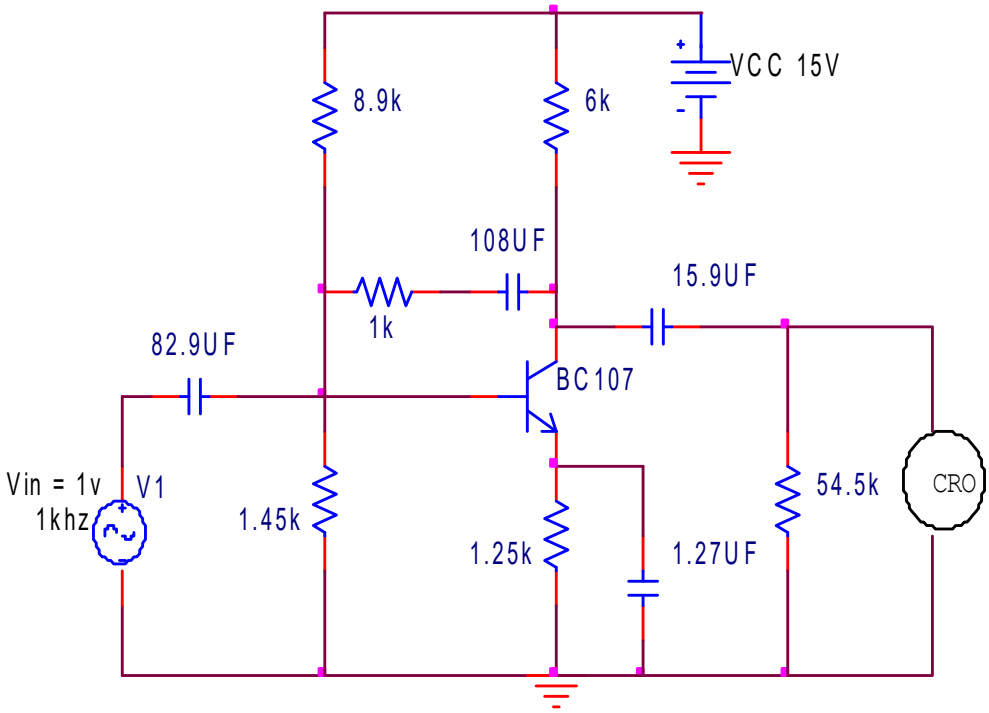
$$C_E \geq \frac{1}{2\pi\times50\times1\times10^3\times0.1}$$

$$C_E \geq 31.83\mu F$$

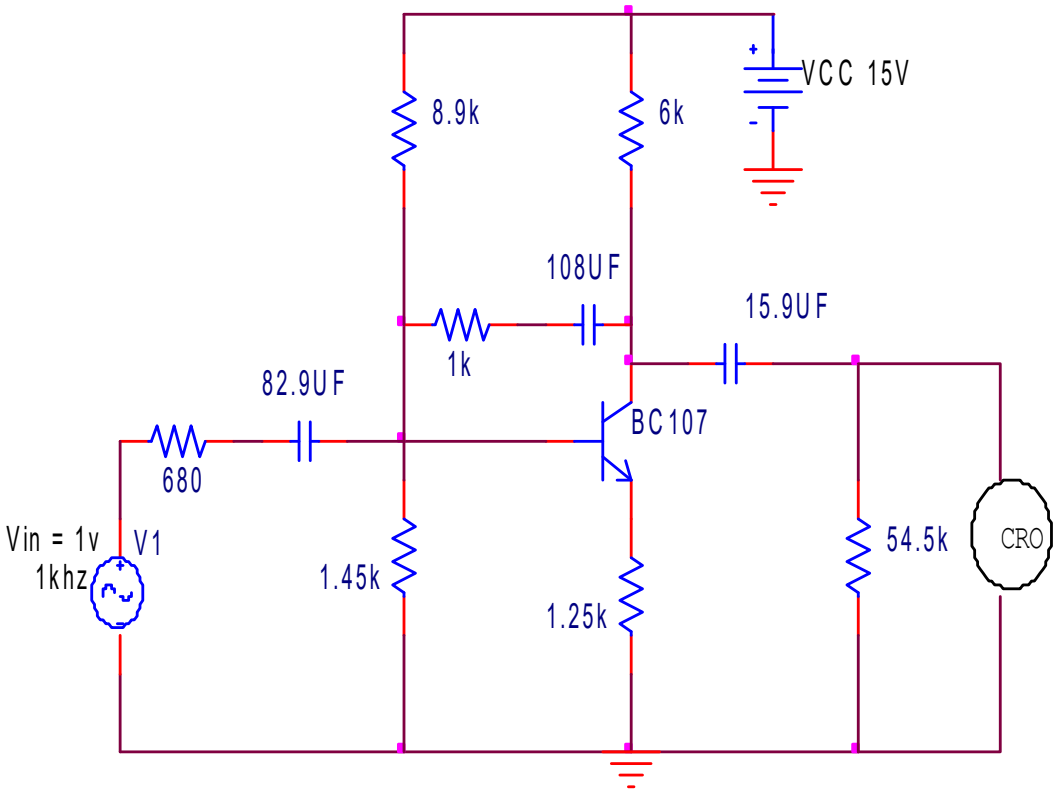
VOLTAGE SHUNT:

CIRCUIT DIAGRAM:

WITHOUT FEEDBACK



WITH FEEDBACK



Observation:

CURRENT SERIES:

With Out Feedback **Vin = ---------- Volts**

S.No	Frequency	O/P voltage Vo	Gain Av=20 log Vo/Vi

With Feedback **Vin = ---------- Volts**

S.No	Frequency	O/P voltage Vo	Gain Av=20 log Vo/Vi

DESIGN CALCULATION:

Design specification:

V_{CC}=12v I_C=1mA A_{VF}=100 V_{CE} = 6v

Selection of R_E :

$V_{RE} = 0.1 . V_{CC} = 0.1 \times 12 = 1.2v$

$V_{RE} = I_C R_E$

$$R_E = \frac{V_{RE}}{I_C} = \frac{1.2}{1 \times 10^{-3}}$$

$R_E = 1.2k\Omega$

Selection of R_C :

$V_{CC} = I_E R_E + V_{CE} + I_C R_C$

$$R_C = \frac{V_{CC} I_E R_E I_C - V_{CE}}{}$$

$$= \frac{12-1\times10^{-3}\times1.2\times10^{3}-}{61\times10^{-3}}$$

$R_C = 4.8k\Omega$

Selection of R_1&R2:

$V_{R2} = V_{BE} + V_{RE}$

$= 0.6 + 1.2 = 1.8V$

$V_{R1} = V_{CC} - V_{R1}$

$= 12 \_ 1.8 = 10.2V$

$$\frac{V_{R1}}{V_{R2}} = {}^{R1}/_{R2} = {}^{10.2}/_{1.8}$$

$=5.67$

Choose $R_2 = 10K\Omega$

$R_1 = 5.6 \times 10 \times 10^3$

$= 56.7K\Omega$

Choose $R_1 = 47K\Omega$

Selection of R_F :

$A_{VF} = -R_F / R_S$

$-R_F = -A_{VF} R_S$

Choose $R_S = 600\Omega$

$-R_F = -100 \times 600 = 60K\Omega$

Choose $R_F = 60K\Omega$

Selection of C_E :

$X_{CE} \leq 0.1 R_E$

$$\frac{1}{2\pi F C_E} \leq 0.1 R_E \rightarrow C_E \geq \frac{1}{2\pi F R_E \times 0.1}$$

$$C_E \geq \frac{1}{2\pi \times 50 \times 1.2 \times 10^3 \times 0.1}$$

$C_E \geq 26.52\mu F$

Choose $C_E = 47\mu F$

Selection of C_C:

$X_{CC} \leq 0.1 R_C$

$$\frac{1}{2\pi F C_C} \leq 0.1 R_C$$

$$C_C \geq \frac{1}{2\pi F R_C \times 0.1}$$

$$C_C \geq \frac{1}{2\pi \times 50 \times 4.7 \times 10^3 \times 0.1}$$

$C_C \geq 6.77\mu F$

Choose $C_C = 5\mu F$

RESULT:

Thus the current series and voltage shunt feedback amplifier is constructed and frequency response is plotted.

VALUES	CURRENT SERIES	VOLTAGE SHUNT
Without Feedback		
With Feedback		

EX. NO :	

DATE:	**RC PHASE SHIFT OSCILLATOR**

AIM:

To design and construct the transistor Phase shift oscillator.

APPARATUS REQUIRED:

S.NO	COMPONENTS	RANGE	QTY
1	Transistor	BC107	1
2	Resistor	2kΩ, 1kΩ, 25.17kΩ,10kΩ 4.7KΩ	1each 3
3	Capacitor	5µf, 100 µf0.02µf	1 3
4	CRO	(0-30)MHz	1
5	RPS	(0-30) V	1
6	Connecting wires	-	-
7	Breadboard	-	1

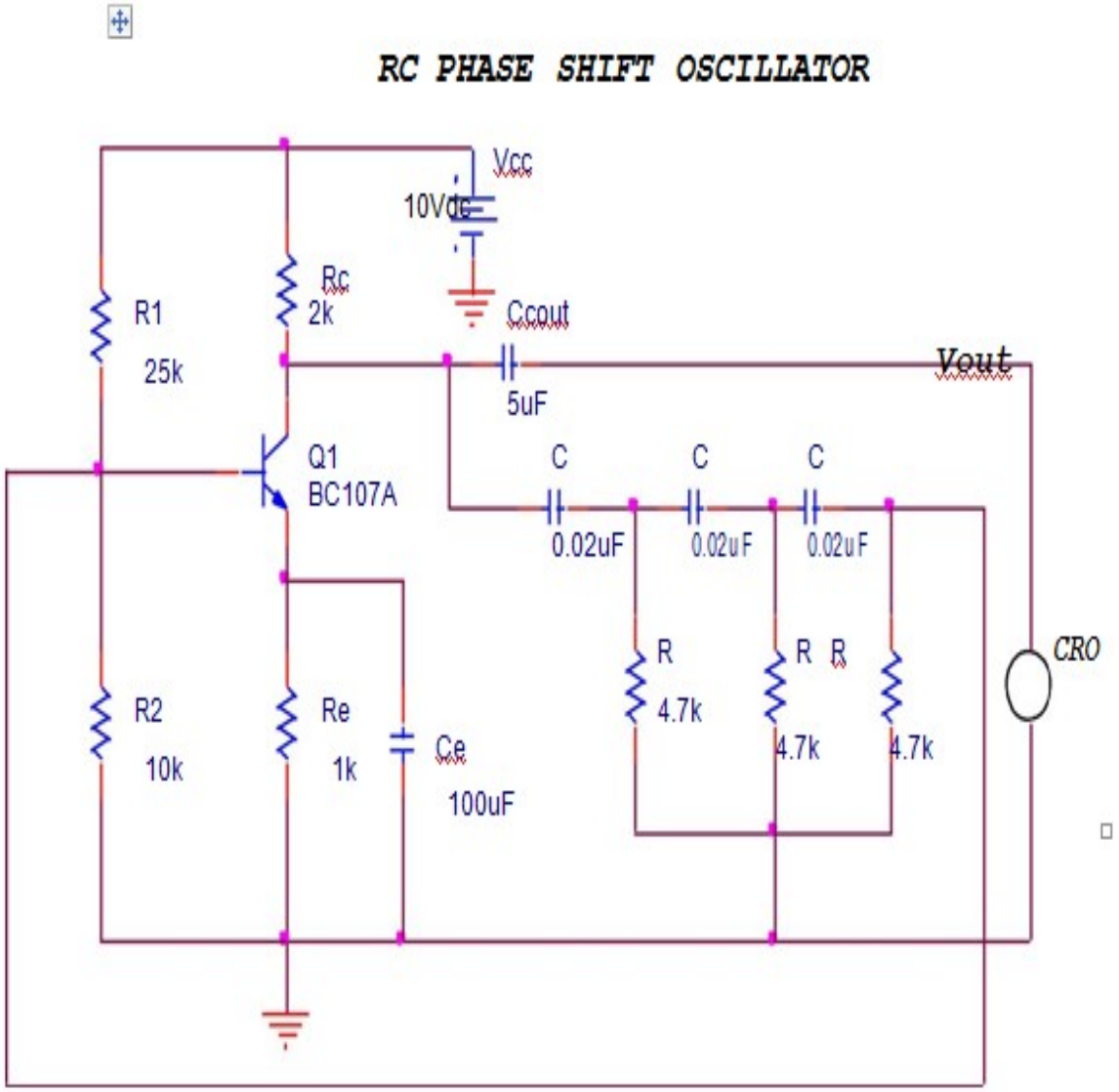
THEORY:

The Transistor Phase Shift Oscillator produces a sine wave of desired designed frequency. The RC combination will give a 60 phase shift totally three combination will give a 180 phase shift. . The BC107 is in the common emitter configuration. Therefore that will give a 180 phase shift totally a 360 phase shift output is produced. The capacitor value is designed in order to get the desired output frequency. Initially the C and R are connected as a feedback with respect to input and output and this will maintain constant sine wave output. CRO is connected at the output

PROCEDURE:

1. The circuit is constructed as per the given circuit diagram.
2. 7Switch on the power supply and observe the output on the CRO(sine wave)
3. Note down the practical frequency and compare it with the theoretical frequency.

CIRCUIT DIAGRAM:



OBSERVATION:PRACTICAL:-

Amplitude (V)	Time period(ms)	Frequency(H_Z)

THEORETICAL:-

Frequency = $1/2\pi RC\sqrt{6}$ = 1 KHZ

DESIGN SPECIFICATION:

V_{CC}=10v I_C =2mA

H_{fe}= 2000 A_V = 100

A_{VF} =100 V_{CE} = 4

V_{BE} = 0.7V

Selection of R_C:

$$= \frac{H_{fe} R_C}{H_{ie}}$$

$$R_c = A_V H_{ie} =$$

$$\frac{100 \times 2000}{100}$$

$$= 2k\Omega$$

Selection of R_E

$V_{CC} = I_E R_E + V_{CE} + I_C R_C$ $R_E =$

$$\frac{V_{CC} - I_C R_C - V_{CE}}{I_C}$$

$$= \frac{10 - 4 - 2\times10^{-3}\times2\times10^{3}}{2\times10^{-3}}$$

$R_E = 1k\Omega$

$=$

R_E $1K\Omega$

Selection of R_1&R2:

$$V_{R2} = V_{BE} + V_{RE} = V_{BE} + I_C R_E$$

$$= 0.7 + 2 \times 10^{-3} \times 1 \times 10^{3}$$

$$= 2.7V$$

$$V_{R1} = V_{CC} - V_{R2}$$

$$= 10 - 2.7 = 7.3V$$

$$\frac{V_{R1}}{V_{R2}} = {}^{R1}/_{R2} = {}^{7.3}/_{2.7} = 2.7037$$

Choose $R_2 = 10K\Omega$

$$R_1 = 2.7037 \times 10 \times 10^{3}$$

$$= 27K\Omega$$

Choose $R_1 = 25K\Omega$

Selection of C_E :

$$X_{CE} \leq 0.1R_E$$

$$\frac{1}{2\pi F\, C_E} \leq 0.1\, R_E \longrightarrow C_E \geq \frac{1}{2\pi F\, R_E \times 0.1}$$

$$C_E \geq \frac{1}{2\pi \times 50 \times 1000 \times 0.1}$$

$$C_E \geq 31.8\mu F$$

Choose $C_E = 100\mu F$

Selection of C_C:

$$X_{CC} \leq 0.1R_C$$

$$\frac{1}{2\pi F\, C_C} \leq 0.1\, R_C$$

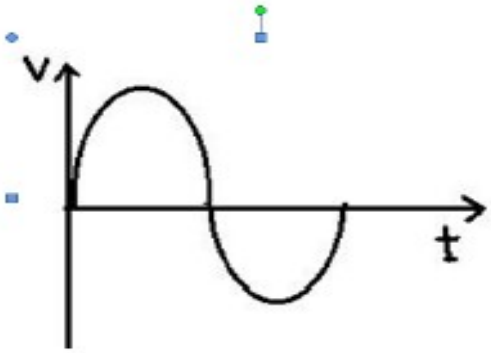
$$C_C \geq \frac{1}{2\pi F\, R_C \times 0.1}$$

$$C_C \geq \frac{1}{2\pi \times 50 \times 2000 \times 0.1}$$

$$C_C \geq 15.9\mu F$$

Choose $C_C = 5\mu F$

MODEL GRAPH:



RESULT:

Thus the RC Phase Shift Oscillator is designed and the output is verified

Theoretical frequency =

Practical frequency =

EX. NO :	

DATE:	Wien – Bridge Oscillator

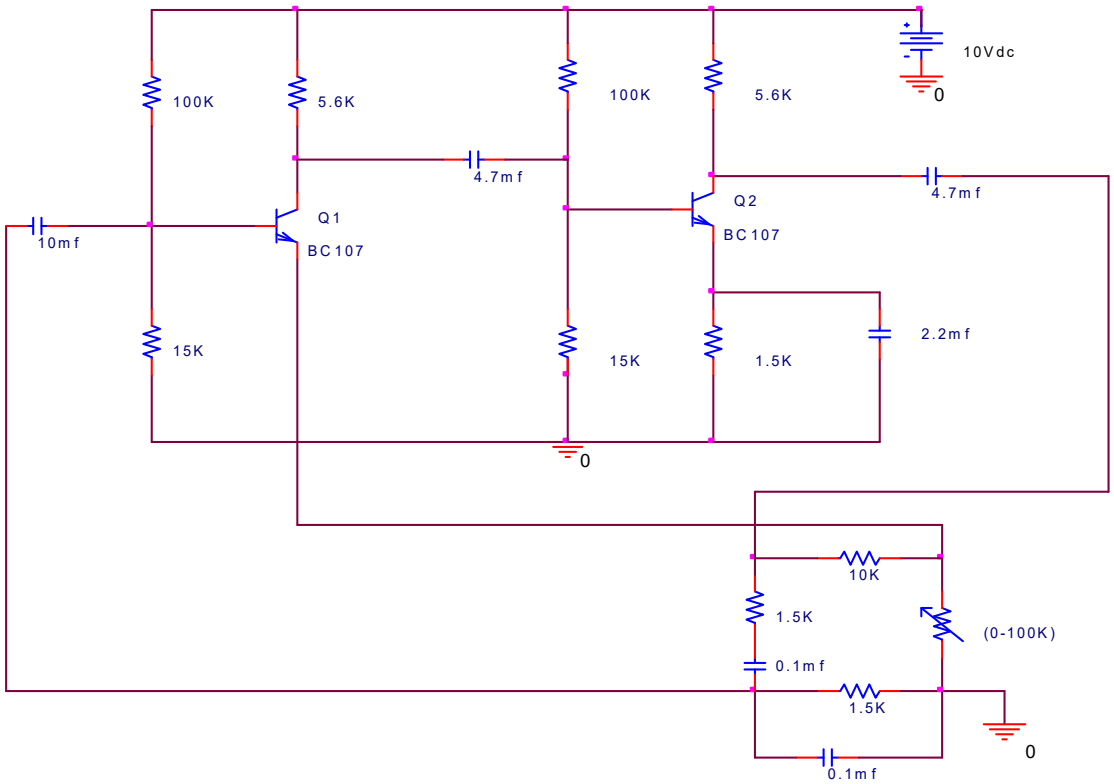
AIM:

To Design and construct a Wien – Bridge Oscillator for a given cut-off frequency.

APPARATUS REQUIRED:

S.NO	COMPONENTS	RANGE	QTY
1	Transistor	BC 107	1
2	Resistor	10kΩ, 2.7kΩ, 47kΩ , 4.7kΩ, 680Ω	2each
3	Capacitor	47 µf, 0.01 µf,	1,2
4	CRO	(0-30)MHz	1
5	RPS	(0-30) V	1
6	Breadboard	-	1
7	Connecting wires	-	-

CIRCUIT DIAGRAM:



DESIGN SPECIFICATION:

V_{CC}=12v I_C =2mA A_{VF} =100 V_{CE} = 50% *of* V_{CC} =6V
V_{RE}=10% of V_{CC} =1.2V V_{RC} =40% of V_{CC} = 4.8V
h_{fe} = 100 F = 1KH_Z

Selection of R_C

$$V_{RC} = I_C R_C$$

$$R_C = \frac{V_{RC}}{I_C} = \frac{4.8}{2\times10^{-3}}$$

$$R_C = 2.4k\Omega$$

Selection of R_E :

$$V_{RE} = I_E R_E$$

$$R_E = \frac{V_{RE}}{I_C} = \frac{1.2}{2\times10^{-3}}$$

$$R_E = 600\Omega$$

Choose $R_E = 680\Omega$

Selection of R1&R2:

$$V_{R2} = V_{BE+} V_{RE}$$
$$= 0.7 + 1.2$$
$$= 1.9V$$
$$V_{R1} = V_{CC} - V_{R2}$$
$$= 12 - 1.9 = 10.1V$$
$$\frac{V_{R1}}{V_{R2}} = R1/_{R2} = 10.1/_{1.9} = 5.315$$

Choose $R_2 = 10K\Omega$

$$R_1 = 5.315\times10\times10^3$$
$$= 47K\Omega$$

Choose $R_1 = 47K\Omega$

Selection of C_C :

$$F = \frac{1}{2\pi C_C (R_1 \| R_2 \| h_{ie} R_e)}$$

$$C_C \geq = \frac{1}{2\pi\times1000\times[47k\|10k\|68k]}$$

$$C_C \geq 21.958\mu F$$

THEORY:

In Wien bridge oscillator, Wien bridge circuit is connected between the amplifier input terminals and output terminals. The bridge has a series RC network in one arm and parallel network in the adjoining arm. In the remaining 2 arms of the bridge resistors R1and Rf are connected . To maintain oscillations total phase shift around the circuit must be zero and loop

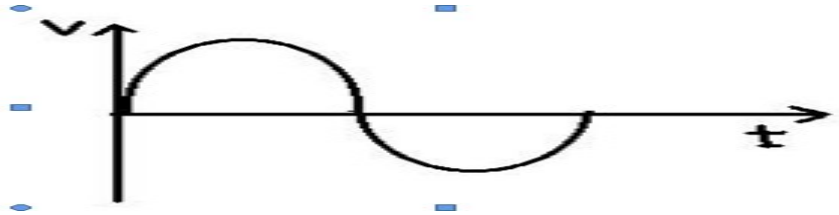
gain unity. First condition occurs only when the bridge is balanced . Assuming that the resistors and capacitors are equal in value, the resonant frequency of balanced bridge is given by

$$Fo = 0.159\ RC$$

PROCEDURE:

1. The circuit is constructed as per the given circuit diagram.
2. Switch on the power supply and observe the output on the CRO
3. (sine wave)
4. Note down the practical frequency and compare it with the theoretical frequency.

MODEL GRAPH:



OBSERVATION:

AMPLITUDE (V)	TIME (ms)	FREQUENCY(H_Z)

RESULT:

Thus the Wien bridge oscillator is designed and the output is drawn.

Ex. No :	HARTLEY OSCILLATOR
Date:	

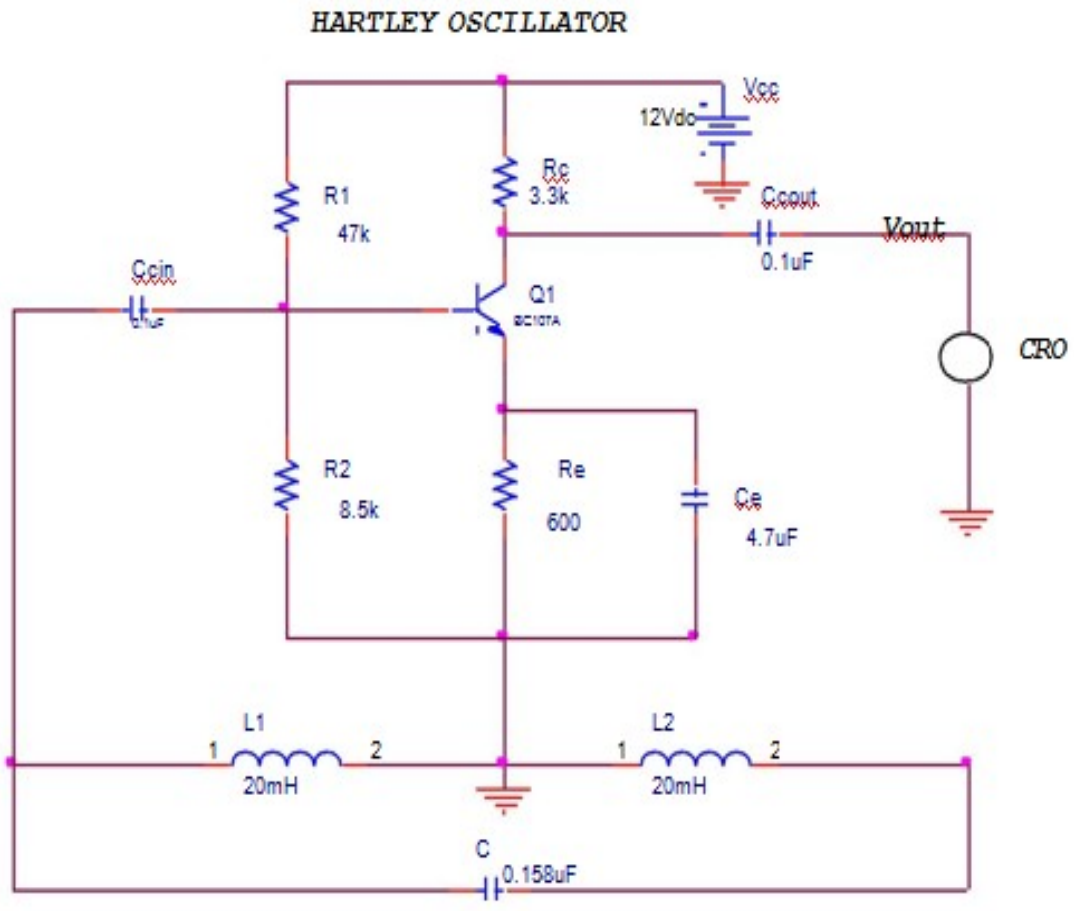
AIM:

To Design and construct the given Oscillator at the given operating frequency.

APPARATUS REQUIRED:

S.NO	COMPONENTS	RANGE	QTY
1	Transistor	BC 107	1
2	Resistor	8.5kΩ,3.3kΩ, 600Ω, 47kΩ	Each one
3	Capacitor	4.7µf, 0.1 µf	Each one
4	Inductor	20mH	2
5	CRO	(0-30)MHz	1
6	RPS	(0-30) V	1
7	Function Generator	(0 – 1)MHZ	1

CIRCUIT DIAGRAM:



DESIGN SPECIFICATION

Vcc=12v Ic =2mA V_{CE} =5V S =12| 5v h_{fe} = 125
F = 2KH_Z

Selection of R_C & R_E:

$$V_{CC} = I_C(R_C + R_E) + V_{CE}$$

$$R_C + R_E = \frac{V_{CC} - V_{CE}}{I_C}$$

$$V_{RE} = 0.1V_{CC} =$$

$0.1 \times 12 = 1.2V$

$$V_{RE} = I_E R_E$$

$$R_E = \frac{V_{RE}}{I_C}$$

$$= \frac{1.2}{2\times10^{-3}} = 600\Omega$$

$$R_C = (R_C + R_E) - R_E$$

Selection of R_1 & R_2:

$$S = \frac{1+\beta}{1+\beta\left(\frac{Re}{Re+Rb}\right)}$$

$$12 = \frac{1+125}{1+125\left(\frac{600}{600+Rb}\right)}$$

$$R_B = 7.29K\Omega$$

$$V_{R2} = V_{BE} + I_E R_E$$

$=0.6\times2\times10\_3\times600$

$= 1.8V$

$$R_2 = \frac{Vcc}{R1+R2} R2 \Longrightarrow \frac{VR2}{Vcc} = \frac{R2}{R1+R2}$$

$$\frac{R2}{R1+R2} = \frac{VR2}{Vcc} = \frac{1\_8}{12} = 0.15$$

$$R_B = \frac{R1R2}{R1+R2} = 7.29K\Omega$$

$0.15R_1 = 7.29K\Omega$

$R_1 = 48.6\ K\Omega$ Choose $R_1 = 47K\Omega$

$$\frac{R2}{R1+R2} = 0.15$$

$R_2 = 0.15\ R_2 + 0.15\ R_1$

$0.85\ R_2 = 0.15\ R_1$

$R_2 = 0.176 \times 47 \times 10^{-3}$

$R_2 = 8.5K\Omega$

Selection of C_E:

$$X_{CE} \le 0.1R_E$$

$$\frac{1}{2\pi F\ C_E} \le 0.1\ R_E \quad \rightarrow \quad C_E \ge \frac{1}{2\pi F\ R_E \times 0.1}$$

Selection of C_C:

$$X_{CC} \le 0.1R_C$$

$$\frac{1}{2\pi F\ C_C} \le 0.1\ R_C$$

$$C_C \ge \frac{1}{2\pi F\ R_C \times 0.1}$$

Selection of $L_1 L_2$ &C :

$$F = \frac{1}{2\pi\sqrt{Leq\ C}}$$

$$Leq = L_1 L_2$$

$$L_1 = L_2 = 20mH$$

$Leq = 40mH$

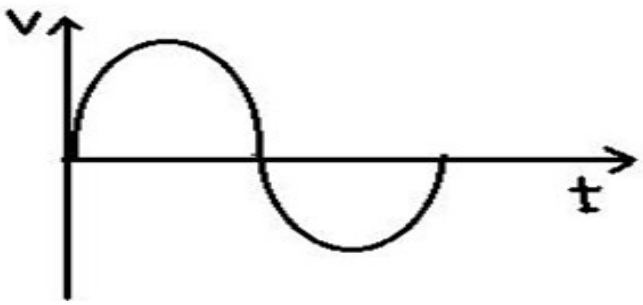
$$C = \frac{1}{4\pi2\ f2\ Leq}$$

$$= 1\ C = \frac{}{4\pi2\times4\times10^{6}\times40\times10^{-3}}$$

$0.158\ \mu f$ Choose

$C = 0.1\mu f$

MODELGRAPH:



THEORY:

LC oscillator consisting of a tank circuit for generating sine wave of required frequency. Rectifying Barkhausen criteria A for a circuit containing reactance A must be positive and greater than or equal to unity.

PROCEDURE:

1. The circuit is constructed as per the given circuit diagram.
2. Switch on the power supply and observe the output on the CRO (sine wave)
3. Note down the practical frequency and compare it with the theoretical frequency.

TABULATION:

AMPLITUDE (V)	TIME (ms)	FREQUENCY(H_Z)

RESULT:

Thus the Hartley oscillator is designed frequency and the output waveform is drawn.

Ex. No :	COLPITTS OSCILLATOR
Date:	

AIM:

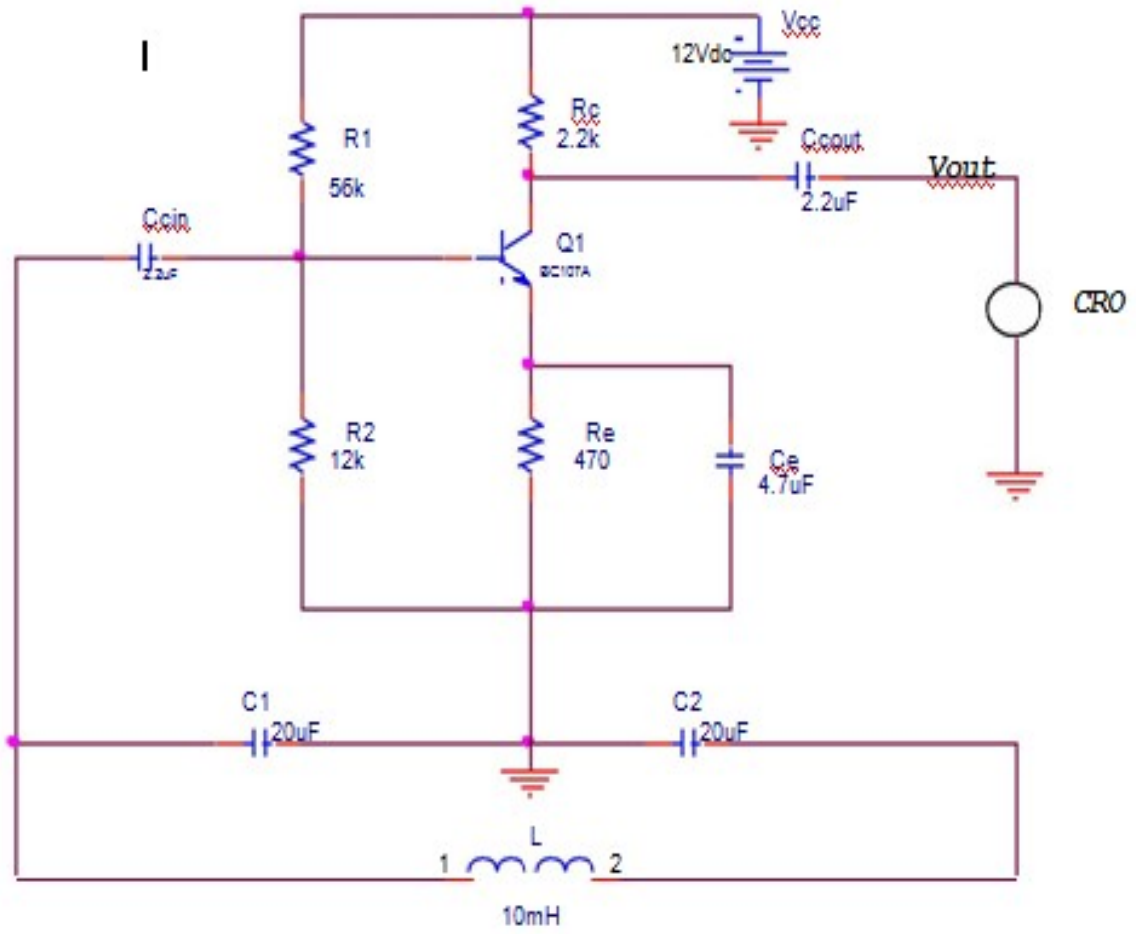
To Design and construct the given Oscillator at the given operating frequency.

APPARATUS REQUIRED:

S.NO	COMPONENTS	RANGE	QTY
1	Transistor	BC 107	1
2	Resistor	56kΩ, 2.2kΩ, 12kΩ, 470kΩ	1each
3	Capacitor	4.7µf, 2.2µf, 0.01 µf	1 3
4	Inductor	10mH	1
5	CRO	(0-30)MHz	1
6	RPS	(0-30) V	1
7	Function Generator	(0 – 1)MHZ	1

CIRCUIT DIAGRAM:

COLPITT'S OSCILLATOR



DESIGN SPECIFICATION

V_{CC}=12v I_C=2mA V_{CE} = 5v S= 20
F = 500KHz

Selection of R_E:

$V_{RE} = 0.1V_{CC}$ =

$0.1\times12=1.2V$

$V_{RE} = I_E R_E$

$R_E = \frac{V_{RE}}{I_C}$

$= \frac{1.2}{2\times10^{-3}} = 600\Omega$

$R_C = (R_C \ R_E) - R_E$

Choose R_E = 470Ω Vcc

$= I_E R_E + V_{CE} + I_C R_C$

$R_C = \frac{V_{CC} I_E R_E I_C - V_{CE}}{}$

$= \frac{12-5-2\times10^{-3}\times470}{1\times10^{-3}}$

$= 3.03\times10^{3}$

Choose R_C = 2.2kΩ

Selection of R_1 & R_2:

$$S = \frac{1+\beta}{1+\beta\left(\frac{Re}{Re+Rb}\right)}$$

$$12 = \frac{1+125}{1+125\left(\frac{470}{470+Rb}\right)}$$

$R_B = 10.6K\Omega$

$R_B = \frac{R1R2}{R1+R2} = 10.6K\Omega$

Choose $R_2 = 12k\Omega$

$\frac{1200R1}{1200+R1} = 10.6\times10^{3}$

$R_1 = 60K\Omega$

Choose $R_1 = 56k\Omega$

Selection of L&C:

$F = \frac{1}{2\pi}\sqrt{\frac{1}{L}\left(\frac{C1+C2}{C1C2}\right)}$

$F^2 = \frac{1}{4\pi2} \times \frac{1}{L}\left(\frac{C1+C2}{C1C2}\right)$

Choose $L = 10mH$

$\frac{C1+C2}{C1C2} = 4\pi^2 f^2 L$

$= 4\pi^2 \times 250000 \times 10 \times 10^{-3}$

$= 98696.04$

Assume $C_1 = C_2 = C$

$\frac{2C}{C2} = \frac{2}{C} = 98696.04$

$C = 20.26\mu f$

Choose $C_1 = C_2 = 20\ \mu f$

Selection of C_E:

$X_{CE} \le 0.1R_E$

$\frac{1}{2\pi F C_E} \le 0.1 R_E \quad \rightarrow \quad C_E \ge \frac{1}{2\pi F R_E \times 0.1}$

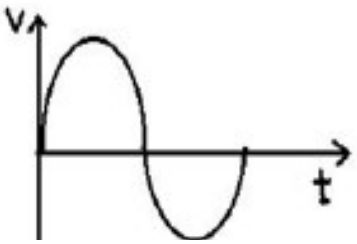
Selection of C_C:

$X_{CC} \le 0.1R_C$

$\frac{1}{2\pi F C_C} \le 0.1 R_C$

$C_C \ge \frac{1}{2\pi F R_C \times 0.1}$

MODEL GRAPH:



THEORY:

LC oscillator consisting of a tank circuit for generating sine wave of required frequency. Rectifying Barkhausen criteria A for a circuit containing reactance A must be positive and greater than or equal to unity.

PROCEDURE:

1. The circuit connection is made as per the circuit diagram.
2. Switch on the power supply and observe the output on the CRO(sine wave).
3. Note down the practical frequency and compare it with the theoretical frequency.

TABULATION:

AMPLITUDE (V)	TIME (ms)	FREQUENCY(H_Z)

RESULT:

Thus the Colpitts oscillator is designed for the given frequency and the output response is verified.

Theoretical value =

Practical value =

INTEGRATOR AND DIFFERENTIATOR USING OP-AMP.

Exp. No :

Date :

AIM:

To construct the Integrator and Differentiator circuits using Op-amp. IC and study the output waveforms.

APPARATUS REQUIRED:

Sl. No:	Apparatus Name	Range	Qty.
1	Operational Amplifier	IC 741	1
2	Resistors	1 KΩ 10 KΩ	2 1
3	Capacitor	0.1μF	
4	Bread Board		1
5	Regulated Power Supply	± 15V, Dual	1
6	Function Generator	(1Hz – 1MHz.)	1
7	Cathode Ray Oscilloscope	20 / 40MHz, Dual Trace	1
8	Connecting Wires & CRO Probes		

THEORY:

Integrator produces a voltage output proportional to the product (multiplication) of the input voltage and time; and the differentiator (not to be confused with differential) produces a voltage output proportional to the input voltage's rate of change.

Differentiator:

Capacitance can be defined as the measure of a capacitor's opposition to changes in voltage. The greater the capacitance, the more the opposition. Capacitors oppose voltage change by creating current in the circuit: that is, they either charge or discharge in response to a change in applied voltage. So, the more capacitance a capacitor has, the greater its charge or discharge current will be for any given rate of voltage change across it. The equation for this is quite simple:

$$i = C\,(dv/dt)$$

The dv/dt fraction is a calculus expression representing the rate of voltage changes over time.

Capacitor current moves through the feedback resistor, producing a drop across it, which is the same as the output voltage. A linear, positive rate of input voltage change will result in a steady negative voltage at the output of the Op-amp. Conversely, a linear, negative rate of input voltage change will

result in a steady positive voltage at the output of the op-amp. The faster the rate of voltage changes at the input (either positive or negative), the greater the voltage at the output.

The formula for determining voltage output for the differentiator is as follows:

Vout = -RC d/dt (Vin)

Integrator:

Here, the op-amp circuit would generate an output voltage proportional to the magnitude and duration that an input voltage signal has deviated from 0 volts. Stated differently, a constant input signal would generate a certain rate of change in the output voltage: differentiation in reverse. To do this, all we have to do is swap the capacitor and resistor in the previous circuit:

A simple low pass RC circuit can also work as an Integrator when time constant is very large. This requires very large values of R and C. The components R and C cannot be made infinitely large because of practical limitations. However in the op-amp integrator by Miller's theorem, the effective input capacitance becomes Cf (1-Av), where Av is the gain of the Op-amp. The Gain (Av) is the infinite for an ideal Op-amp, so the effective time constant of the Op-amp Integrator becomes very large which results perfect integration.

The integrator produces a voltage output proportional to the product (multiplication) of the input voltage and time

However, if we apply a constant, positive voltage to the input, the Op-amp output will fall negative at a linear rate, in an attempt to produce the changing voltage across the capacitor necessary to maintain the current established by the voltage difference across the resistor. Conversely, a constant, negative voltage at the input results in a linear, rising (positive) voltage at the output. The output voltage rate-of-change will be proportional to the value of the input voltage.

The formula for determining voltage output for the integrator is as follows:

$$\frac{dV_{out}}{dt} = -\frac{V_{in}}{RC}$$

or

$$V_{out} = \int_0^t -\frac{V_{in}}{RC}\,dt + c$$

Where,

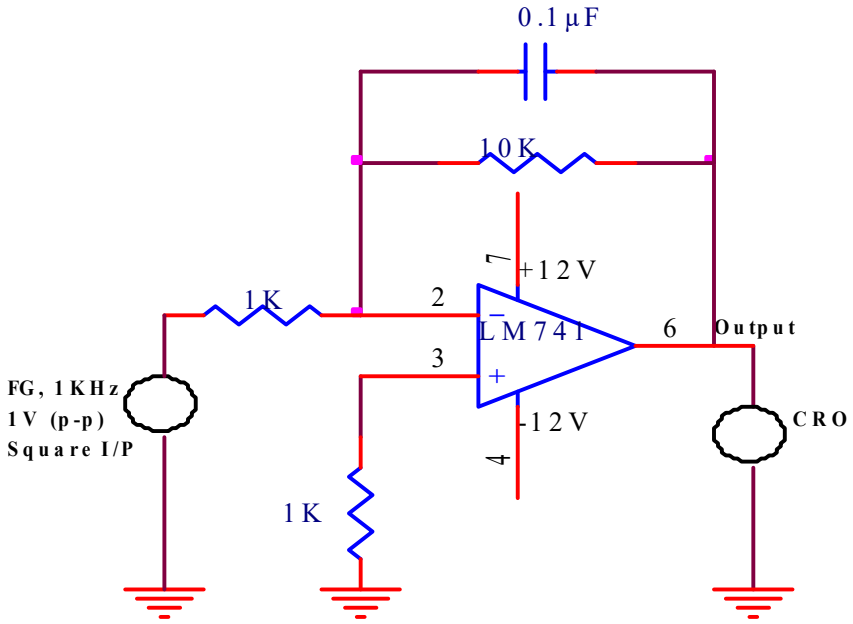
c = Output voltage at start time (t=0)

DESIGN & CALCULATIONS IF ANY:

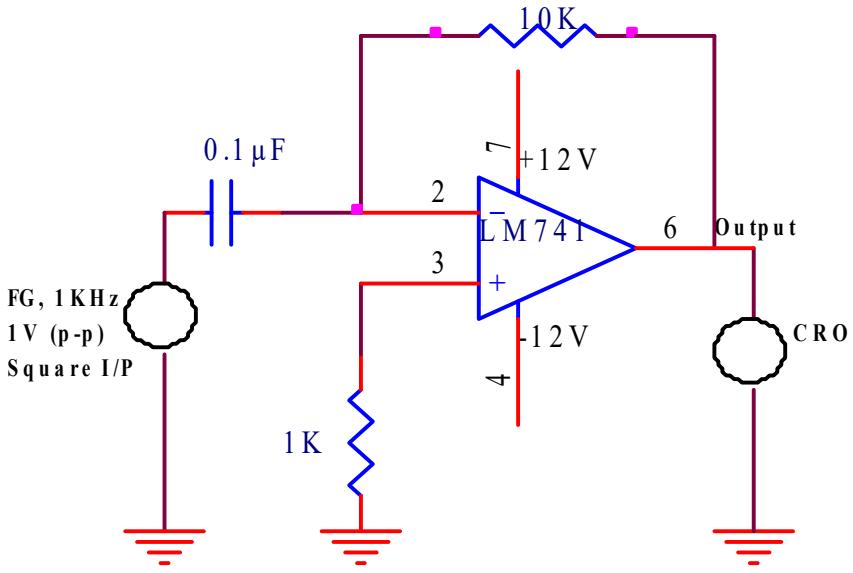
Integrator: Differentiator:

CIRCUIT DIAGRAM:

INTEGRATOR CIRCUIT



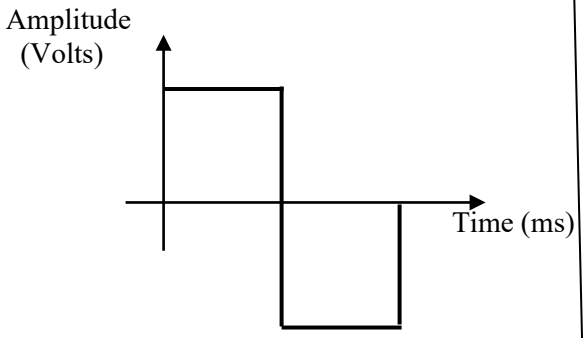
DIFFERENTIATOR CIRCUIT



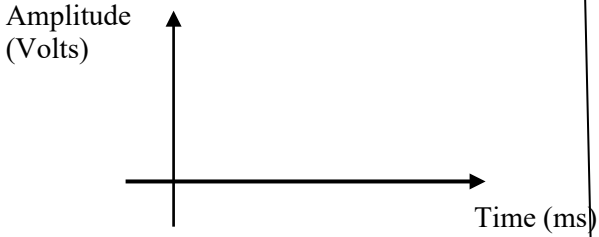
MODEL GRAPH:

Integrator

Input Signal (1 KHz Freq.)

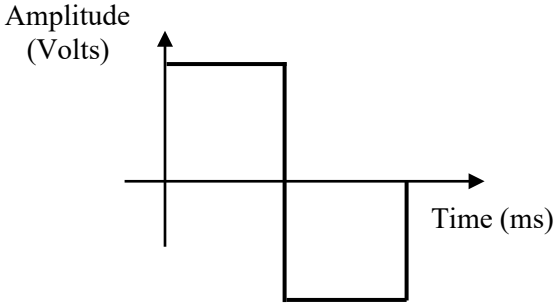


Output Signal (1 KHz Freq.)

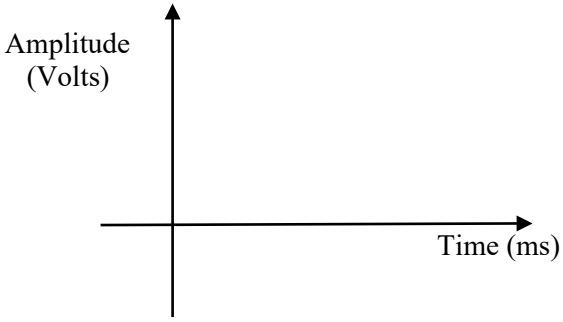


Differentiator

Input Signal (1 KHz Freq.)



Output Signal (1 KHz Freq.)



TABULAR COLOUMN:

INTEGRATOR			DIFFERENTIATOR	
	Input Signal	Output Signal	Input Signal	Output Signal
Amplitude				
Time Period				
Frequency				

PROCEDURE:

1. Construct the circuit as per Circuit diagram shown in figure.
2. Select the Square waveform in Function Generator and set fixed amplitude and fixed frequency say 1V (p-p) and 1 KHz respectively.
3. The resistance Rcomp is also connected to the Non-inverting input terminal to minimize the effect of the input bias current.
4. Note the corresponding input and output signals (refer model graph) for both Circuits.
5. Note the gain of the integrator decreases with increasing frequency.
6. Tabulate the noted readings and draw the input and output waveforms in Graph sheet.

RESULT:

VIVA VOCE:

1. What are the main drawbacks of ideal differentiator?

   At high frequency, differentiators may become unstable and break into oscillation. The input impedance i.e. ($1/\omega C1$) decreases with increase in frequency, thereby making the circuit sensitive to high frequency noise.

2. What are the steps to be followed while designing a good differentiator?

   Choose fa equal to highest frequency of the input signal. Assume a practical value of C1 (<1μF) and then calculate Rf.
   Choose fb=10fa (Say). Now calculate the values of R1 and C1.
   R1C1 = RfCf.

3. What are the main drawbacks of ideal integrator circuit?

   At low frequencies such as dc ($\omega \approx 0$) the gain becomes infinite.
   When the op-amp saturates i.e. the capacitor is fully charged it behaves like an open circuit.

EX.NO:	
DATE:	**CLIPPER AND CLAMPER**

AIM:

To design and study the clipper and clamper circuits.

APPARATUS REQUIRED:

S.NO	COMPONENTS	RANGE	QTY
1	Diode	IN4001	1
2	Resistor	1kΩ	1
3	CRO	(0-30)MHz	1
4	RPS	(0-30) V	1
5	Function Generator	(0 – 1)MHZ	1
6	Breadboard	-	1
7	Connecting wires	-	1

THEORY:

CLIPPERS:

Clippers have the ability to clip off a portion of the input signal without distorting the remaining part of the alternating waveform. The half wave rectifier is an example of the simplest form of diode clipper – one resistor and diode. Depending upon the orientation of the diode, the positive or negative region of the input signal is clipped off.Clippers are of two: i.Series ii. Parallel.Series configuration is defined as one where diode is in series with the load, while in parallel the diode is connected in parallel to the load.

CLAMPERS:

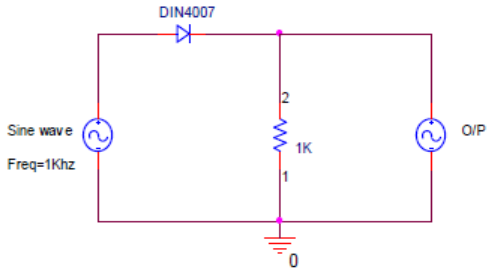
The clamping network is one that will clamp a signal to different dc level. The circuit has a diode, resistor and a capacitive element, but it can also employ an independent dc supply to introduce an additional shift. The magnitude of R and C must be chosen that the time constant. τ = RC is large enough that the voltage across the capacitor does not discharge significantly during the interval when the diode is non conducting.

PROCEDURE:

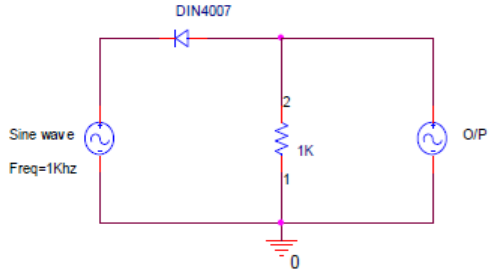
1. Connections are given as per the circuit .
2. Set input signal voltage (5v,1kHz) using function generator.
3. Observe the output waveform using CRO
4. Sketch the observed waveform on the graph sheet.

CIRCUIT DIAGRAM:

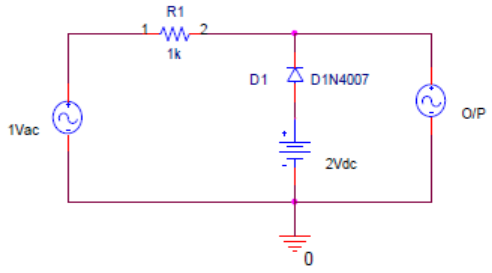
NEGATIVE CLIPPER:



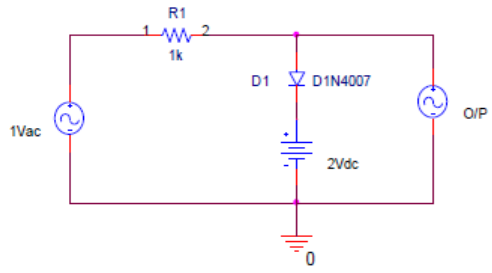
POSITIVE CLIPPER:



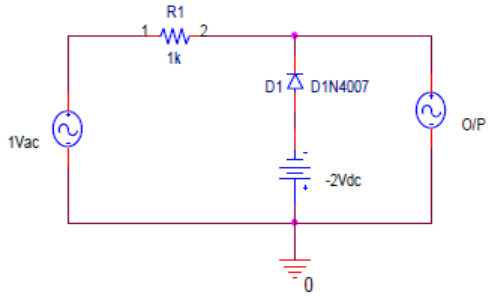
POSITIVE BIASED NEGATIVE CLIPPER:



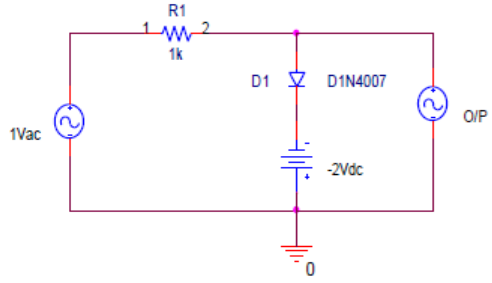
POSITIVE BIASED POSITIVE CLIPPER:



NEGATIVE BIASED NEGATIVE CLIPPER:



NEGATIVE BIASED PASITIVE CLIPPER:

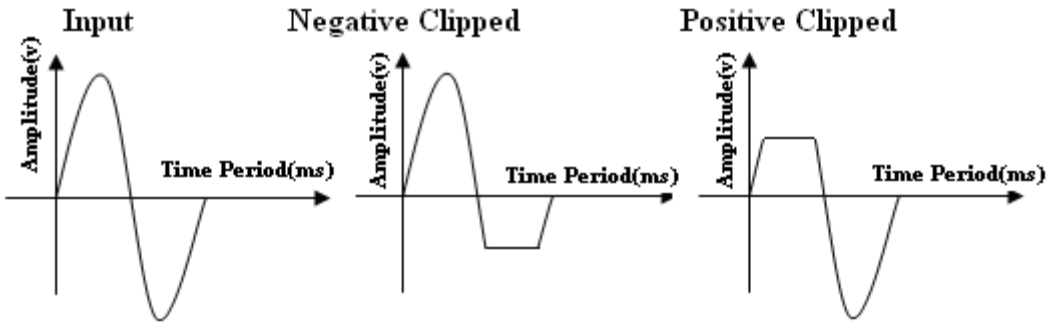


TABULATION:

WAVE FORM	**AMPLITUDE (V)**	**TIME PERIOD (ms)**
INPUT SIGNAL		
+VE BIASED +VE CLIPPER		

-VE BIASED +VE CLIPPER		
+VE BIASED -VE CLIPPER		
-VE BIASED -VE CLIPPER		

MODEL GRAPH:



CLAMPING CIRCUITS

AIM: To study the clamping circuits

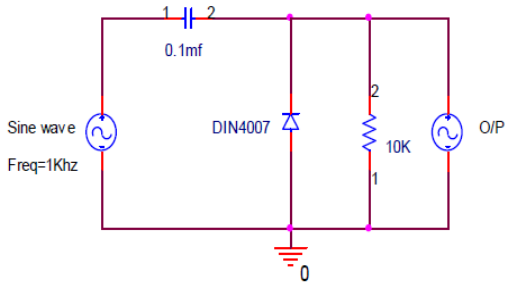
(a). Positive clamper circuit (b) Negative clamper circuit

APPARATUS REQUIRED :

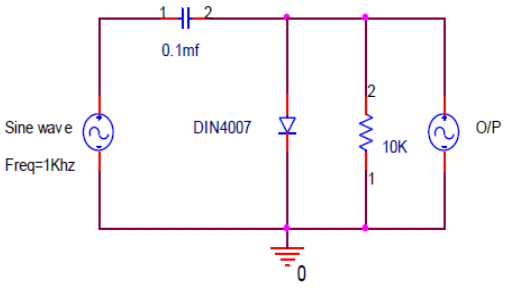
S.NO	COMPONENTS	RANGE	QTY
1	Diode	IN4001	1
2	Resistor	10kΩ	2
3	Capacitor	0.1 µf	1
4	CRO	(0-30)MHz	1
5	RPS	(0-30) V	1
6	Function Generator	(0 – 1)MHZ	1
7	Breadboard	-	1
8	Connecting wires	-	-

CIRCUIT DIAGRAM:

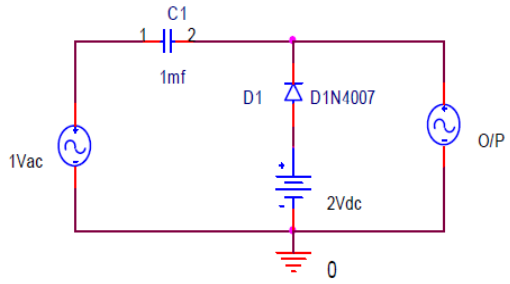
POSITIVE CLAMPER:



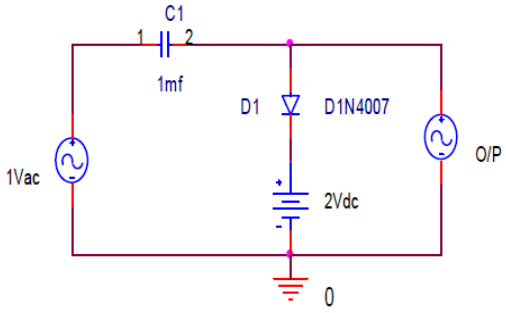
NEGATIVE CLAMPER:



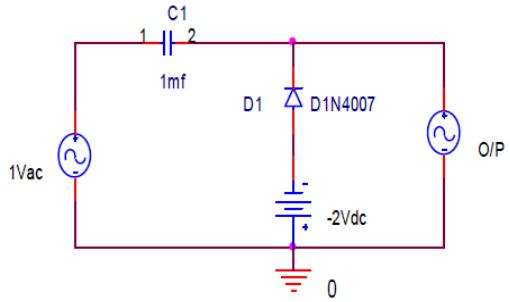
POSITIVE BIASED POSITIVE CLAMPER:



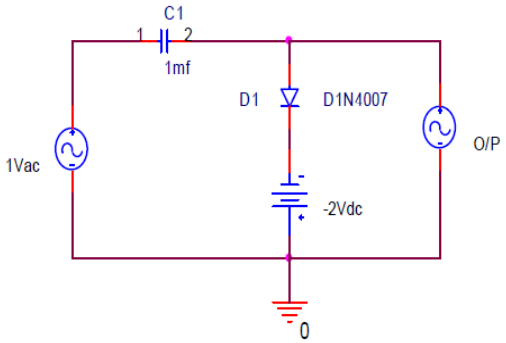
POSITIVE BIASED NEGATIVE CLAMPER:



NEGATIVE BIASED POSITIVE CLAMPER:



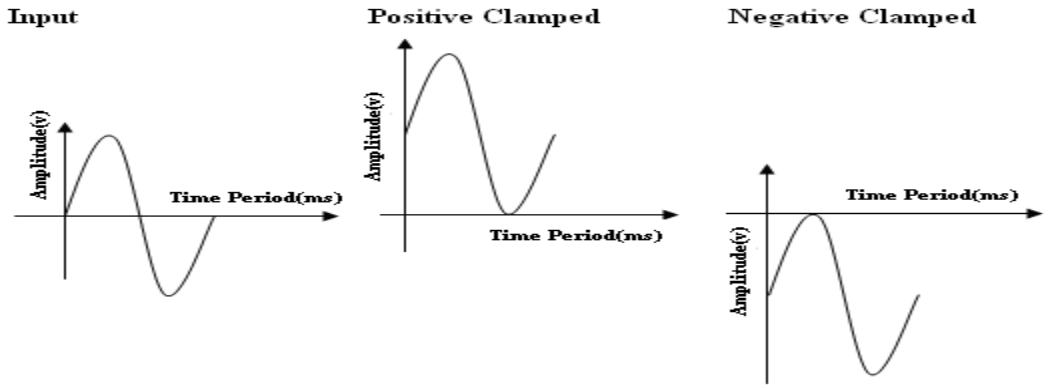
NEGATIVE BIASED NEGATIVE CLAMPER:



TABULATION:

WAVE FORM	AMPLITUDE (V)	TIME PERIOD (ms)
INPUT SIGNAL		
+VE BIASED +VE CLAMPER		
-VE BIASED +VE CLAMPER		
+VE BIASED -VE CLAMPER		
-VE BIASED -VE CLAMPER		

MODEL GRAPH:



PROCEDURE:

1. Connections are given as per the circuit .
2. Set input signal voltage (5v,1kHz) using function generator.
3. Observe the output waveform using CRO.
4. Sketch the observed waveform on the graph sheet.

RESULT:

Thus the clipper and clamper circuits are designed and its waveform are observed.

SECOND ORDER ACTIVE LOW PASS FILTER.

Exp. No :

Date :

AIM:

To Design and Construct a second order low pass filter having upper cut off frequency 1 KHz using Op-amp. IC and also determine its frequency response.

APPARATUS REQUIRED:

Sl. No:	Apparatus Name	Range	Qty.
1	Operational Amplifier	IC 741	1
2	Resistors	10 KΩ 1.5 KΩ 5.6 KΩ	1 2 1
3	Capacitor	0.1μF	2
4	Bread Board		1
5	Regulated Power Supply	± 15V, Dual	1
6	Function Generator	(1Hz – 1MHz.)	1
7	Cathode Ray Oscilloscope	20 / 40MHz, Dual Trace	1
8	Connecting Wires & CRO Probes		

THEORY:

An improved filter response can be obtained by using a Second order Active Filter. A second order filter consists of two RC pairs and has a roll-off rate of -40 dB/decade. A general second order filter (Sallen Kay filter) is used to analyze different LP, HP, BP and BSF. A first order filter can be converted to second order type using an additional RC network as shown in circuit diagram. The cut off frequency f_H for the filter is now decided by R and C. The gain of the filter is usual decided by op-amp i.e. the resistance R3 and Rf.

DESIGN & CALCULATIONS IF ANY:

Given: fH = 1 KHz = 1/ (2πRC)

Let C = 0.1 μF, R = 1.6 KΩ
For n = 2, α (damping factor) = 1.414,
Pass Band Gain = Ao = 3 - α =3 – 1.414 = 1.586.

Transfer function of second order Butter worth LPF as:

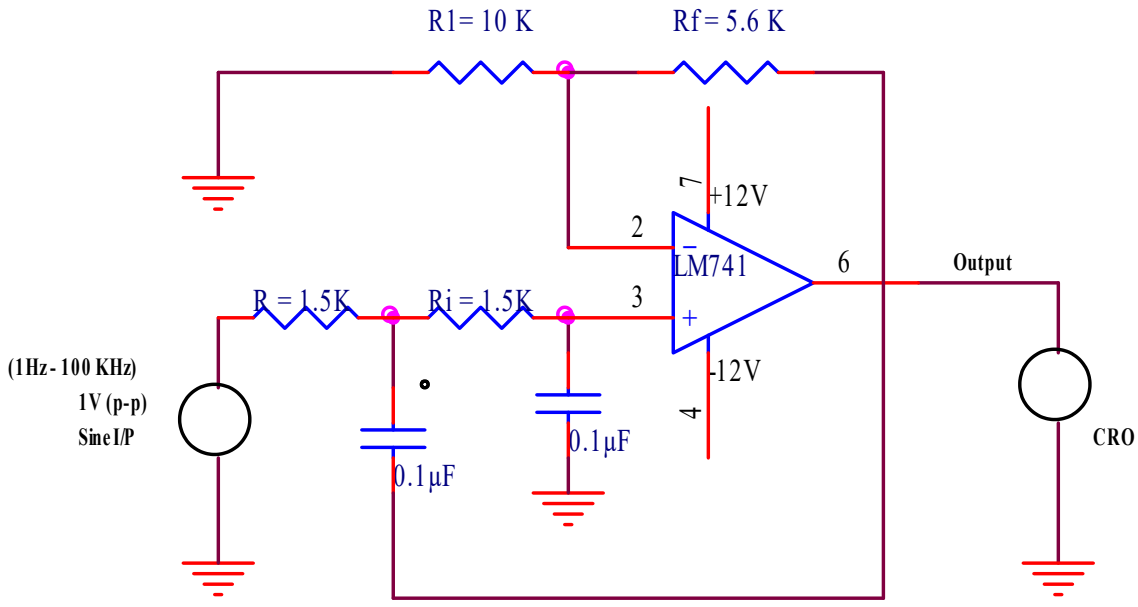
$$H(s) = \frac{1.586}{S2 + 1.414\,s + 1}$$

Now Ao = 1 + (Rf / R1) = 1.586 = 1 + 0.586

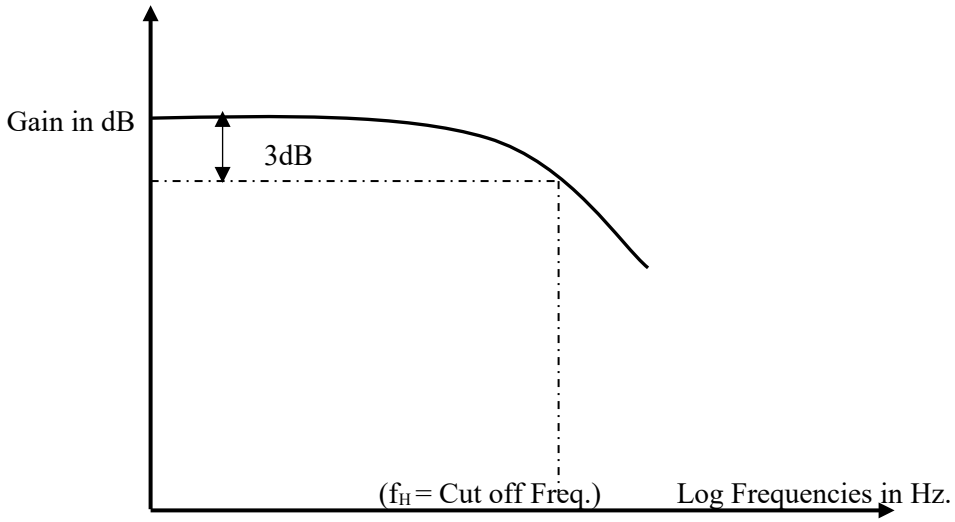
Let Ri = 10 KΩ, then Rf = 5.86 KΩ

CIRCUIT DIAGRAM:

SECOND ORDER ACTIVE LOW PASS FILTER



MODEL GRAPH:



TABULAR COLOUMN: Vin =

Sl.No.	Frequency (Hz)	Vout (V)	Gain = Vo / Vin	Gain in dB = 20 log Gain
1				
2				
3				
4				
5				
6				
7				
8				
9				
10				
11				
12				
13				
14				
15				

PROCEDURE:

1. Construct the circuit as per Circuit diagram shown in figure.
2. Select the Sine waveform in Function Generator and set fixed amplitude and fixed frequency say 1V (p-p) and 1 KHz respectively.
3. Observe the output waveform for different frequency ranges (start from 50 Hz to beyond some value of cut of frequency)
4. Note the readings observed on CRO and find its gain for different frequency ranges.
5. Draw the graph for its Gain in dB Vs. Frequency and find its Cut off frequency.

RESULT:

VIVA VOCE:

1. What are the main drawbacks of ideal differentiator?

   At high frequency, differentiators may become unstable and break into oscillation. The input impedance i.e. $(1/\omega C1)$ decreases with increase in frequency, thereby making the circuit sensitive to high frequency noise.

2. What are the steps to be followed while designing a good differentiator?

   Choose fa equal to highest frequency of the input signal. Assume a practical value of C1 ($<1\mu F$) and then calculate Rf.
   Choose fb=10fa (Say). Now calculate the values of R1 and C1.
   $R1C1 = RfCf$.

3. What are the main drawbacks of ideal integrator circuit?

   At low frequencies such as dc ($\omega \approx 0$) the gain becomes infinite.
   When the op-amp saturates i.e. the capacitor is fully charged it behaves like an open circuit.

SECOND ORDER ACTIVE HIGH PASS FILTER.

Exp. No :

Date :

AIM:

To Design and Construct a second order low pass filter having upper cut off frequency 1 KHz using Op-amp. IC and also determine its frequency response.

APPARATUS REQUIRED:

Sl. No:	Apparatus Name	Range	Qty.
1	Operational Amplifier	IC 741	1
2	Resistors		
3	Capacitor	0.1Mf	2
4	Bread Board		1
5	Regulated Power Supply	$\pm$ 15V, Dual	1
6	Function Generator	(1Hz – 1MHz.)	1
7	Cathode Ray Oscilloscope	20 / 40MHz, Dual Trace	1
8	Connecting Wires & CRO Probes		

THEORY:

An improved filter response can be obtained by using a Second order Active Filter. A second order filter consists of two RC pairs and has a roll-off rate of -40 dB/decade. A general second order filter (Sallen Kay filter) is used to analyze different LP, HP, BP and BSF. A first order filter can be converted to second order type using an additional RC network as shown in circuit diagram. The cut off frequency f_L for the filter is now decided by R and C. The gain of the filter is usual decided by op-amp i.e. the resistance R3 and Rf.

DESIGN & CALCULATIONS IF ANY:

Given: $f_L = 1$ KHz $= 1/(2\pi RC)$

Let C = 0.1 μF, R = 1.6 KΩ
For n = 2, α (damping factor) = 1.414,
Pass Band Gain = Ao = 3 - α =3 – 1.414 = 1.586.

Transfer function of second order Butter worth HPF as:

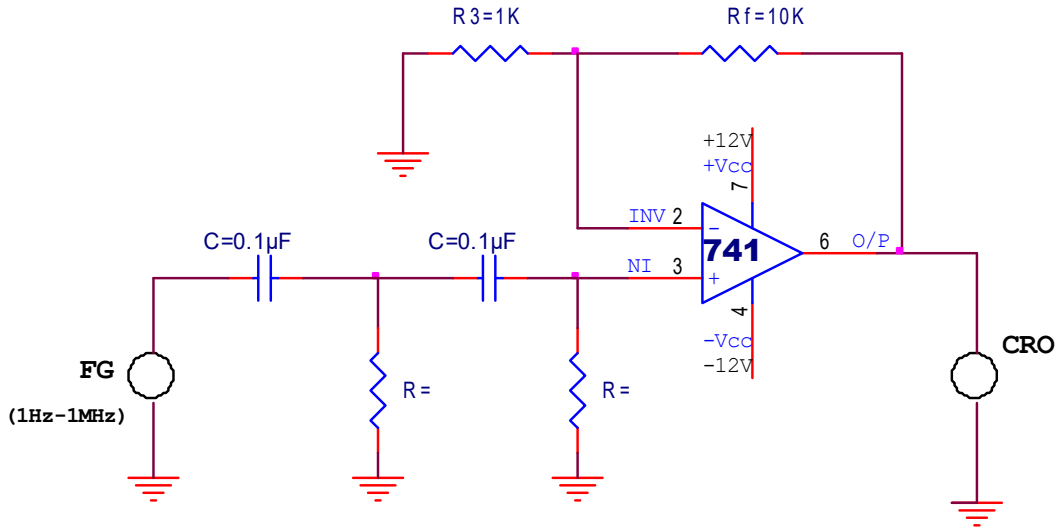
$$H(s) = \frac{1.586}{S2 + 1.414\ s + 1}$$

Now Ao = 1 + (Rf / R1) = 1.586 = 1 + 0.586

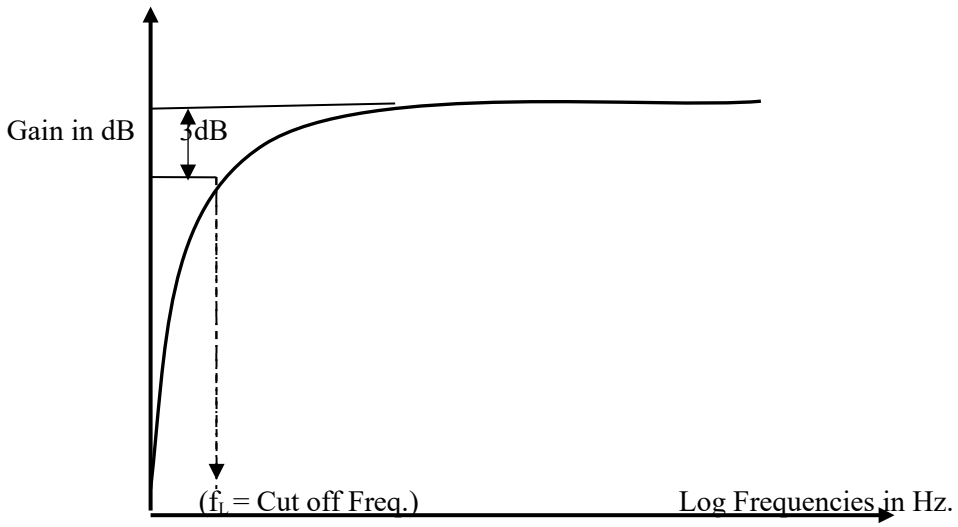
Let Ri = 10 KΩ, then Rf = 5.86 KΩ

CIRCUIT DIAGRAM:

SECOND ORDER ACTIVE HIGHPASS FILTER CIRCUIT DIAGRAM



MODEL GRAPH:



TABULAR COLOUMN: Vin =

Sl.No.	Frequency (Hz)	Vout (V)	Gain = Vo / Vin	Gain in dB = 20 log Gain
1				
2				
3				
4				
5				
6				
7				
8				
9				
10				
11				
12				
13				
14				
15				

PROCEDURE:

1. Construct the circuit as per Circuit diagram shown in figure.
2. Select the Sine waveform in Function Generator and set fixed amplitude and fixed frequency say 1V (p-p) and 1 KHz respectively.
3. Observe the output waveform for different frequency ranges (start from 100 Hz to beyond some value of cut of frequency, observe the output signal which pass beyond the higher cut of frequency)
4. Note the readings observed on CRO and find its gain for different frequency ranges.
5. Draw the graph for its Gain in dB Vs. Frequency and find its Cut off frequency.

RESULT:

ACTIVE BAND PASS FILTER.

Exp. No :

Date :

AIM:

To Design and Construct a second order low pass filter having upper cut off frequency 400 Hz and lower cut of frequency for 2 KHz using Op-amp. IC and also determine its frequency response.

APPARATUS REQUIRED:

Sl. No:	Apparatus Name	Range	Qty.
1	Operational Amplifier	IC 741	1
2	Resistors		
3	Capacitor	0.1μF	2
4	Bread Board		1
5	Regulated Power Supply	± 15V, Dual	1
6	Function Generator	(1Hz – 1MHz.)	1
7	Cathode Ray Oscilloscope	20 / 40MHz, Dual Trace	1
8	Connecting Wires & CRO Probes		

THEORY:

An improved filter response can be obtained by using a Second order Active Filter. A second order filter consists of two RC pairs and has a roll-off rate of -40 dB/decade. A general second order filter (Sallen Kay filter) is used to analyze different LP, HP, BP and BSF. Band pass filter is a combination of High pass and Low pass filter. A Band pass filter is basically a frequency selector. It allows one particular band of frequencies to pass. Its pass band between two cut off frequencies f_H and f_L. The pass band which is between f_H and f_L is called Bandwidth of the filter denoted as BW.

$$\text{Bandwidth} = f_H - f_L$$

DESIGN & CALCULATIONS IF ANY:

Given: fH = 400Hz = 1/ (2πRC)

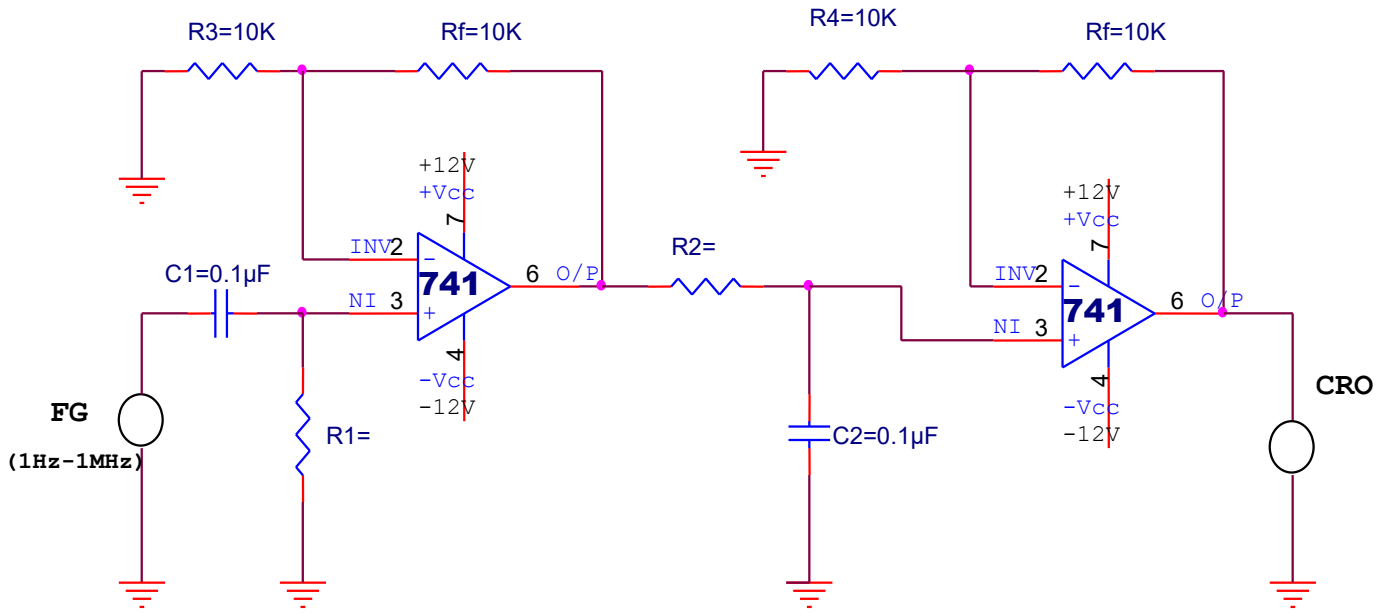
Let C = 0.1 μF, R =

Similarly, for LPF
fL = 2KHz = 1/ (2πRC)

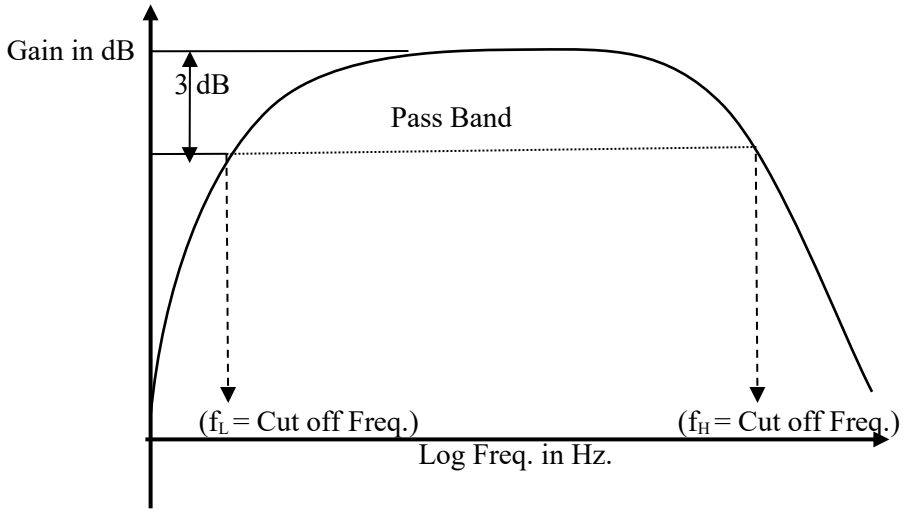
Let C = 0.1 μF, R =

CIRCUIT DIAGRAM:

ACTIVE BANDPASS FILTER CIRCUIT DIAGRAM



MODEL GRAPH:



TABULAR COLOUMN: Vin =

Sl.No.	Frequency (Hz)	Vout (V)	Gain = Vo / Vin	Gain in dB = 20 log Gain
1				
2				
3				
4				
5				
6				
7				
8				
9				
10				
11				
12				
13				
14				
15				

PROCEDURE:

1. Construct the circuit as per Circuit diagram shown in figure.
2. Select the Sine waveform in Function Generator and set fixed amplitude and fixed frequency say 1V (p-p) and 1 KHz respectively.
3. Observe the output waveform for different frequency ranges (start from 100 Hz to beyond some value of cut of frequency, observe the output signal which pass beyond the higher cut of frequency and it attenuates from lower cut of frequency)
4. Note the readings observed on CRO and find its gain for different frequency ranges.
5. Draw the graph for its Gain in dB Vs. Frequency and find its Cut off frequency.

RESULT:

VIVA VOCE:

1. State the disadvantages of passive filters?

   At audio frequencies inductors becomes problematic, as the inductors become large, heavy and expensive. For low frequency application, more number of turns of wire must be used which in turn adds to the series resistance degrading inductors performance.

2. Derive the expression for voltage gain of an inverting operational amplifier?

$$A_{CL} = Vo/Vi = -R_f / R_1$$

INSTRUMENTATION AMPLIFIER

Exp. No :

Date :

AIM:

To design and construct Instrumentation Amplifier Circuit using Op-amp IC.

APPARATUS REQUIRED:

Sl. No:	Apparatus Name	Range	Qty.
1	Operational Amplifier	IC 741	3
2	Resistors	10 KΩ	7
3	Bread Board		1
4	Regulated Power Supply (Variable)	± 15V, Dual	4
5	Multimeter		1
6	Connecting Wires & CRO Probes		

THEORY:

An instrumentation amplifier is a type of differential amplifier that has been specifically designed to have characteristics suitable for use in measurement and test equipment. These characteristics include very low DC offset, low drift, low noise, very high open-loop gain, very high common-mode rejection ratio, and very high input impedances. They are used where great accuracy and stability of the circuit both short- and long-term are required.

The most commonly used instrumentation amplifier circuit is shown in the figure. The gain of the circuit is

$$\frac{V_{\text{out}}}{V_2 - V_1} = \left(1 + \frac{2R_1}{R_{\text{gain}}}\right)\frac{R_3}{R_2}$$

The ideal common-mode gain of an instrumentation amplifier is zero. In the circuit shown, common-mode gain is caused by mismatches in the values of the equally numbered resistors and by the non-zero common mode gains of the two input op-amps. Obtaining very closely matched resistors is a significant difficulty in fabricating these circuits, as is optimizing the common mode performance of the input op-amps.

DESIGN & CALCULATIONS IF ANY:

$$\frac{V_{out}}{V_2 - V_1} = \left(1 + \frac{2R_1}{R_{gain}}\right)\frac{R_3}{R_2}$$

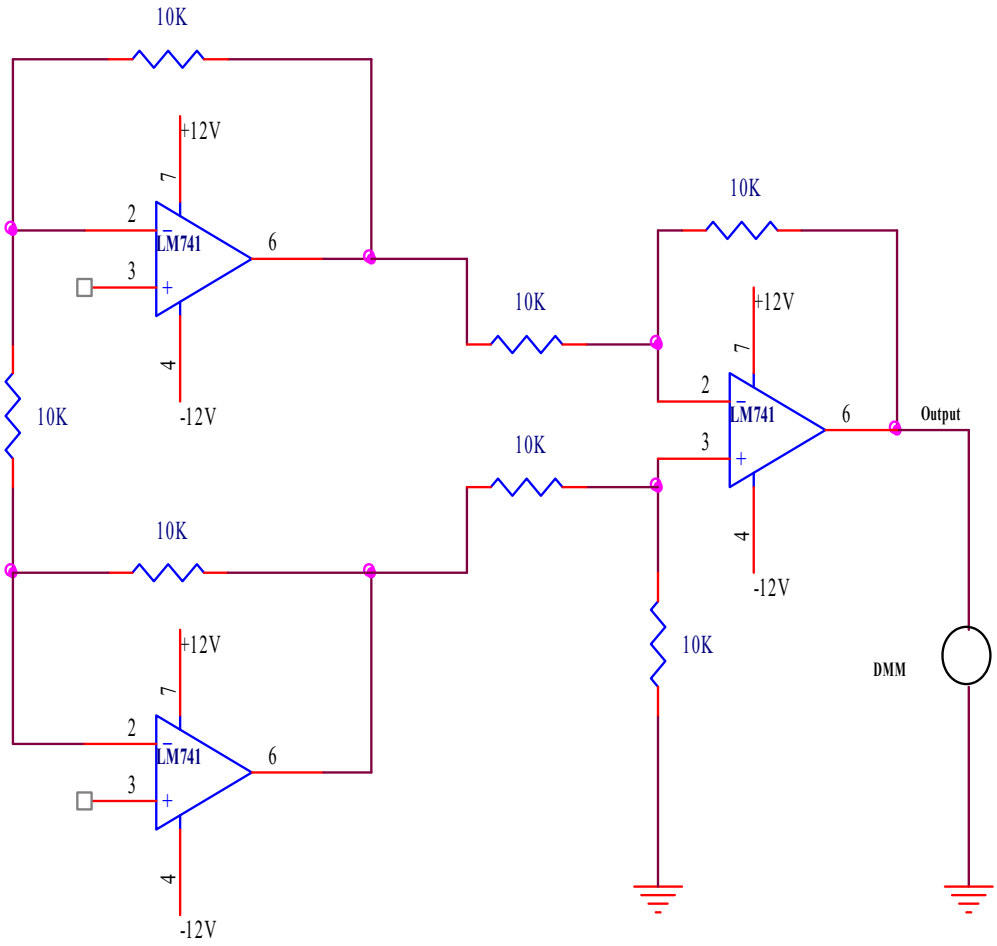
Let R1= R2 = R3 = Rgain = 10 KΩ then

Vout = (1+2) (V2-V1)

Vout = 3 (V2-V1)

CIRCUIT DIAGRAM:

INSTRUMENTATION AMPLIFIER USING 741 IC.



TABULAR COLOUMN:

SL.NO.	INPUTS		OUTPUT	
	V1 (V)	V2 (V)	Theoretically (V)	Practically (V)
1				
2				
3				
4				
5				
6				
7				

PROCEDURE:

1. Construct the circuit as per Circuit diagram shown in figure.
2. Switch ON IC Power Supplies and apply the Input Voltages at Non-inverting input terminals.
3. Observe the Output Voltage using Digital Multimeter for different input voltages.
4. Note the readings and verify its values with theoretical calculation.

RESULT:

CHARACTERISTICS OF PLL.

Exp. No :

Date :

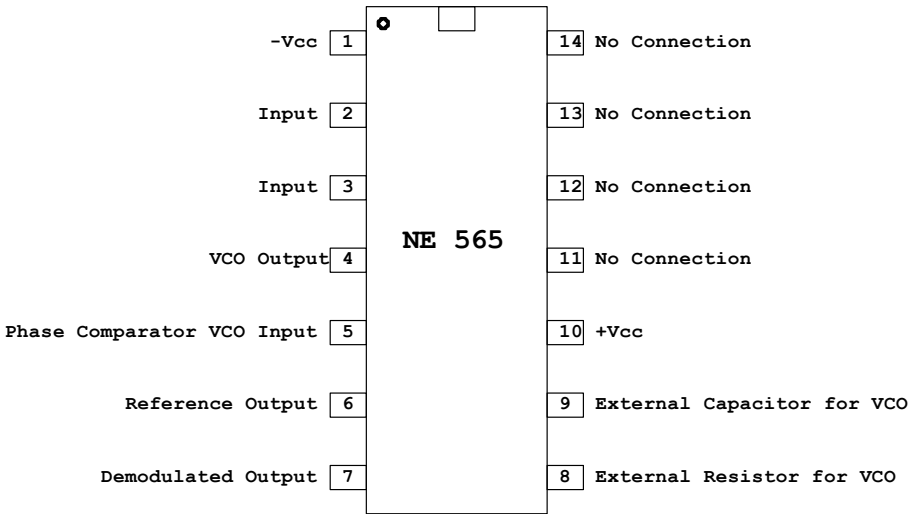
AIM:

To construct and study the operation of PLL IC 565 and determine its Characteristics.

APPARATUS REQUIRED:

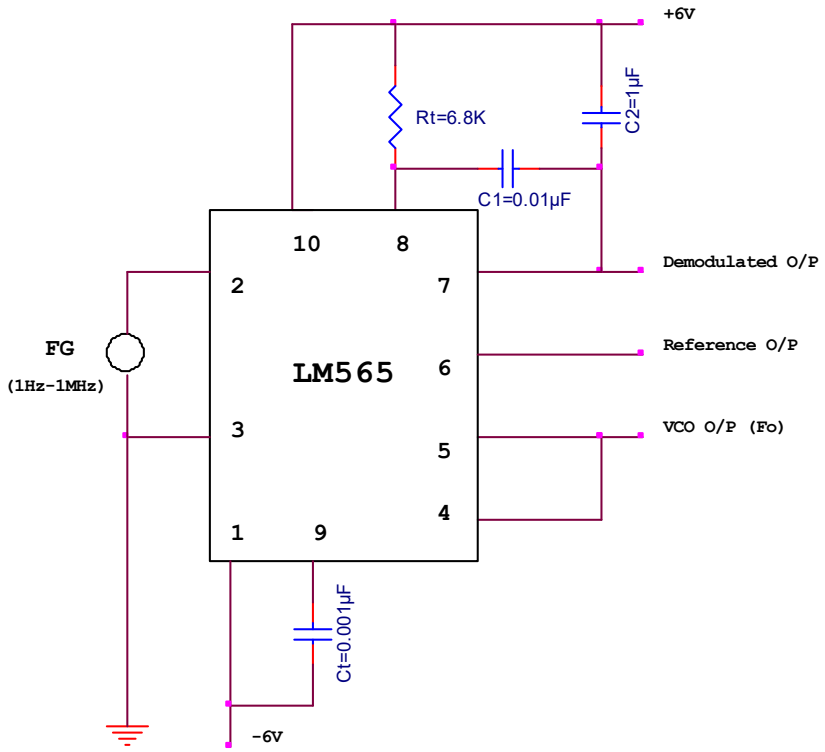
S.No	Components	Range	Quantity
1	IC 565	-	1
2	Resistors	6.8 KΩ	1
3	Capacitors	0.001 μF 0.1 μF, 1 μF	1 each
4	Function Generator	(1Hz – 1MHz.)	1
5	C.R.O	-	1
6	Dual Power Supply	0- 30 V	1

PIN DIAGRAM (IC 565 - PLL)



CIRCUIT DIAGRAM:

PLL CHARACTERISTICS USING LM565 IC CIRCUIT DIAGRAM



PROCEDURE:

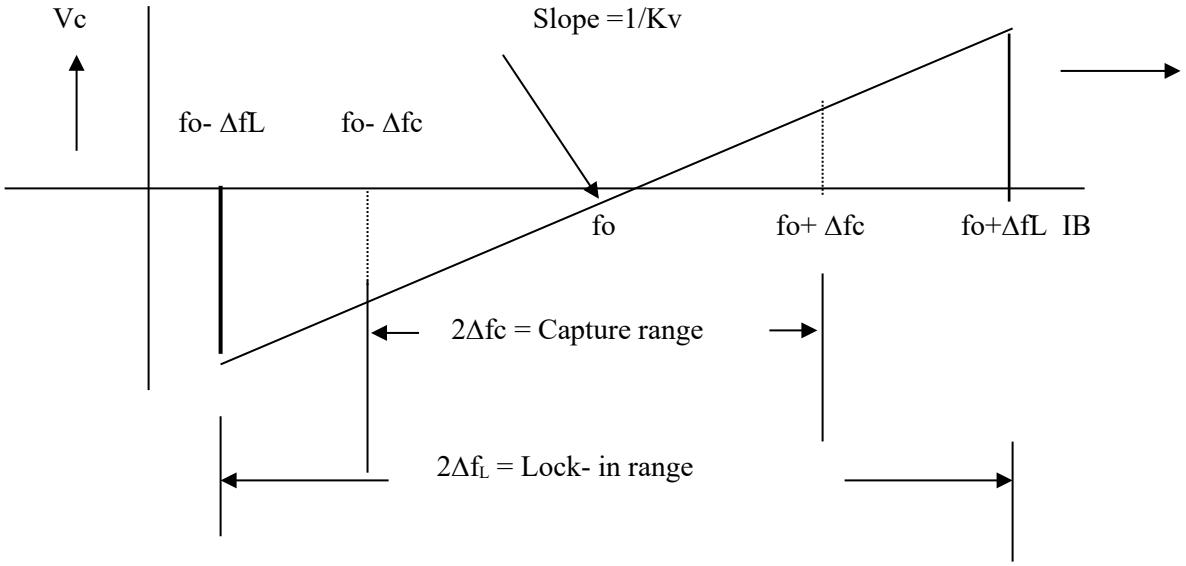
- The connections are given as per the circuit diagram.
- Measure the free running frequency of VCO at pin 4, with the input signal Vi set equal to zero. Compare it with the calculated value = 0.25 / (RT CT).
- Now apply the input signal of 1 VPP square wave at a 1 KHz to pin 2. Connect one channel of the scope to pin 2 and display this signal on the scope.
- Gradually increase the input frequency till the PLL is locked to the input frequency. This frequency f1 gives the lower end of the capture range. Go on increasing the input frequency, till PLL tracks the input signal, say, to a frequency f2.This frequency f2 gives the upper end of the lock range. If input frequency is increased further, the loop will get unlocked.
- Now gradually decrease the input frequency till the PLL is again locked. This is the frequency f3, the upper end of the capture range. Keep on decreasing the input frequency until the loop is unlocked. This frequency f4 gives the lower end of the lock range.
- The lock range $\Delta fL = (f2 - f4)$. Compare it with the calculated value of $\pm$ 7.8 fo /12. Also the capture range is $\Delta fc = (f3 - f1)$.Compare it with the calculated value of capture range.

$$\Delta fc = \pm (\Delta fL / (2\pi)(3.6)(103)\, C)1/$$

TABULAR COLOUMN:

INPUT WAVEFORM		OUTPUT WAVEFORM	
Square wave Signal		Square wave Signal with Multiple Freq.	
Amplitude (V)		Amplitude (V)	
Time (ms)		Time (ms)	
Frequency (Hz)		Frequency (Hz)	

MODEL GRAPH



RESULT :

FREQUENCY MULTIPLIER USING PLL.

Exp. No :

Date :

AIM:

To construct and study the operation of frequency multiplier using IC 565.

APPARATUS REQUIRED:

S.No	Components	Range	Quantity
1	IC 565,IC 7490,2N2222	-	1
2	Resistors	20 KΩ, 2kΩ, 4.7kΩ,10kΩ	1
3	Capacitors	0.001 µF, 10 µF	1 each
4	FunctionGenerator (Digital)	1 Hz – 2 MHz	1
5	C.R.O	-	1
6	Dual Power Supply	0- 30 V	1
7.			

THEORY:

The circuit diagram of a Frequency multiplier using PLL is shown in Figure. A divide by N network is inserted between VCO Output and Phase comparator input. In the locked stste, the VCO output frequency f_O is given by,

$f_O = N\ f_S$

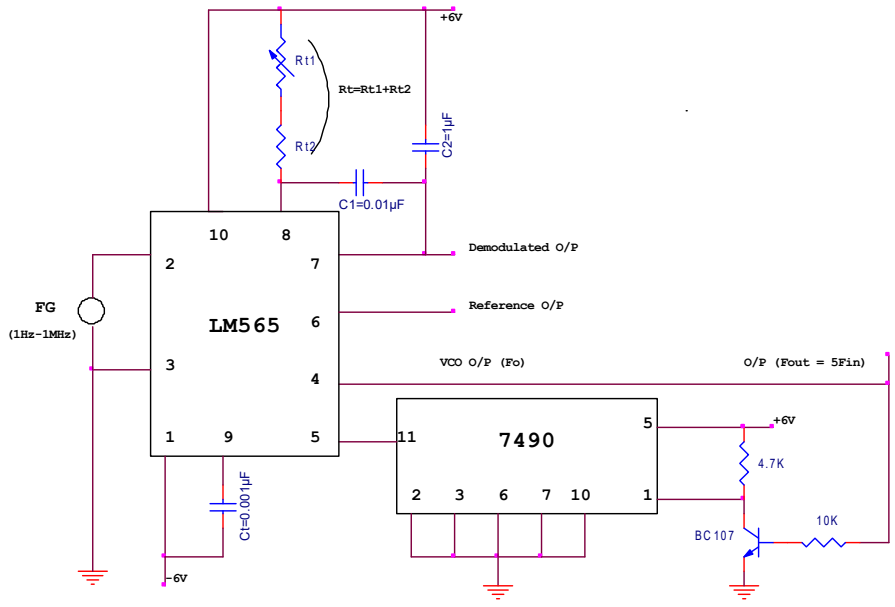
The multiplication factor can be obtained by selecting a proper scaling factor N of the counter. Frequency multiplication can also be obtained by using PLL in its harmonic locing mode.

The output of VCO is given by,

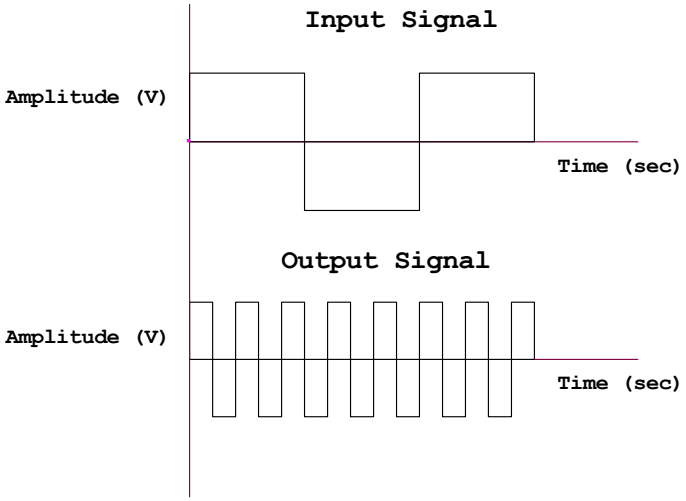
$f_O = f_S / m$

CIRCUIT DIAGRAM:

FREQUENCY MULTIPLIER USING PLL IC LM565 CIRCUIT DIAGRAM



MODEL GRAPH:



TABULAR COLOUMN:

INPUT WAVEFORM		OUTPUT WAVEFORM	
Square wave Signal		Square wave Signal (Multiples of input freq)	
Amplitude (V)		Amplitude (V)	
Time Period (ms)		Time Period (ms)	

PROCEDURE:

1. The connections are given as per the circuit diagram.
2. The circuit uses a 4- bit binary counter 7490 used as a divide-by-5 circuit.
3. Measure the free running frequency of VCO at pin 4, with the input signal Vi set equal to zero. Compare it with the calculated value = 0.25 / (RT CT).
4. Now apply the input signal of 1 Vpp square wave at 500 Hz to pin 2.
5. Vary the VCO frequency by adjusting the 20kΩ potentiometer till the PLL is locked. Measure the output frequency. It should be 5 times the input frequency.
6. Repeat steps 4, 5 for input frequency of 1 kHz and 1.5 kHz.

RESULT :

R-2R LADDER TYPE D- A CONVERTER USING OP-AMP

Exp. No :

Date :

AIM:

To construct and test the operation of a 4 bit R – 2R ladder type digital to analog converter using op-amp IC 741

APPARATUS REQUIRED:

Sl. No:	Apparatus Name	Range	Qty.
1	Operational Amplifier	IC 741	2
2	Resistors	10 KΩ 22K	3 6
3	Digital Trainer Kit		1
4	Multimeter		1
5	Connecting Wires		1

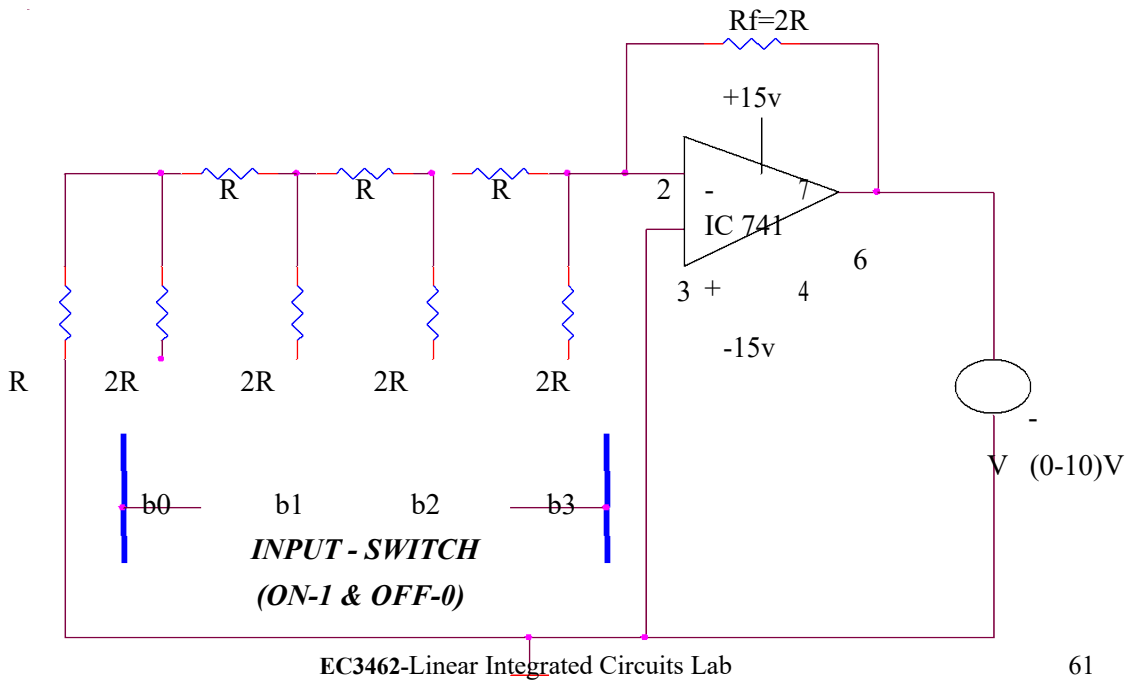
THEORY:

Most DACs architectures are based on the popular R-2R ladder. Starting from the left hand side of the circuit to the right hand side, one can easily prove that the equivalent resistance to the right of each labeled node equals 2R. Consequently, the current flowing downward, away from each node equal to the current flowing toward the right; twice this current enters the node from the left. The currents and, hence, the node voltages are binary weighted.

With a resistance spread of only 2-to-1, R-2R ladders can be fabricated monolithically to a high degree of accuracy and stability. Depending on how ladders are used, there were many DAC architectures available. There were two common types of R-2R DACs available based on current or voltage.

They are Current mode DAC and Voltage mode DAC based on whether the circuit operated on current or voltage respectively. The major advantage of R-2R ladder architecture when compared with the binary weighted type is the use of only two value resistors. These two values R and 2R make the design simple for any resolution and thus easily realizable as an integrated circuit.

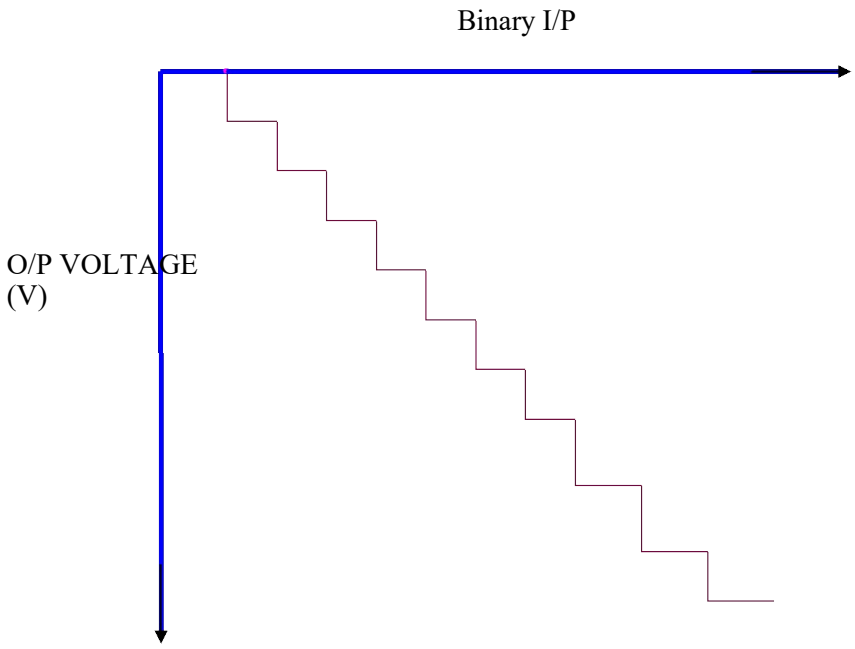
CIRCUIT DIAGRAM:



TABULATION:

DECIMAL	EQUIVALENT BINARY				PRACTICAL VOLTAGE	THEORTICAL VOLTAGE
	b_0	b_0	b_0	b_0		
0						
1						
2						
3						
4						
5						
6						
7						
8						
9						
10						
11						
12						
13						
14						

MODEL GRAPH:



DESIGN PROCEDURE:

1. Assume any value of R & find 2R.
2. Let R = 10KΩ; therefore 2R = 20KΩ ≡ 22KΩ.
3. Let R_f = 2R = 22KΩ.

PROCEDURE:

- Select the given resolution as $2^4 = 16$.
- Assume the value of Resistor R and thus select another resistor with twice a value of the first resistor (2R).
- Connect the circuit as shown in the circuit diagram. Connect the series resistances R finally to the inverting terminal of the op-amp.
- Connect the other end of the parallel arm resistors 2R to the digital switch to represent binary logic conditions.
- Calculate the output voltage from the voltmeter. Since negative output results from op-amp connect the output of op-amp to the negative terminal of the voltmeter, to get Positive deflections.
- Plot the graph for output voltage versus input binary combinations.

RESULT:

CYCLE III
SIMULATION LAB

STUDY OF PSPICE

INTRODUCTION OF PSPICE:

Spice is a powerful general purpose analog and mixed mode circuit simulator that is used to verify circuit design and to predict the circuit behavior. This is of particular importance for integrated circuit. It was for this reason that spice was originally developed at the electronics research laboratory of the university of California, Berkeley (1975), as its name implies.

Simulation program for integrated circuits emphasis. The pspice light version has the following limitation. Circuits have a maximum of 64 nodes, 10 transistor and 2 op-amp.

Spice can do several types of circuit analysis.

Non- linear DC analysis : Calculate the DC transfer curve

Non-linear transient and fourier analysis : Calculate the voltage and current as a function of time when a large signal is applied; fourier analysis gives the frequency spectrum.

Linear AC Analysis: calculate the output as a function of frequency. A bode plot is generated.

Noise analysis.

Parametric analysis

Monte carlo analysis

In addition, pspice has analog and digital libraries standard components such as NAND, NOR, Flip Flo, Multiplexer, FPGA, PLDs and many more digital component this makes it a useful tool for a wide range of analog and digital application.

MODELING DEVICES AND ELEMENT:

A model that specifies a set of parameter for an element can be generated in pspice using the .MODEL command.

.MODEL MNAME TYPE (P1=A1 P2=A2 P3=A3…) PN=AN

[<tolerance specifications>]

EX : .MODEL QMOD NPN (BF=50 IS = 1E-9)

BIPOLAR MODEL PARAMETERS FOR BJT

NAME	MODEL PARAMAETERS	UNIT	DEFAULT	
IS	PN saturation current	A	1E-16	
BF	Ideal max. forward beta		100	
BR	Ideal max. Reverse beta resistance (base spreading resistance)	Ω		
RE	Emitter ohmic resistance			
RC	Collector ohmic resistance & collector lead and bulk resistance			
TF	Ideal forward transist time			
TR	Ideal reverse transit time			

PSPICE / SPICE COMMANDS:

COMMAND	ANALYSIS OR FUNCTION
	Absolute value operator
.AC	AC / frequency analysis
.OP	DC operating point
.DC	Dc sweep
DIF	Different Operator
.ENDS	End of subcircuits
.FUNC	Function definition
.GLOBAL	Global nodes
.PROBE	Graphics post-processor
.INC	Include file
.IC	Initial condition
.LIB	Library file
.MODEL	Model definition
.MULTI	Multiplier (operator)
.NODEST	Node setting
.OPTIONS	Options
.NOISE	Noise analysis
.STEP	Parameter analysis
.PLOT	Plot output
.PRINT	Print output
.PROBE	Probe
.SUBCKT	Subcircuit definition
.TF	Transfer function
.TRAN	Transient analysis
.VALUE	Value

I .CREATING NETLIST:

Once a schematic is drawn, create a netlist to use with other pspice / spice software application. After drawing schematic, choose create netlist from the analysis menu.

EXAMPLE:

C 0 1 10UF	C is connected between node 0 and 1
L 2 1 50UH	L is connected between nodes 2 and 1
R 3 2 1K	R is connected between nodes 3 and 2
VS 3 0 ac 1v	VS is connected between nodes 3 and 0
+Pulse 0 1V 0 1ns 0.5ms 1ms	pulse voltage specification

Analysis description for both AC and pulse source

.AC DEC 10 100HZ 100KHZ ;	AC analysis from 100hz to 100khz
.TRAN 10ns 0.5ms;	Transient analysis from 0 to 0.5ms
.PROBE;	Graphics post-processor
.END;	This is the last line and must always be included.

II. Pspice with OrCAD Capture

Before one can simulate a circuit one needs to specify the circuit configuration. This can be done in a variety of ways. One way is to enter the circuit description as a text file in terms of the elements, connections, the models of the elements and the type of analysis. This file is called the SPICE input file or source file .

An alternative way is to use a schematic entry program such as OrCAD CAPTURE. Capture is a user-friendly program that allows you to capture the schematic of the circuits and to specify the type of simulation. Capture is non only intended to generate the input for PSpice but also for PCD layout design programs.

Step 1: Circuit Creation with Capture

- Create a new Analog, mixed AD project
- Place circuit parts
- Connect the parts
- Specify values and names

Step 2: Specify type of simulation

- Create a simulation profile
- Select type of analysis: o Bias, DC sweep, Transient, AC sweep
- Run Pspice

Step 3: View the results

- Add traces to the probe window
- Use cursors to analyze waveforms
- Check the output file, if needed
- Save or print the results

The values of elements can be specified using scaling factors (upper or lower case):

T or Tera (= 1E12);

G or Giga (= E9);

MEG or Mega (= E6);

K or Kilo (= E3);

M or Milli (= E-3);

U or Micro (= E-6);

N or Nano (= E-9);

P or Pico (= E-12)

F of Femto (= E-15)

Both upper and lower case letters are allowed in Pspice and HSpice. As an example, one can specify a capacitor of 225 picofarad in the following ways:

225P, 225p, 225pF; 225pFarad; 225E-12; 0.225N

Notice that Mega is written as MEG, e.g. a 15 megaOhm resistor can be specified as 15MEG, 15MEGohm, 15meg, or 15E6. Be careful not to use M for Mega! When you write 15Mohm or 15M, Spice will read this as 15 milliOhm!

We'll illustrate the different types of simulations for the following circuit:

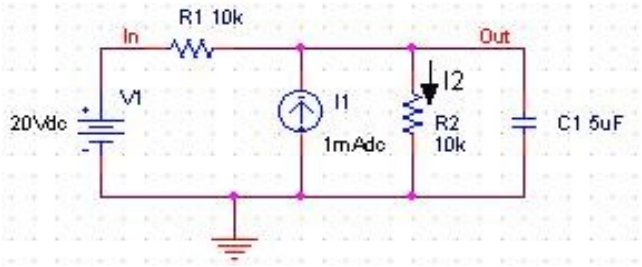


Figure 1: Circuit to be simulated (screen shot from OrCAD Capture).

2.1 Step 1: Creating the circuit in Capture

2.1.1 Create new project:

1. Open OrCAD Capture

2. Create a new Project: FILE MENU/NEW_PROJECT

3. Enter the name of the project

4. Select Analog or Mixed-AD

5. When the Create Pspice Project box opens, select "Create Blank Project".

A new page will open in the Project Design Manager as shown below.

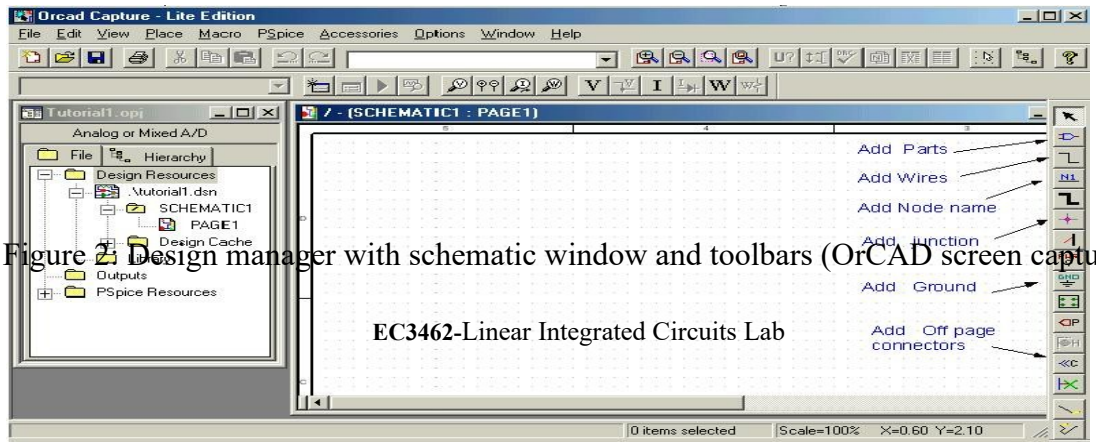


Figure 2: Design manager with schematic window and toolbars (OrCAD screen capture)

2.1.2. Place the components and connect the parts

1. Click on the Schematic window in Capture.

2. To Place a part go to PLACE/PART menu or click on the Place Part Icon. This will open a dialog box shown below.

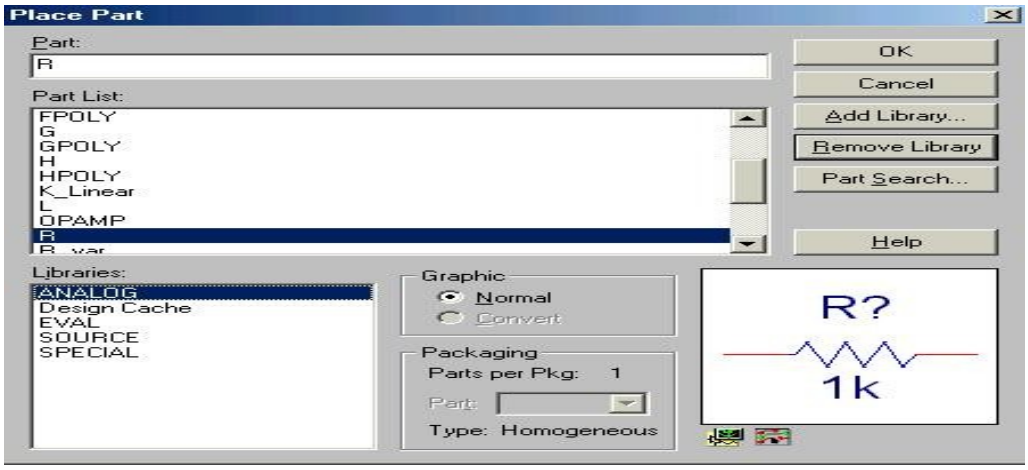


Figure 3: Place Part window

3. Select the library that contains the required components. Type the beginning of the name in the Part box. The part list will scroll to the components whose name contains the same letters. If the library is not available, you need to add the library, by clicking on the Add Library button. This will bring up the Add Library window. Select the desired library. For Spice you should select the libraries from the apture/Library/Pspice folder.

Analog: contains the passive components (R,L,C), mutual inductane, transmission line, and voltage and current dependent sources (voltage dependent voltage source E, current-dependent current source F, voltage-dependent current source G and current-dependent voltage source H).

Source: give the different type of independent voltage and current sources, such as Vdc, Idc, Vac, Iac, Vsin, Vexp, pulse, piecewise linear, etc. Browse the library to see what is available.

Eval: provides diodes (D…), bipolar transistors (Q…), MOS transistors, JFETs (J…), real opamp such as the u741, switches (SW_tClose, SW_tOpen), various digital gates and components.

Abm: contains a selection of interesting mathematical operators that can be applied to signals, such as multiplication (MULT), summation (SUM), Square Root (SWRT), Laplace (LAPLACE), arctan (ARCTAN), and many more.

Special: contains a variety of other components, such as PARAM, NODESET, etc.

4. Place the resistors, capacitor (from the Analog library), and the DC voltage and current source. You can place the part by the left mouse click. You can rotate the components by

clicking on the R key. To place another instance of the same part, click the left mouse button again. Hit the ESC key when done with a particular element. You can add initial conditions to the capacitor. Double-click on the part; this will open the Property window that looks like a spreadsheet. Under the column, labeled IC, enter the value of the initial condition, e.g. 2V. For our example we assume that IC was 0V (this is the default value).

5. After placing all part, you need to place the Ground terminal by clicking on the GND icon (on the right side toolbar – see Fig. 3). When the Place Ground window opens, select GND/CAPSYM and give it the name 0 (i.e. zero). Do not forget to change the name to 0, otherwise Pspice will give an error or "Floating Node". The reason is that SPICE needs a ground terminal as the reference node that has the node number or name 0 (zero).

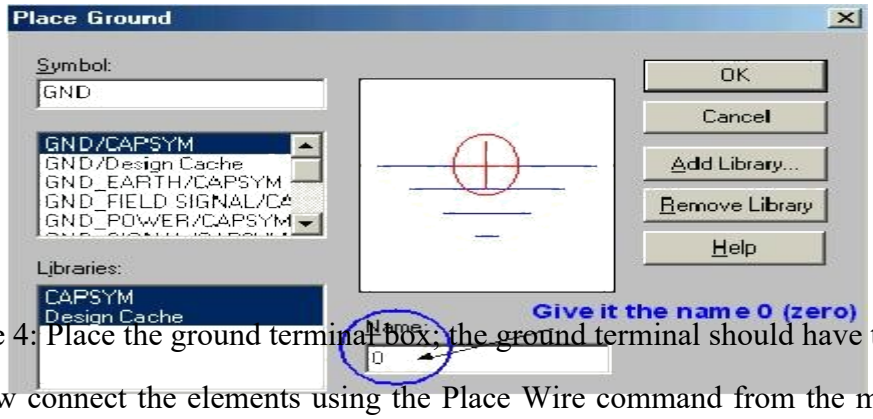


Figure 4: Place the ground terminal box; the ground terminal should have the name 0

6. Now connect the elements using the Place Wire command from the menu (PLACE/WIRE) or by clicking on the Place Wire icon.

7. You can assign names to nets or nodes using the Place Net Alias command (PLACE/NET ALIAS menu). We will do this for the output node and input node. Name these Out and In, as shown in Figure 1.

2.1.3. Assign Values and Names to the parts

1. Change the values of the resistors by double-clicking on the number next to the resistor. You can also change the name of the resistor. Do the same for the capacitor and voltage and current source.

2. If you haven't done so yet, you can assign names to nodes (e.g. Out and In nodes).

3. Save the project

Result :

Hence the study of a pspice was done.

EX.NO:	
DATE:	**TUNED COLLECTOR OSCILLATOR**

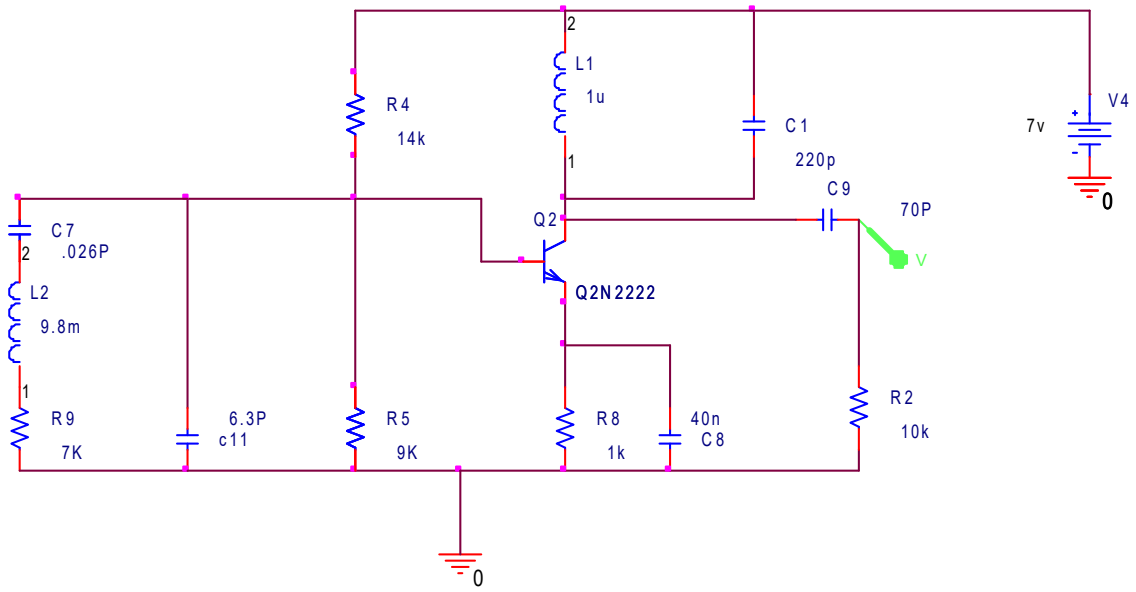
AIM: To simulate a Tuned collector oscillator using PSPICE.

APPARATUS REQUIRED: PSPICE software

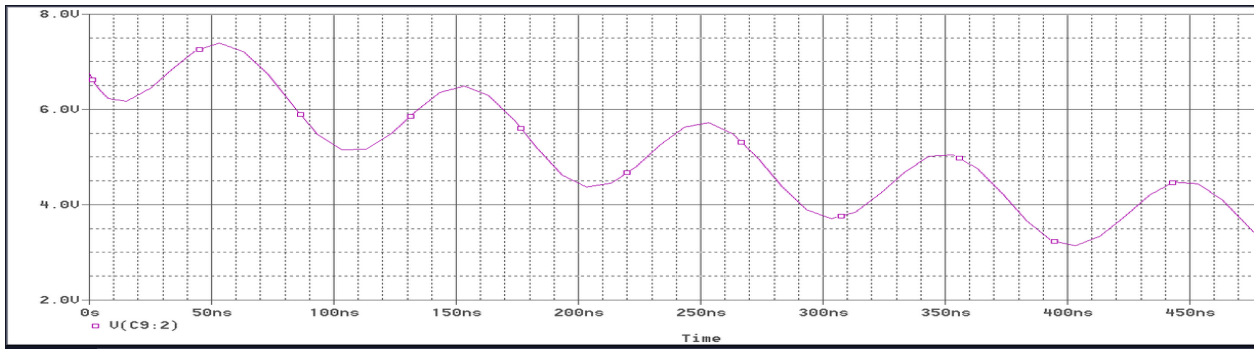
PROCEDURE:

1. Start the program
2. Select the ORCAD release capture
3. Go to new and select project
4. Create the title of the project
5. Drag the elements as per the circuit diagram requirement.
6. Make connections as per the circuit diagram using wire icon.
7. Create the new simulation
8. Set the output level setting.
9. Placed the voltage markers in input and output mode.
10. Run the circuit diagram and print the output.

CIRCUIT DIAGRAM



SIMULATED OUTPUT:



NETLIST: SOURCE TUNED COLLECTOR:

```
Q Q1        N02551 N01986 N02311 Q2N2222
R_R7        0 N01986 1k
V_V4        N02483 0 7v
L_L2        N003180 N006491 9.8m
Q_Q2        N02551 N01986 N02311 Q2N2222
C_C1        N02551 N02483 220p
R_R8        0 N02311 1k
R_R9        0 N003180 7K
R_R2        0 N02696 10k
C_c11       N01986 0 6.3P
R_R3        N01986 N02483 14K
R_R4        N01986 N02483 14k
C_C9        N02551 N02696 70P
C_C6        N01986 N006491 .026P
R_R5        0 N01986 9K
C_C7        N01986 N006491 1n
L_L1        N02551 N02483 1u
R_R6        0 N01986 1k
C_C8        N02311 0 40n
```

RESULT:

Thus the Tuned collector oscillator circuit is simulated using PSPICE and the output waveform is plotted.

EX.NO:	
DATE:	**TWIN T OSCILLATOR**

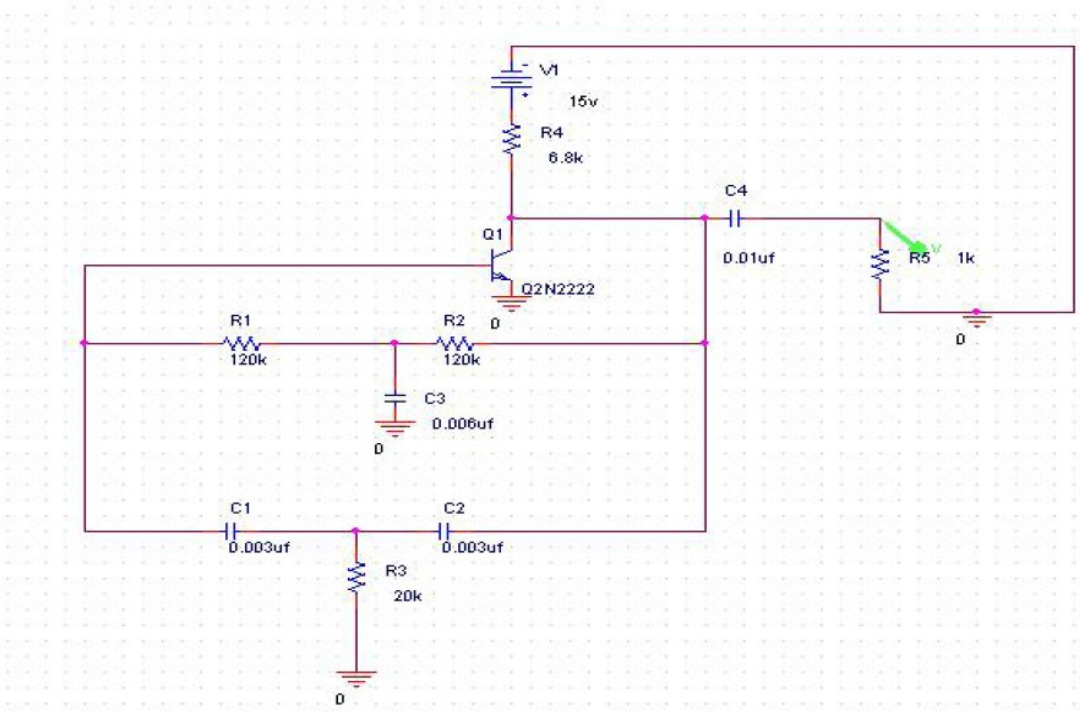
AIM:
To simulate a twin-T oscillation circuit using PSPICE

APPARATUS REQUIRED:
1. PC
2. PSPICE software

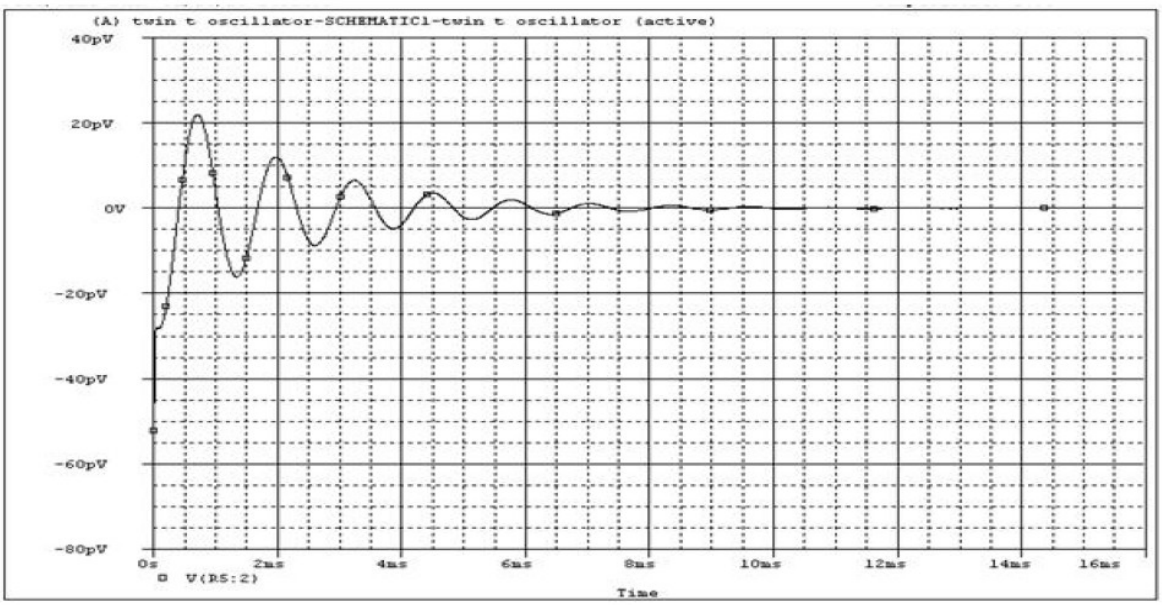
THEORY:
"Twin-T" oscillator uses two "T" RC circuits operated in parallel. One circuit is an R-C-R "T" which acts as a low-pass filter. The second circuit is a C-R-C "T" which operates as a highpass filter. Together, these circuits form a bridge which is tuned at the desired frequency of oscillation. The signal in the C-R-C branch of the Twin-T filter is advanced, in the R-C-R - delayed, so they may cancel one another for frequency $f=12\pi RC$ if $x=2$; if it is connected as a negative feedback to an amplifier, and x>2, the amplifier becomes an oscillator.

PROCEDURE:
1. Click on the start menu and select the Pspice simulation software
2. Select the parts required for the circuit from the parts menu and place them in the work space
3. Connect the parts using wires
4. Save the file and select the appropriate analysis
5. Simulate the circuit and observe the corresponding output waveforms

CIRCUIT DIAGRAM(Twin-T Oscillator)



MODEL GRAPH:



RESULT:

Thus, the twin-T oscillator oscillator circuit is simulated using Pspice.

EX.NO:	WIEN BRIDGE OSCILLATOR
DATE:	

AIM:

To simulate a Wien bridge oscillator using PSPICE.

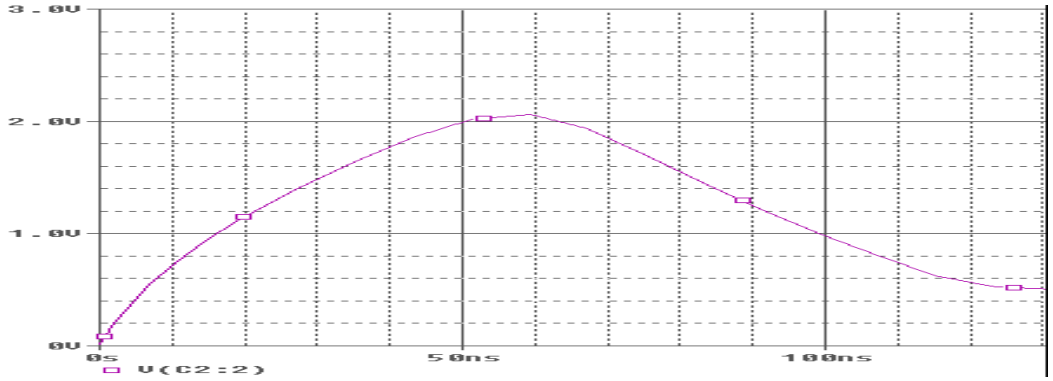
APPARATUS REQUIRED:

PSPICE software

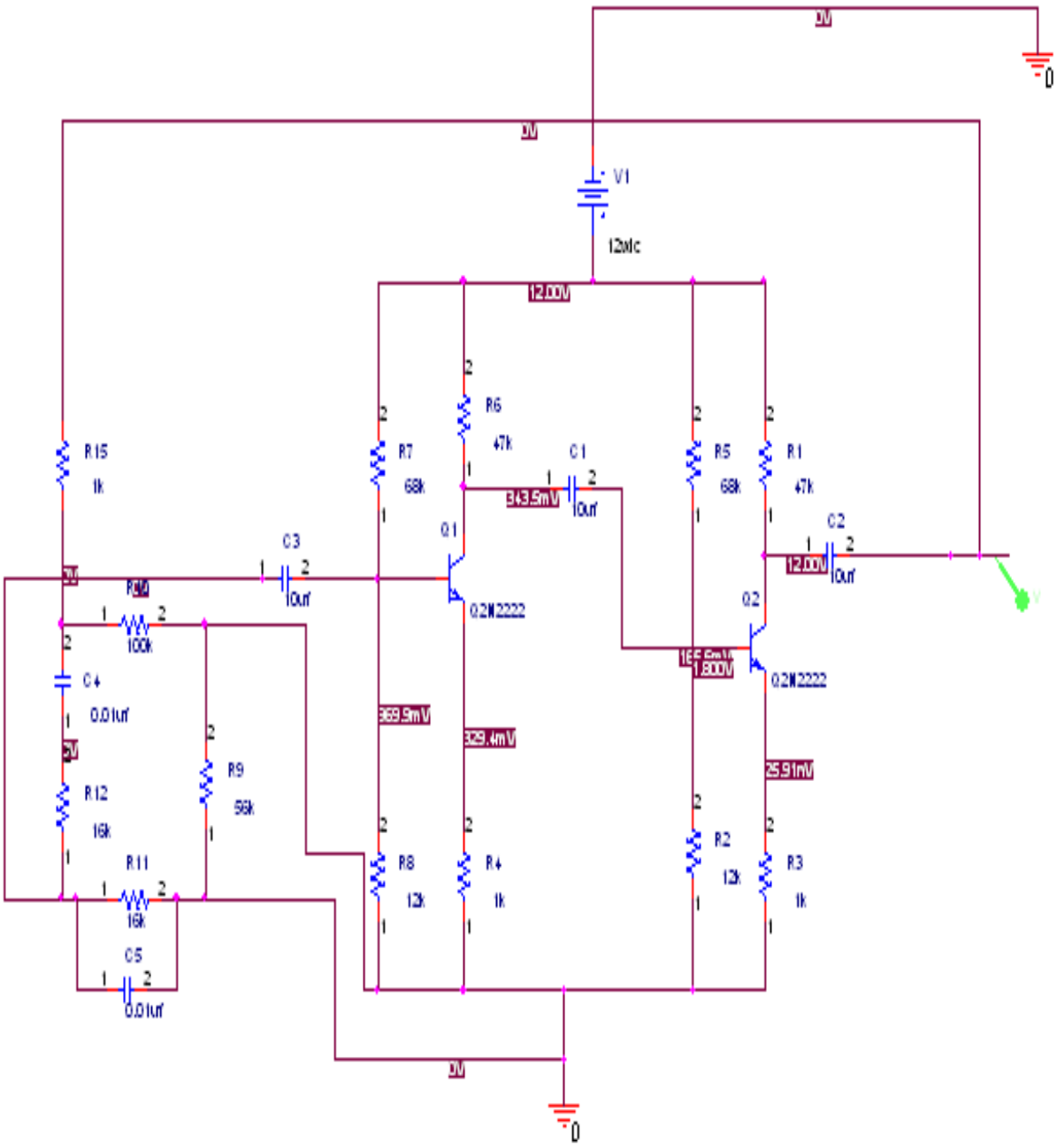
PROCEDURE:

1. Start the program
2. Select the ORCAD release capture
3. Go to new and select project
4. Create the title of the project
5. Drag the elements as per the circuit diagram requirement.
6. Make connections as per the circuit diagram using wire icon.
7. Create the new simulation
8. Set the output level setting.
9. Placed the voltage markers in input and output mode.
10. Run the circuit diagram and print the output.

SIMULATION OUTPUT:



CIRCUIT DIAGRAM:



NETLIST SOURCE WEIN BRIDGE OSCILLATOR:

Q_Q1 N00484 N00513 N00455 Q2N2222
Q_Q2 N00688 N00746 N00717 Q2N2222
R_R5 N00847 N00579 68k
C_C3 N01418 N00513 10uf
R_R6 N00484 N00579 47k
C_C1 N00484 N00746 10uf
C_C4 N01662 N01778 0.01uf

R_R7 N00513 N00579 68k
R_R1 N00688 N00579 47k
R_R10 N01778 0 100k
C_C2 N00688 N01085 10uf
R_R8 0 N00513 12k
V_V1 N00579 0 12vdc
R_R2 0 N00847 12k
R_R15 N01778 N01085 1k
R_R11 N01418 0 16k
R_R9 0 0 56k
R_R3 0 N00717 1k
R_R12 N01418 N01662 16k
R_R4 0 N00455 1k
C_C5 N01418 0 0.01uf

RESULT:

Thus the Wien bridge oscillator circuit is simulated using PSPICE and the output waveform is plotted.

EX.NO:	
DATE:	**DOUBLE AND STAGER TUNED AMPLIFIERS**

AIM:

To simulate a double and stager tuned amplifiers circuit using PSPICE

APPARATUS REQUIRED:

1. PC
2. PSPICE software

THEORY:

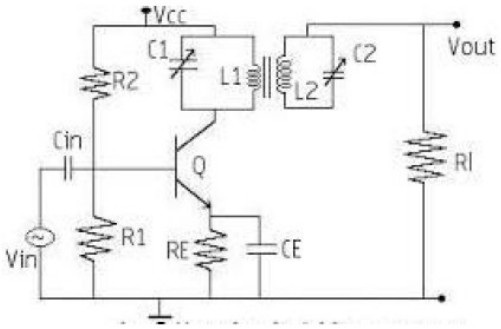
Stagger Tuned Amplifiers are used to improve the overall frequency response of tuned Amplifiers. Stagger tuned Amplifiers are usually designed so that the overall response exhibits maximal flatness around the centre frequency. It needs a number of tuned circuits operating in union. The overall frequency response of a Stagger tuned amplifier is obtained by adding the individual response together. Since the resonant Frequencies of different tuned circuits are displaced or staggered, they are referred as stagger tuned amplifier.

PROCEDURE:

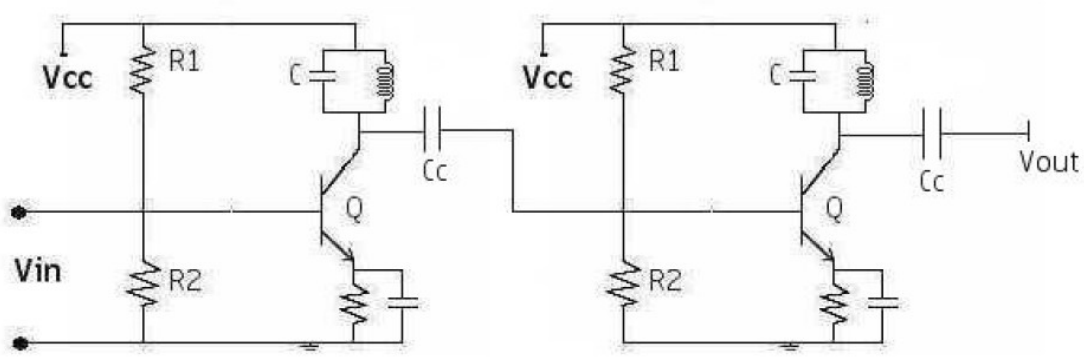
1. Click on the start menu and select the Pspice simulation software
2. Select the parts required for the circuit from the parts menu and place them in the work space
3. Connect the parts using wires
4. Save the file and select the appropriate analysis
5. Simulate the circuit and observe the corresponding output waveforms

CIRCUIT DIAGRAM:

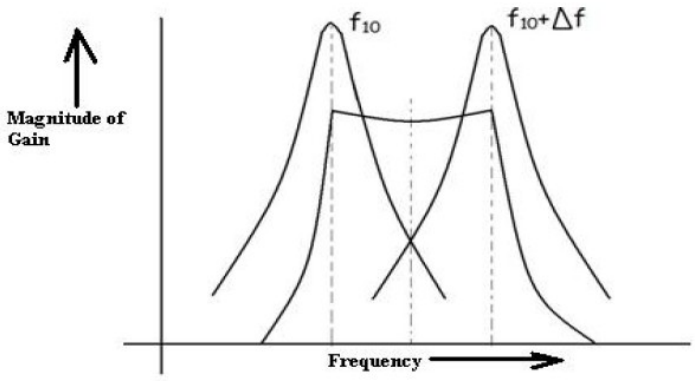
(a) Double tuned Amplifiers



(b) Stager tuned Amplifiers



MODEL GRAPH:



RESULT:

Thus, the double and stager tuned amplifier circuit is simulated using Pspice.

EX.NO:	
DATE:	**BISTABLE MULTIVIBRATOR**

AIM:

To simulate a Bistable Multivibrator using PSPICE.

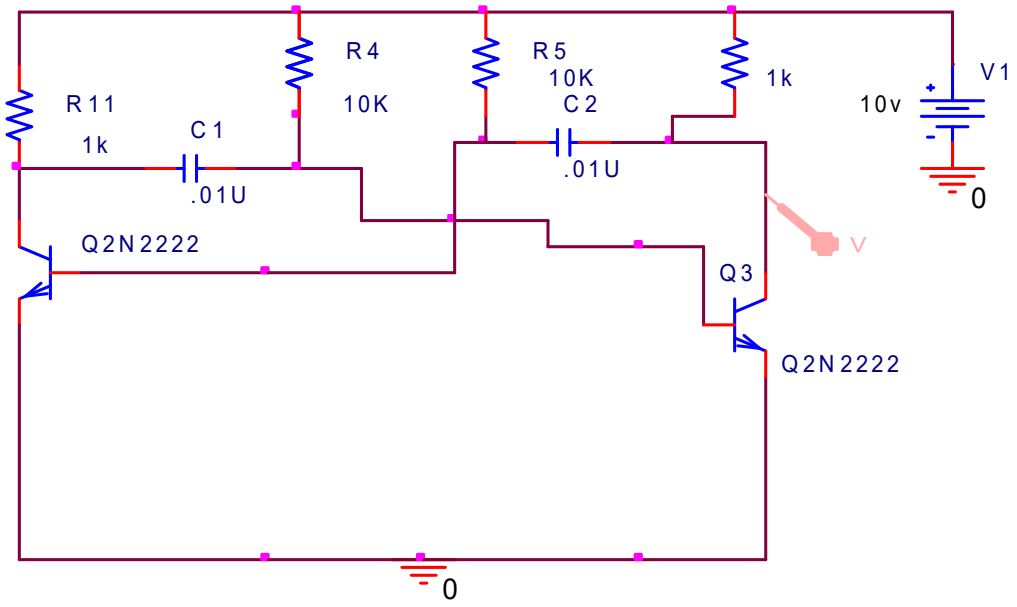
APPARATUS REQUIRED:

PSPICE software

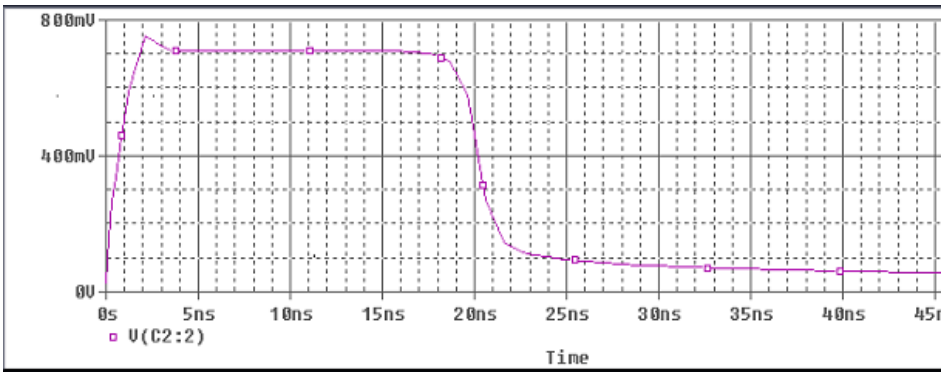
PROCEDURE:

1. Start the program
2. Select the ORCAD release capture
3. Go to new and select project
4. Create the title of the project
5. Drag the elements as per the circuit diagram requirement.
6. Make connections as per the circuit diagram using wire icon.
7. Create the new simulation
8. Set the output level setting.
9. Placed the voltage markers in input and output mode.
10. Run the circuit diagram and print the output.

CIRCUIT DIAGRAM:



SIMULATED OUTPUT:



NETLIST SOURCE BISTABLE:

R_R3 N01818 N02554 10K

R_R4 N01818 N02554 1k

C_C1 N02903 N01818 .01U

Q_Q3 N02667 N01818 0 Q2N2222

C_C2 N01818 N02667 .01U

R_R5 N01818 N02554 10K

R_R6 N02667 N02554 1k

R_R11 N02903 N02554 1k

Q__01U N02903 N01818 0 Q2N2222

V_V1 N02554 0 10v

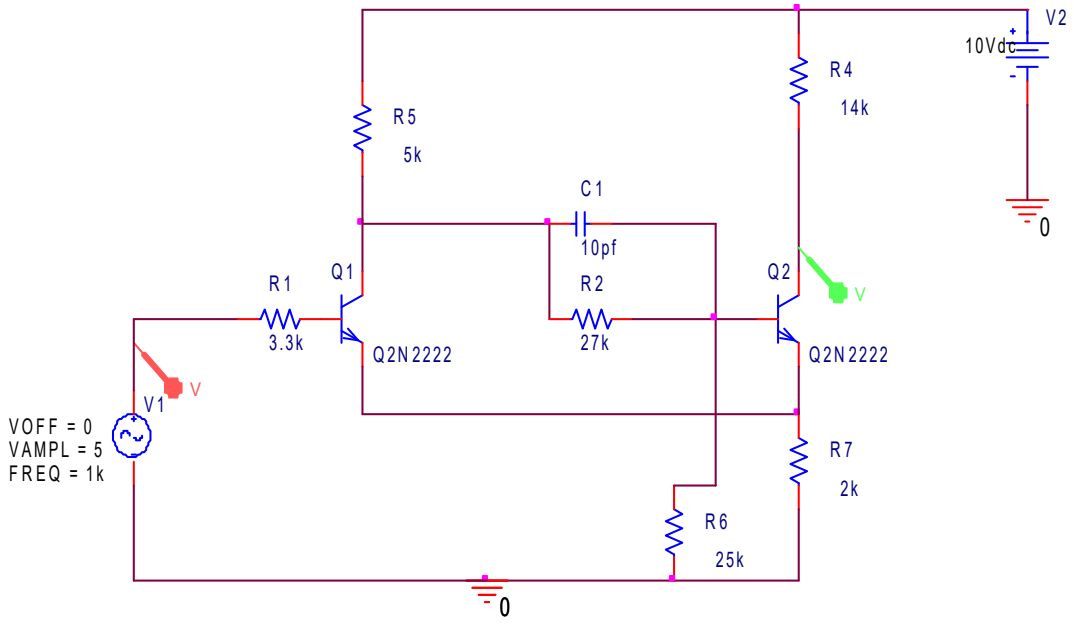
RESULT:

Thus the bistable multivibrator circuit is simulated using PSPICE and the output waveform is plotted.

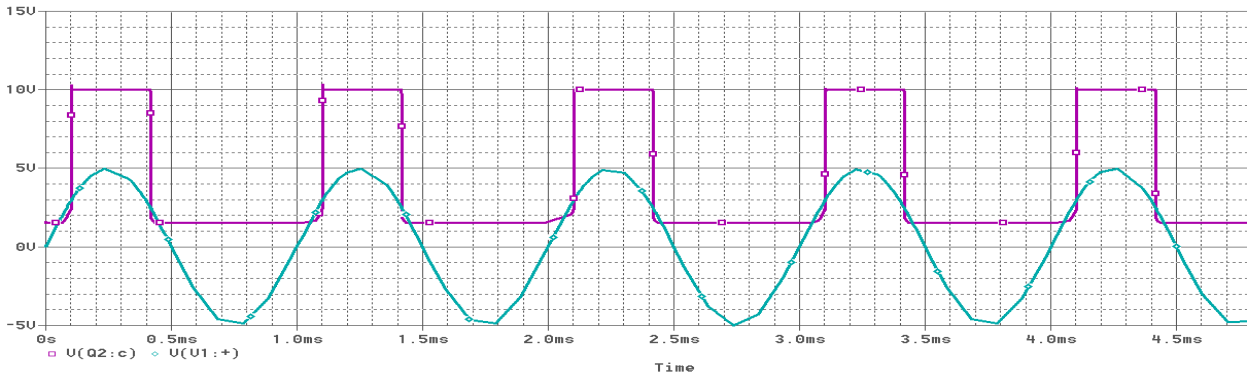
EX.NO:	
DATE:	**SCHMITT TRIGGER**

AIM: To simulate a Schmitt Trigger using PSPICE.
APPARATUS REQUIRED: PSPICE software
PROCEDURE:
1. Start the program
2. Select the ORCAD release capture
3. Go to new and select project
4. Create the title of the project
5. Drag the elements as per the circuit diagram requirement.
6. Make connections as per the circuit diagram using wire icon.
7. Create the new simulation
8. Set the output level setting.
9. Placed the voltage markers in input and output mode.
10. Run the circuit diagram and print the output.

CIRCUIT DIAGRAM:



SIMULATED OUTPUT:



NETLIST SOURCE SCHMITT TRIGGER:

Q_Q1 N00522 N000030 N00825 Q2N2222
Q_Q2 N00796 N00708 N00825 Q2N2222
R_R1 N00484 N000030 3.3k
C_C1 N00522 N00708 10pf
R_R2 N00522 N00708 27k
V_V1 N00484 0 +SIN 0 5 1k 0 0 0
R_R4 N00796 N00551 14k
V_V2 N00551 0 10Vdc
R_R5 N00522 N00551 5k
R_R6 0 N00708 25k
R_R7 0 N00825 2k

RESULT:

Thus the Schmitt Trigger circuit is simulated using PSPICE and the output waveform is plotted.

EX.NO:	
DATE:	**MONOSTABLE MULTIVIBRATOR**

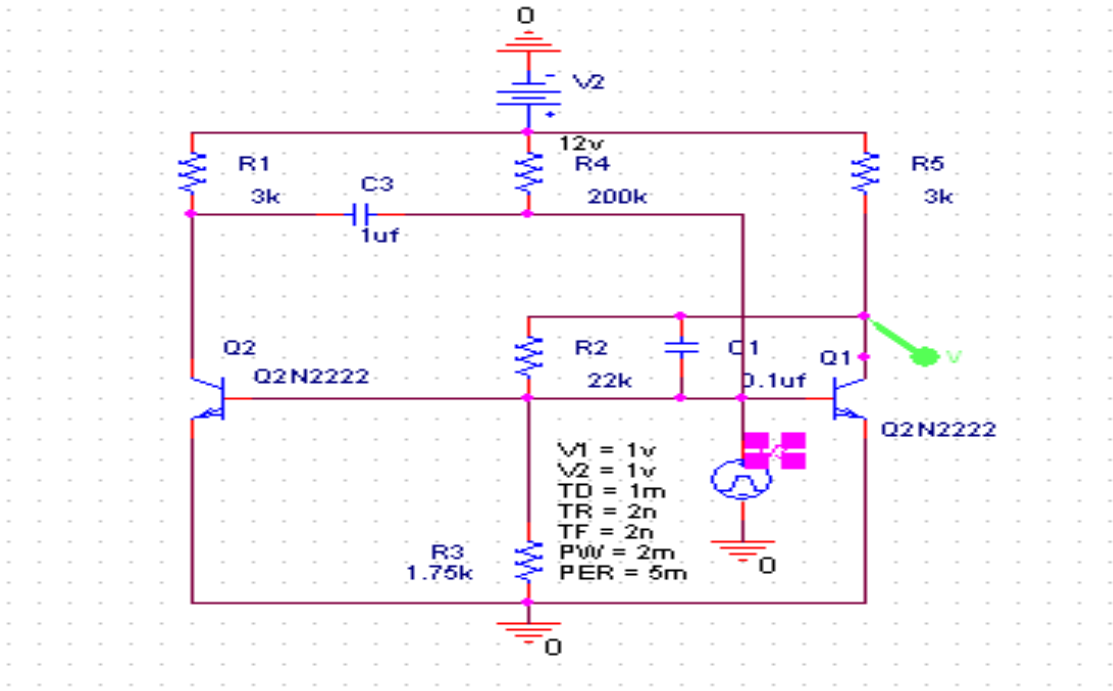
AIM : To simulate a Monostable multivibrator using PSPICE.

APPARATUS REQUIRED: PSPICE software

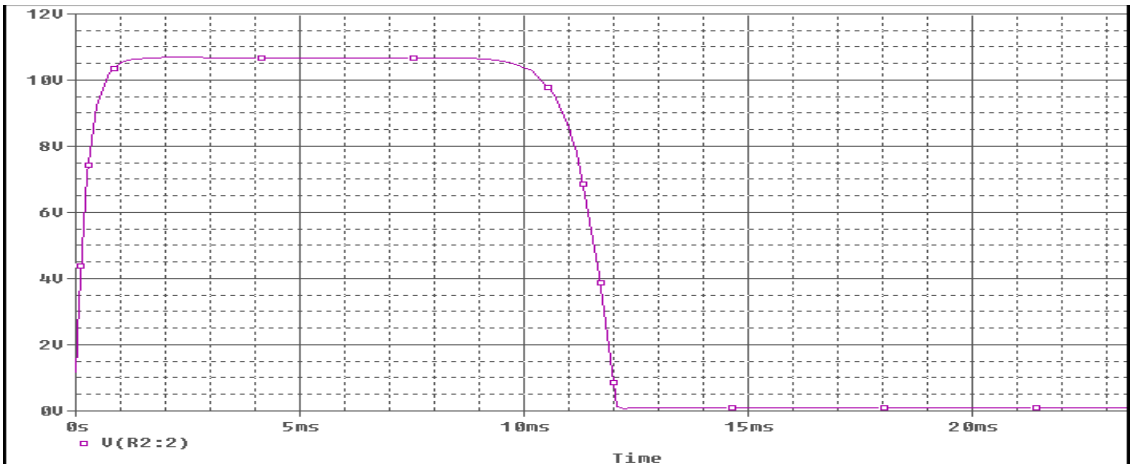
PROCEDURE:

1. Start the program
2. Select the ORCAD release capture
3. Go to new and select project
4. Create the title of the project
5. Drag the elements as per the circuit diagram requirement.
6. Make connections as per the circuit diagram using wire icon.
7. Create the new simulation
8. Set the output level setting.
9. Placed the voltage markers in input and output mode.
10. Run the circuit diagram and print the output.

CIRCUIT DIAGRAM:



SIMULATED OUTPUT:



NETLIST SOURCE MONOSTABLE:

Q_Q1 N00381 N00434 0 Q2N2222
C_C3 N00236 N00434 1uf
Q_Q2 N00236 N00265 0 Q2N2222
R_R1 N00236 N00591 3k
V_V2 N00591 0 12v
R_R2 N00265 N00381 22k
R_R3 0 N00265 1.75k
R_R4 N00434 N00591 200k
R_R5 N00381 N00591 3k
V_V3 N00265 0 +PULSE 1v 1v 1m 2n 2n 2m 5m
C_C1 N00265 N00381 0.1uf

RESULT:

Thus the monostable multivibrator circuit is simulated using PSPICE and the output waveform is plotted.

EX.NO:	
DATE:	**VOLTAGE TIME BASE GENERATOR**

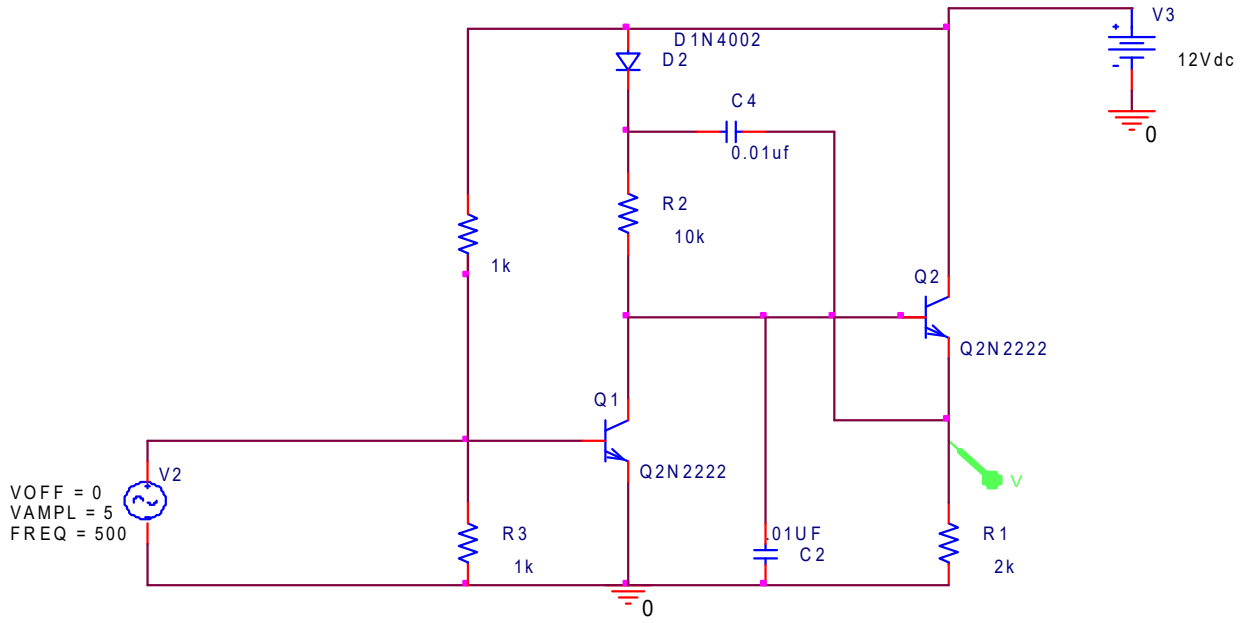
AIM : To simulate a voltage time base generator using PSPICE.

APPARATUS REQUIRED: PSPICE software

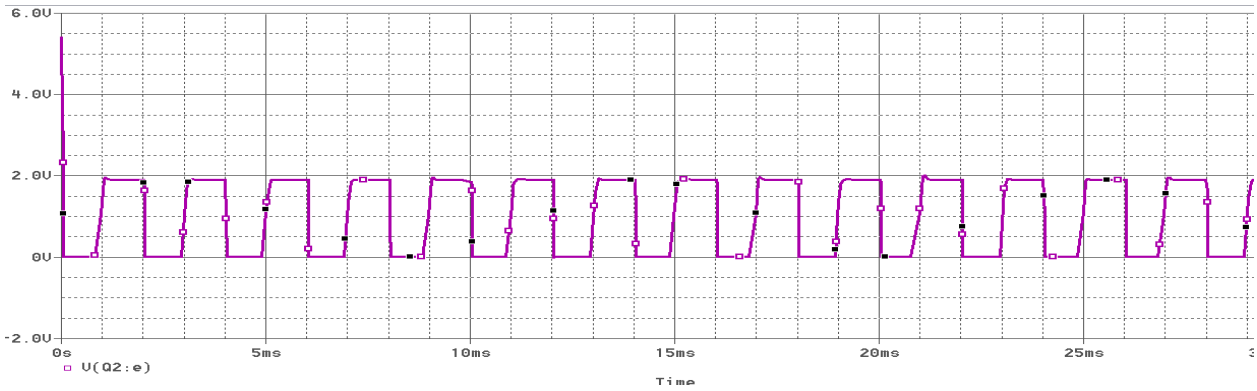
PROCEDURE:

1. Start the program
2. Select the ORCAD release capture
3. Go to new and select project
4. Create the title of the project
5. Drag the elements as per the circuit diagram requirement.
6. Make connections as per the circuit diagram using wire icon.
7. Create the new simulation
8. Set the output level setting.
9. Placed the voltage markers in input and output mode.
10. Run the circuit diagram and print the output.

CIRCUIT DIAGRAM:



SIMULATED OUTPUT:



NETLIST SOURCE VOLTAGE TIME BASE GENERATOR:

Q_Q1 N00852 N00575 0 Q2N2222

C_C2 0 N00852 .01UF

R_R1 0 N00852 2k

R_R2 N00852 N00822 10k

Q_Q2 N00631 N00852 N00852 Q2N2222

V_V3 N00631 0 12Vdc

R_R3 0 N00575 1k

C_C4 N00822 N00852 0.01uf

R_R4 N00575 N00631 1k

D_D2 N00631 N00822 D1N4002

V_V2 N00575 0

+SIN 0 5 500 0 0 0

RESULT:

Thus the voltage time base generator circuit is simulated using PSPICE and the output waveform is plotted.

EX.NO:	
DATE:	**CLASS-C TUNED AMPLIFIER**

AIM :

To simulate a class-c tuned amplifier using PSPICE.

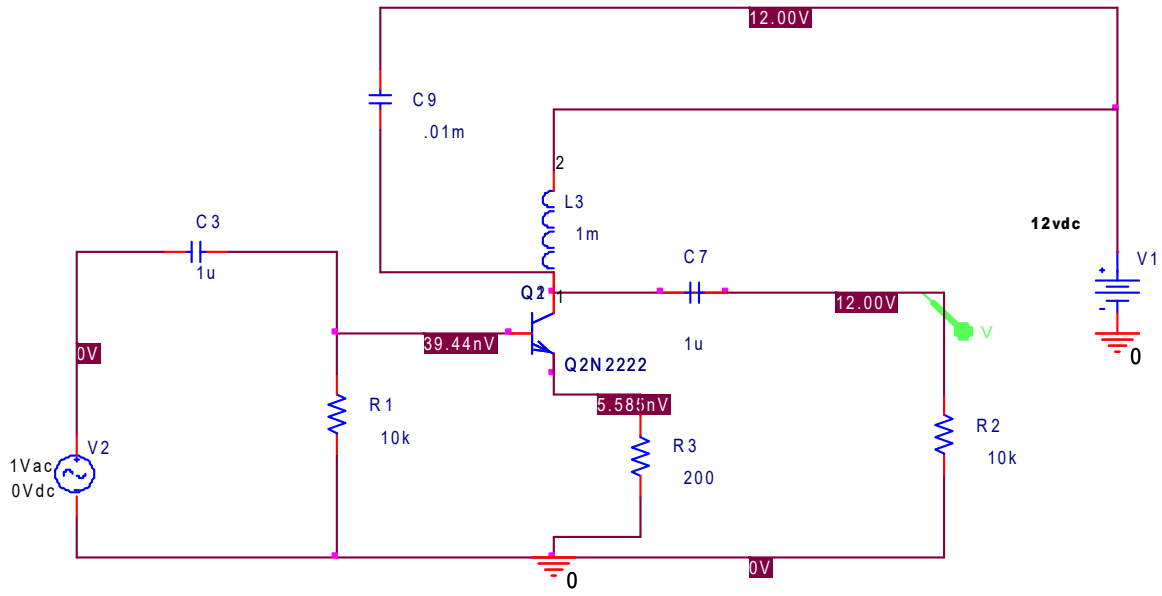
APPARATUS REQUIRED:

PSPICE software

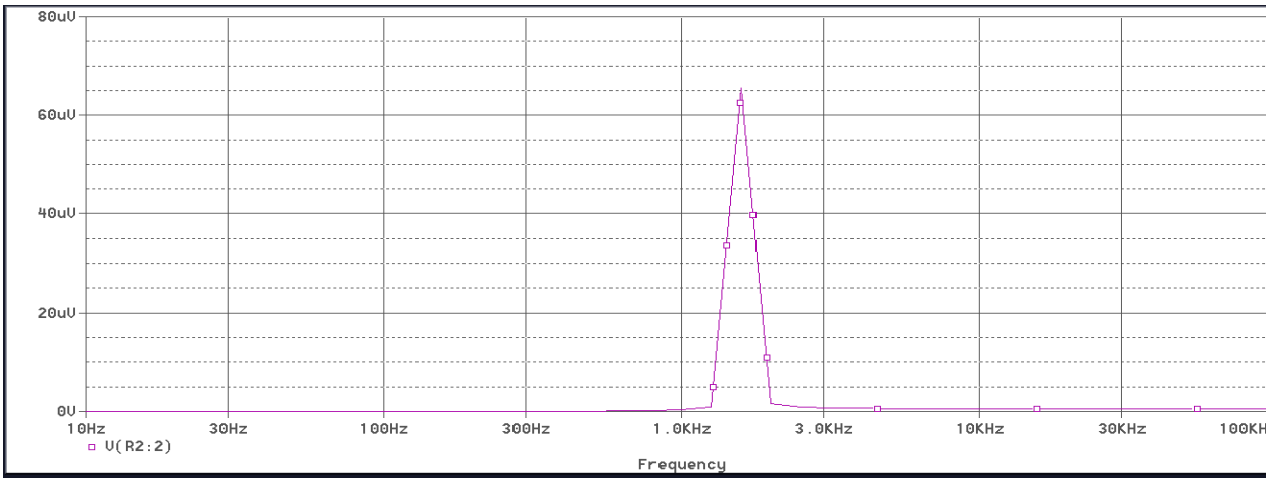
PROCEDURE:

1. Start the program
2. Select the ORCAD release capture
3. Go to new and select project
4. Create the title of the project
5. Drag the elements as per the circuit diagram requirement.
6. Make connections as per the circuit diagram using wire icon.
7. Create the new simulation
8. Set the output level setting.
9. Placed the voltage markers in input and output mode.
10. Run the circuit diagram and print the output.

CIRCUIT DIAGRAM:



SIMULATED OUTPUT:



NETLIST: SOURCE CLASS C TUNED AMPLIFIER:

Q_Q1 N01783 N01693 N02178 Q2N2222
R_R2 0 N01783 10k
C_C9 N01847 N01783 .01m
Q_Q2 N01783 N01693 N02178 Q2N2222
R_R1 0 N01693 10k
C_C3 N02718 N01693 1u
V_V1 N01847 0 12vdc
V_V2 N02718 0 DC 0Vdc AC 1Vac
R_R3 N02178 0 200
L_L3 N01783 N01847 1m
C_C7 N01783 N01783 1u

RESULT:

Thus the class-c tuned amplifier circuit is simulated using PSPICE and the output waveform is plotted.