JEPPIAAR
ENGINEERING COLLEGE

JEPPIAAR NAGAR, CHENNAI – 600119

2021 REGULATION

DEPARTMENT OF ELECTRONICS & COMMUNICATION ENGINEERING.

EC3361 ELECTRONICS DEVICES CIRCUITS ANALYSIS LABORATORY

(B.E III Semester Batch 2023-2027)

(Section A&B)

JEPPIAAR ENGINEERING COLLEGE

JEPPIAAR EDUCATIONAL TRUST

JEPPIAAR NAGAR

RAJIV GANDHI SALAI, CHENNAI-600 119

This is a certified Bonafide Record Book of……..

Register Number……

Submitted for the Anna University practical Examination held on……in.....laboratory during the year …..… to ……

Signature of the Lab-in-charge HOD/ECE

EXAMINERS:

Date…….. **Internal**……

External……

COURSE OBJECTIVES

- To learn the characteristics of PN Junction diode and Zener diode.
- To understand the operation of rectifiers and filters.
- To study the characteristics of amplifier.

S.NO	LIST OF EXPERIMENTS
1	Characteristics of PN Junction Diode and Zener diode.
2	Full Wave Rectifier with Filters.
3	Design of Zener diode Regulator.
4	Common Emitter input-output Characteristics.
5	MOSFET Drain current and Transfer Characteristics.
6	Frequency response of CE and CS amplifiers.
7	Frequency response of CB and CC amplifiers.
8	Frequency response of Cascode Amplifier
9	CMRR measurement of Differential Amplifier
10	Class A Transformer Coupled Power Amplifier.

COURSE OUTCOMES

Upon completion of this course, the students will be able to:

CO1	Characteristics of PN Junction Diode and Zener diode.
CO2	Design and Testing of BJT and MOSFET amplifiers.
CO3	Analyze the Operation of power amplifiers..
CO4	Analyze the performance of various amplifier and oscillator circuits using hardware and circuit simulation tools..
CO5	Demonstrate teamwork and effective communication by documenting experimental procedures, observations, and results systematically.

EC3361-ELECTRONICS DEVICES CIRCUITS AND LABAROTORY
CO PO PSO MATRIX

CO	PO1	PO2	PO3	PO4	PO5	PO6	PO7	PO8	PO9	PO10	PO11	PO12	PSO1	PSO2	PSO3
1	2	2	3	3	2	1	-	-	-	-	-	1	2	1	1
2	2	2	3	3	2	1	-	-	-	-	-	1	2	1	1
3	2		2		1	1	-	-	-	-	-	1	2	1	1
4	-	-	-	-	3	1	-	-	-	-	-	1	2	1	1
5	-	-	-	-	2	1	-	-	-	-	-	1	2	1	1
CO	**2**	**2**	2.6	**3**	**2**	**1**	-	-	-	-	-	**1**	**2**	**1**	**1**

JEPPIAAR ENGINEERING COLLEGE		
Vision of the Institute	To build Jeppiaar Engineering College as an institution of academic excellence in technological and management education to become a world class University	
Mission of the Institute	**M1**	To excel in teaching and learning, research and innovation by promoting the principles of scientific analysis and creative thinking
	M2	To participate in the production, development and dissemination of knowledge and interact with national and international communities.
	M3	To equip students with values, ethics and life skills needed to enrich their lives and enable them to meaningfully contribute to the progress of society
	M4	To prepare students for higher studies and lifelong learning, enrich them with the practical and entrepreneurial skills necessary to excel as future professionals and contribute to Nation's economy
DEPARTMENT: ELECTRONICS AND COMMUNICATION ENGINEERING		
Vision of the Department	To become a centre of excellence to provide quality education and produce creative engineers in the field of Electronics and Communication Engineering to excel at international level.	
Mission of the Department	**M1**	Inculcate creative thinking and zeal for research to excel in teaching-learning process
	M2	Create and disseminate technical knowledge in collaboration with industries
	M3	Provide ethical and value based education by promoting activities for the betterment of the society
	M4	Encourage higher studies, employability skills, entrepreneurship and research to produce efficient professionals thereby adding value to the nation's economy

PROGRAM OUTCOMES (PO)	**PO 1**	**Engineering knowledge**: **Apply** the knowledge of mathematics, science, engineering fundamentals, and an engineering specialization to the solution of complex engineering problems.
	PO 2	**Problem analysis**: **Identify, formulate, review** research literature, and **analyze** complex engineering problems reaching substantiated conclusions using first principles of mathematics, natural sciences, and engineering sciences.
	PO 3	**Design/development of solutions**: **Design solutions** for complex engineering problems and **design** system components or processes that meet the specified needs with appropriate consideration for the public health and safety, and the cultural, societal, and environmental considerations
	PO 4	**Conduct investigations of complex problems**: **Use** research-based knowledge and research methods including **design** of experiments, **analysis** and **interpretation** of data, and **synthesis** of the information to provide valid conclusions.
	PO 5	**Modern tool usage**: **Create**, **select**, and **apply** appropriate techniques, resources, and modern engineering and IT tools including prediction and modeling to complex engineering activities with an understanding of the limitations.
	PO 6	**The engineer and society**: **Apply** reasoning informed by the contextual knowledge to assess societal, health, safety, legal and cultural issues and the consequent responsibilities relevant to the professional engineering practice.
	PO 7	**Environment and sustainability**: **Understand** the impact of the professional engineering solutions in societal and environmental contexts, and **demonstrate** the knowledge of, and need for sustainable development.
	PO 8	**Ethics**: **Apply** ethical principles and commit to professional ethics and responsibilities and norms of the engineering practice.
	PO 9	**Individual and team work**: **Function effectively** as an individual, and as a member or leader in diverse teams, and in multidisciplinary settings.

	PO 10	**Communication**: **Communicate effectively** on complex engineering activities with the engineering community and with society at large, such as, being able **to comprehend** and **write** effective reports and **design** documentation, **make** effective presentations, and **give** and **receive** clear instructions.
	PO 11	**Project management and finance**: **Demonstrate** knowledge and understanding of the engineering and management principles and **apply** these to one's own work, as a member and leader in a team, to **manage** projects and in multidisciplinary environments.
	PO 12	**Life-long learning**: **Recognize** the need for, and have the preparation and ability to **engage** in independent and life-long learning in the broadest context of technological change.
PROGRAM EDUCATIONAL OBJECTIVES (PEOS)	**PEO I**	Produce technically competent graduates with a solid foundation in the field of Electronics and Communication Engineering with the ability to analyze, design, develop, and implement electronic systems.
	PEO II	Motivate the students for choosing the successful career choices in both public and private sectors by imparting professional development activities.
	PEO III	Inculcate the ethical values, effective communication skills and develop the ability to integrate engineering skills to broader social needs to the students.
	PEO IV	Impart professional competence, desire for lifelong learning and leadership skills in the field of Electronics and Communication Engineering.
PROGRAM SPECIFIC OUTCOMES (PSOs)	**PSO 1**	Design, develop and analyze electronic systems through application of relevant electronics, mathematics and engineering principles.
	PSO 2	Design, develop and analyze communication systems through application of fundamentals from communication principles, signal processing, and RF System Design & Electromagnetics.
	PSO 3	Adapt to emerging electronics and communication technologies and develop innovative solutions for existing and newer problems.

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S.No	Date	Name of the Experiment	Page No	Date of submission	Mark	Sign

LIST OF EXPERIMENTS

EC3361 - ELECTRONIC DEVICES AND CIRCUITS LABORATORY

1. Characteristics of PN Junction Diode and Zener diode.
2. Full Wave Rectifier with Filters.
3. Design of Zener diode Regulator.
4. Common Emitter input-output Characteristics.
5. MOSFET Drain current and Transfer Characteristics.
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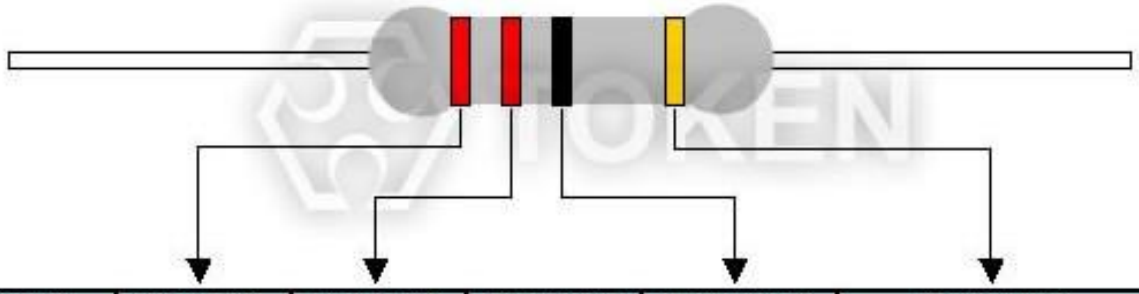
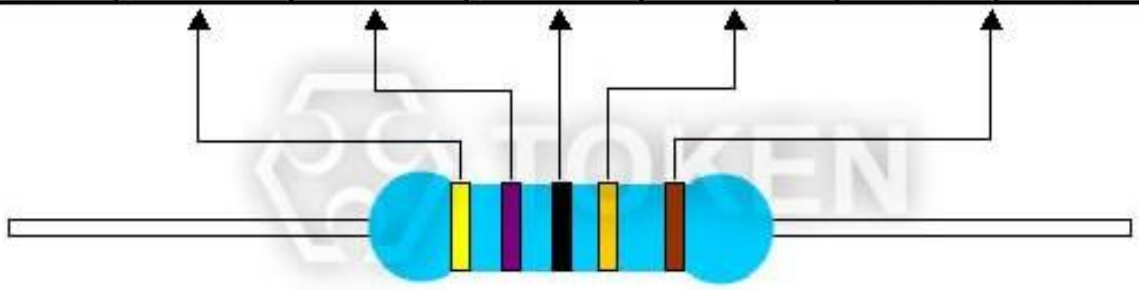
7. Frequency response of CB and CC amplifiers.
8. Frequency response of Cascode Amplifier
9. CMRR measurement of Differential Amplifier
10. Class A Transformer Coupled Power Amplifier.

RESISTOR COLOR CODE



COLOR	1ST BAND	2ND BAND	3TH BAND	MULTIPLIER	TOLERANCE	
BLACK	0	0	0	1		
BROWN	1	1	1	10	± 1%	F
RED	2	2	2	100	± 2%	G
ORANGE	3	3	3	1K		
YELLOW	4	4	4	10K		
GREEN	5	5	5	100K	± 0.5%	D
BLUE	6	6	6	1M	± 0.25%	C
VIOLET	7	7	7	10M	± 0.10%	B
GREY	8	8	8		± 0.05%	A
WHITE	9	9	9			
GOLD				0.1	± 5%	J
SILVER				0.01	± 10%	K
PLAIN					± 20%	M



Ex.No: 1. CHARACTERISTICS OF PN JUNCTION DIODE & ZENER DIODE

Ex.No: (1A) CHARACTERISTICS OF PN JUNCTION DIODE

AIM:

To study the PN junction diode characteristics under Forward & Reverse bias conditions.

APPARATUS REQUIRED:

S.No.	Name	Range	Type	Qty
1	R.P.S	(0-30)V		1
2	Ammeter	(0–30)mA		1
		(0-500)µA		1
3	Voltmeter	(0–1)V		1
		(0-10)V		1

COMPONENTS REQUIRED:

S.No.	Name	Range	Type	Qty
1	Diode	IN4007		1
2	Resistor	1kΩ		1
3	Bread Board			1
4	Wires			

THEORY:

A PN junction diode is a two terminal junction device. It conducts only in one direction (only on forward biasing).

FORWARD BIAS:

On forward biasing, initially no current flows due to barrier potential. As the applied potential exceeds the barrier potential the charge carriers gain sufficient energy to cross the potential barrier and hence enter the other region. The holes, which are majority carriers in the P-region, become minority carriers on entering the N-regions, and electrons, which are the majority carriers in the N-region, become minority carriers on entering the P-region. This injection of Minority carriers results in the current flow, opposite to the direction of electron movement.

REVERSE BIAS:

On reverse biasing, the majority charge carriers are attracted towards the terminals due to the applied potential resulting in the widening of the depletion region. Since the charge carriers are pushed towards the terminals no current flows in the device

due to majority charge carriers. There will be some current in the device due to the thermally generated minority carriers. The generation of such carriers is independent of the applied potential and hence the current is constant for all increasing reverse potential. This current is referred to as Reverse Saturation Current (I_O) and it increases with temperature. When the applied reverse voltage is increased beyond the certain limit, it results in breakdown. During breakdown, the diode current increases tremendously.

PROCEDURE:

FORWARD BIAS:

1. Connect the circuit as per the diagram.
2. Vary the applied voltage V in steps of 0.1V.
3. Note down the corresponding Ammeter readings I.
4. Plot a graph between V & I

OBSERVATIONS

1. Find the d.c (static) resistance = V/I.
2. Find the a.c (dynamic) resistance r = δV / δI (**r = ΔV/ΔI) =** $\frac{V_2 - V_1}{I_2 - I_1}$.
3. Find the forward voltage drop = [Hint: it is equal to 0.7 for Si and 0.3 for Ge]

REVERSE BIAS:

1. Connect the circuit as per the diagram.
2. Vary the applied voltage V in steps of 1.0V.
3. Note down the corresponding Ammeter readings I.
4. Plot a graph between V & I
5. Find the dynamic resistance **r = δV / δI.**

FORMULA FOR REVERSE SATURATION CURRENT (I_O):

$$I_o = \partial I / [\exp(\partial V / \eta V_T)] - 1$$

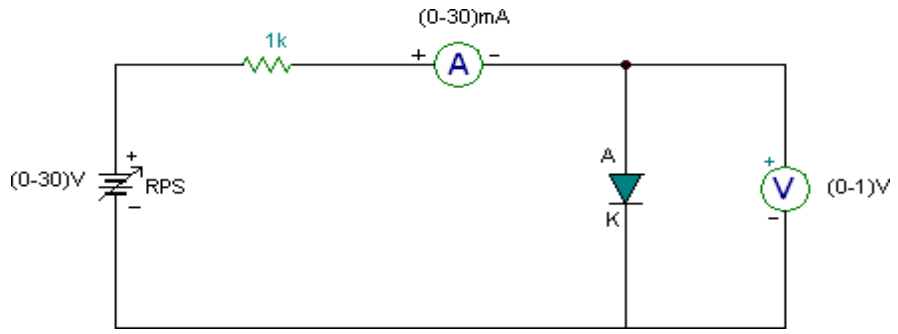
Where V_T is the voltage equivalent of Temperature = kT/q

-k is Boltzmann's constant, q is the charge of the electron and T is the temperature in degrees Kelvin.

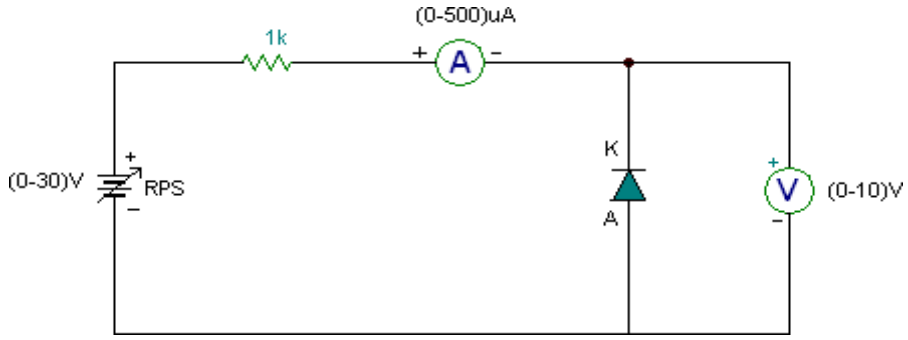
η =1 for Silicon and 2 for Germanium

CIRCUIT DIAGRAM:

FORWARD BIAS:



REVERSE BIAS:



Specification for 1N4007: Silicon Diode

Peak Inverse Voltage: 50V

I_{dc} = 1A.

Maximum forward voltage drop at 1 Amp is 1.1 volts

Maximum reverse current @50 volts is 5μA

TABULAR COLUMN:

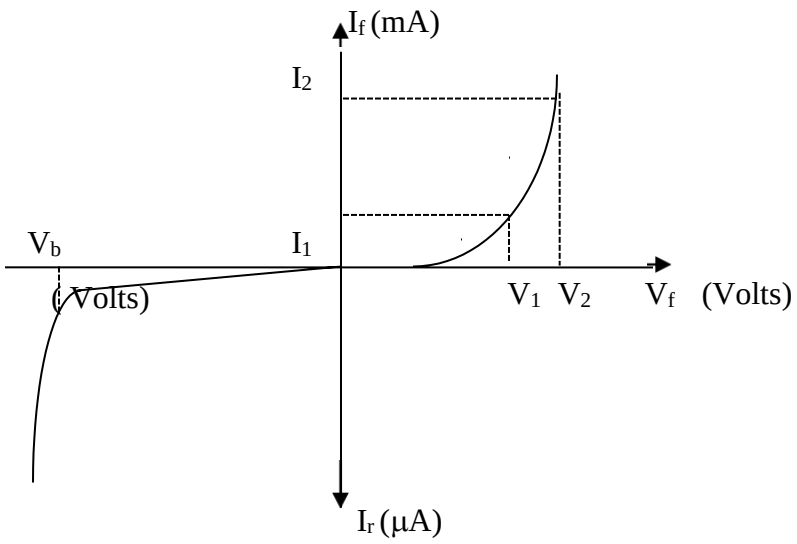
FORWARD BIAS:

S.No.	VOLTAGE (In Volts)	CURRENT (In mA)

REVERSE BIAS:

S..No.	VOLTAGE (In Volts)	CURRENT (In μA)

MODEL GRAPH:



RESULT:

Forward and Reverse bias characteristics of the PN junction diode and the dynamic resistance under

- Forward bias = ----------
- Reverse bias =---------- --.

Ex.No.1B **DATE:**

CHARACTERISTICS OF ZENER DIODE

AIM:

To determine the breakdown voltage of a given zener diode

APPARATUS REQUIRED:

S.No.	Name	Range	Type	Qty
1	R.P.S	(0-30)V		2
2	Ammeter	(0–30)mA		1
		(0–250)µA		1
3	Voltmeter	(0–30)V		1
		(0–10)V		1

COMPONENTS REQUIRED:

S.No.	Name	Range	Type	Qty
1	zener diode	FZ5.1		1
2	Resistor	1KΩ		1
3	Bread Board			1
4	Wires			

THEORY:

A properly doped crystal diode, which has a sharp breakdown voltage, is known as zener diode.

FORWARD BIAS:

On forward biasing, initially no current flows due to barrier potential. As the applied potential increases, it exceeds the barrier potential at one value and the charge carriers gain sufficient energy to cross the potential barrier and enter the other region. the holes ,which are majority carriers in p-region, become minority carriers on entering the N-regions and electrons, which are the majority carriers in the N-regions become minority carriers on entering the P-region. This injection of minority carriers results current, opposite to the direction of electron movement.

REVERSE BIAS:

When the reverse bias is applied due to majority carriers small amount of current (ie) reverse saturation current flows across the junction. As the reverse bias is increased to breakdown voltage, sudden rise in current takes place due to zener effect.

ZENER EFFECT:

Normally, PN junction of Zener Diode is heavily doped. Due to heavy doping the depletion layer will be narrow. When the reverse bias is increased the potential across the depletion layer is more. This exerts a force on the electrons in the outermost shell. Because of this force the electrons are pulled away from the parent nuclei and become free electrons. This ionization, which occurs due to electrostatic force of attraction, is known as Zener effect. It results in large number of free carriers, which in turn increases the reverse saturation current

PROCEDURE:

FORWARD BIAS:

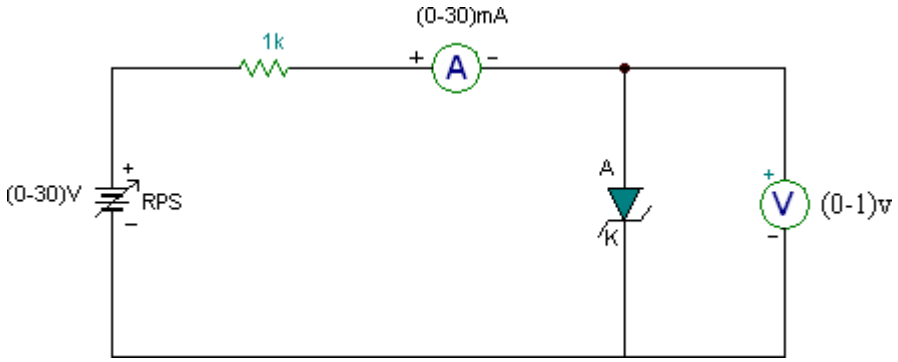
1. Connect the circuit as per the circuit diagram.
2. Vary the power supply in such a way that the readings are taken in steps of 0.1V in the voltmeter till the needle of power supply shows 30V.
3. Note down the corresponding ammeter readings.
4. Plot the graph :V (vs) I.
5. Find the dynamic resistance **r = δV / δI.**

REVERSE BIAS:

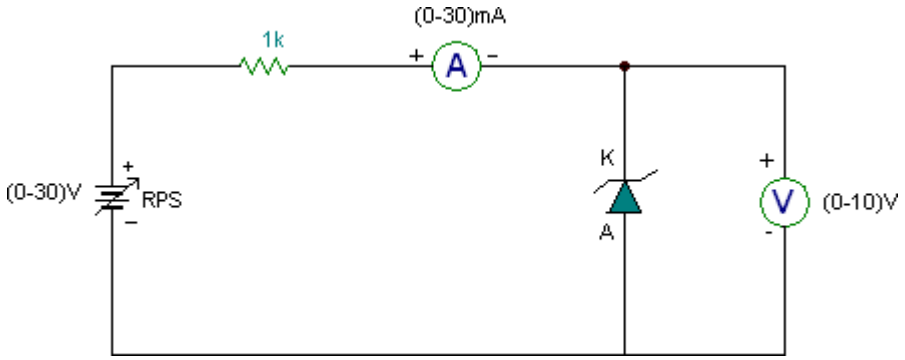
1. Connect the circuit as per the diagram.
2. Vary the power supply in such a way that the readings are taken in steps of 0.1V in the voltmeter till the needle of power supply shows 30V.
3. Note down the corresponding Ammeter readings I.
4. Plot a graph between V & I
5. Find the dynamic resistance **r = δV / δI.**
6. Find the reverse voltage Vr at Iz=20 mA.

CIRCUIT DIAGRAM:

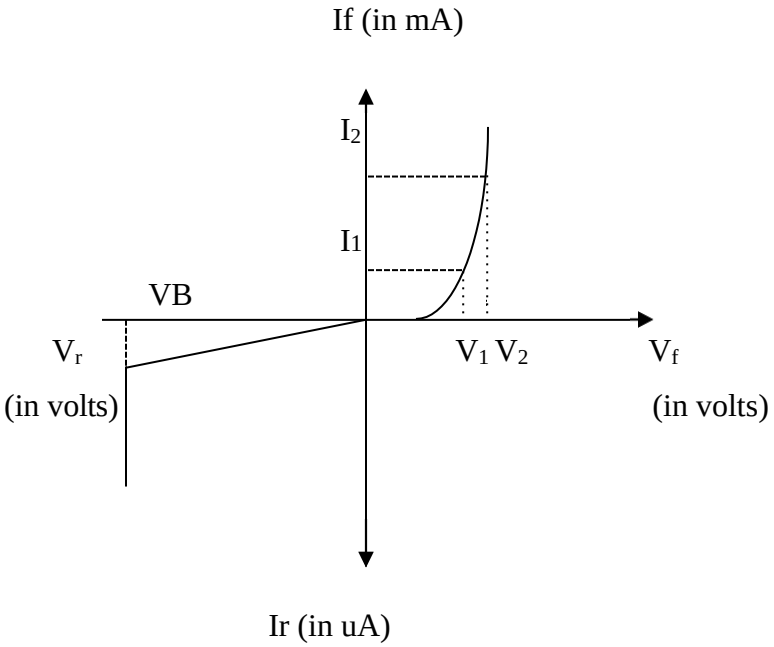
FORWARD BIAS:



REVERSE BIAS:



ZENER DIODE:



TABULAR COLUMN:

FORWARD BIAS:

S..No.	VOLTAGE (In Volts)	CURRENT (In mA)

REVERSE BIAS:

S.No.	VOLTAGE (In Volts)	CURRENT (In μA)

RESULT:

Forward and Reverse bias characteristics of the zener diode was studied and

Forward bias dynamic resistance = ----------

Reverse bias dynamic resistance = ----------

Ex.No: 2 **DATE:**

FULL WAVE RECTIFIER WITH FILTERS

AIM:

To construct a Full wave rectifier using diode and to draw its performance characteristics.

APPARATUS REQUIRED:

S. No.	Name	Range	Type	Qty
1	Transformer	230/(9-0-9)V		1

COMPONENTS REQUIRED:

S. No.	Name	Range	Type	Qty
1	Diode	IN4007		2
2	Resistor	1K Ω		1
3	Bread Board			1
4	Capacitor	100µf		1
5	CRO			1

FORMULAE:

WITHOUT FILTER:

(i) V_{rms} = $V_m / \sqrt{2}$

(ii) V_{dc} = $2V_m / \Pi$

(iii) Ripple Factor = V_{AC}/V_{DC}

(iv) Efficiency = $(V_{dc} / V_{rms})^2 \times 100$

WITH FILTER:

i. V_{rms} = $V_{rpp} /(2*\sqrt{3})$

ii. V_{dc} = $V_{m} - V_{rpp}$

iii. Efficiency = $(V_{dc} / V_{rms})^2 \times 100$

iv. Ripple Factor = $V_{rms'} / V_{dc}$

PROCEDURE:

WITHOUT FILTER:

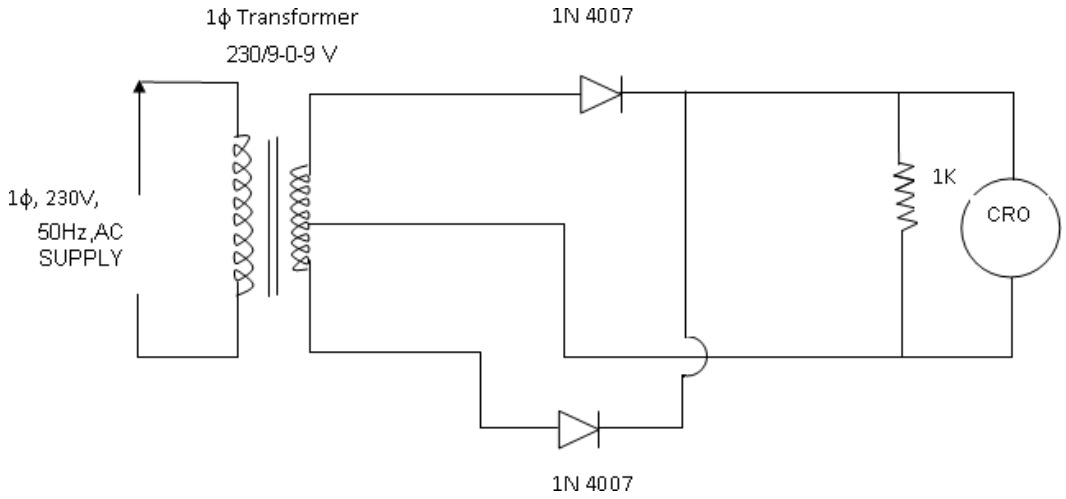
1. Give the connections as per the circuit diagram.
2. Give 230v, 50HZ I/P to the step down TFR where secondary connected to the Rectifier I/P.
3. Take the rectifier output across the Load.
4. Plot its performance graph.

WITH FILTER:

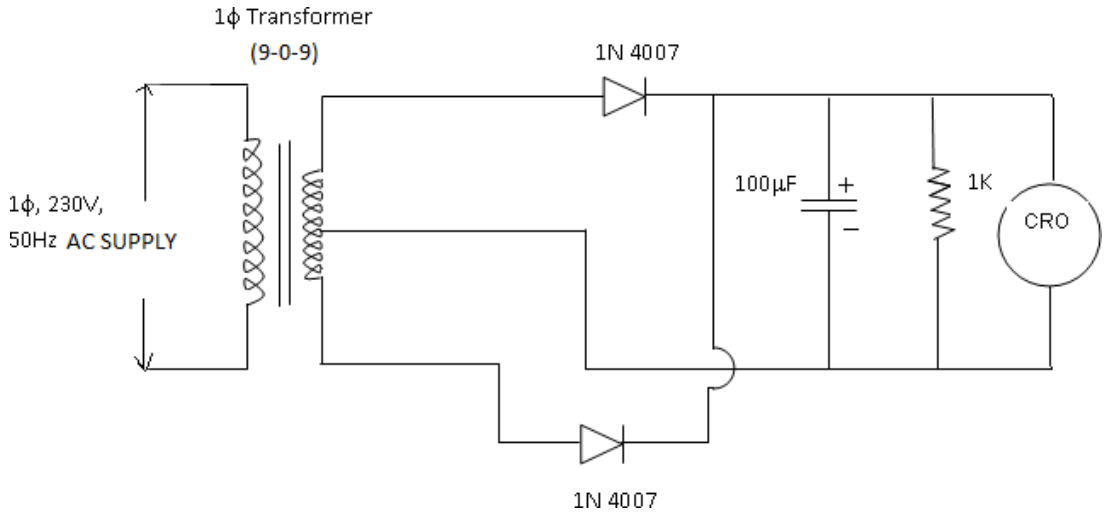
1. Give the connections as per the circuit diagram.
2. Give 230v, 50HZ I/P to the step down TFR where secondary connected to the Rectifier I/P.
3. Connect the Capacitor across the Load.
4. Take the rectifier output across the Load.
5. Plot its performance graph.

CIRCUIT DIAGRAM:

WITHOUT FILTER:



WITH FILTER:



TABULAR COLUMN:

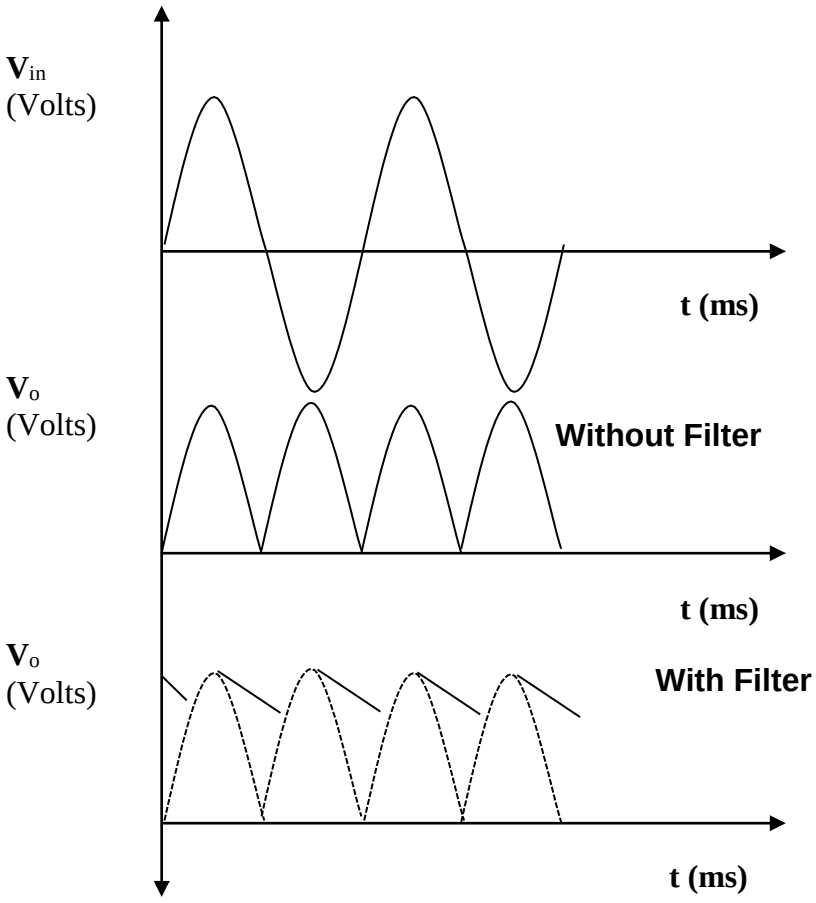
WITHOUT FILTER:

V_m	$V_{rms}= V_m / \sqrt{2}$	$V_{dc}=2V_m / \Pi$	$V_{AC}=Vm/2\sqrt{3}$	Ripple factor

WITH FILTER:

V_m	$V_{rms}= V_m / \sqrt{2}$	$V_{dc}=2V_m / \Pi$	$V_{AC}=Vm/2\sqrt{3}$	Ripple factor

MODEL GRAPH:



RESULT:

Thus the performance characteristics of 1ϕ Full wave rectifier were obtained.

Ex.No: 3 **DATE:**

DESIGN OF ZENER DIODE REGULATOR

AIM:

To setup and study a zener diode shunt regulator and to plot its line and load regulation characteristics.

COMPONENTS REQUIRED:

S.No	Name of the equipment	Type	Range	Quantity (No.S)
1	Zener diode		I_Z5.6	1
2	Resistor, Variable Resistor(rheostat)		150 Ω, 0-2.4K	1
3	Voltmeter	MC	(0-10V) (0-30V)	One from each
4	Ammeter	MC	(0-10 mA)	One
5	Regulated power supply		(0 -30V)	1
6	Bread board			1
7	Connecting wires			As required

THEORY:

A zener diode functions as an ordinary diode when it is forward biased. It is a specially designed device to operate in the reverse bias. When it is in the reverse breakdown region, the zener voltage remains almost constant irrespective of the current Iz through it. A series resistor Rs is used to limit the zener current below its maximum current rating.

The current through Rs is given by the expression Is = Iz+I_L, where $I_L$is the current through the load resistorR_L . The value of must be properly selected to fulfil the following condition requirements.

When the input voltage, V_I increases I_L remains the same, Is and Iz increases. Similarly if input voltage decreases, I_L remains the same, Is and Iz decreases. But if Iz falls lower than the minimum zener current enough to keep the zener in the breakdown region, the regulation will cease and output voltage decreases. A low input voltage can cause the regulator fail to regulate. The series resistance should be selected between Rs_{max}andRs_{min} which are given by the expressions,

$Rs_{min} = [V_{Imax} - Vz]/Iz_{max}$

$Rs_{max} = [V_{Imin} - Vz]/[Iz_{min} + I_L]$

PROCEDURE:

1. Wire up the circuit on the bread board after testing all the components.
2. Keep the load constant. Note down the output voltage varying input from 8V to 14V in steps of 1V. Plot the line regulation graph with Vi along x-axis andV_0 along y-axis. Calculate percentage line regulation using the expression ($\Delta Vo/\Delta Vi$)x100%.
3. 3. Keep the input voltage constant (say 10V) and note down the output voltage for various values of load current starting from 0 to 5 mA, by varying R_L using a rheostat. Plot the load regulation graph with I_L along x-axis and Vo along y-axis.
4. To calculate percentage load regulation, mark V_{NL} and V_{FL}on y-axis on the load regulation graph. V_{NL} is the output voltage in the absence of load resistor and V_{FL} is the output voltage corresponding to rated I_L (here, 5 mA). Calculate the percentage load regulation V_R as per the equation,

$$V_R = \frac{V_{NL} - V_{FL}}{V} x100\%$$

DESIGN

Assume Vo = 5.6V, I_{Lmax} = 5mA Input voltage is in the range 8-14V.

Select 5.6V zener [Po = 400mW , Vz = 5.6 , rd= 8Ω at Iz= 10mA].
Use 2.4 k rheostat as load resistance load current can be varied from 2.4 mA and upwards.

$$Izmax = \frac{P_{max}}{V_Z} = \frac{0.4}{5.6} = 71.42mA$$

Iz min = 10%of I_{Zmax}= 0.1 x 71.42 = 7.142mA

Rsmax > R > Rsmin

$$Rsmax = [V_{Imin} - Vz]/[I_{zmin} + I_{Lmax}] = \frac{(8 - 5.6)V}{(7.142 + 5)mA} = 197.6\Omega$$

$$RSmin = [V_{Imax} - Vz]/Izmax = \frac{(14 - 5.6)V}{71.42mA} = 117.6\Omega$$

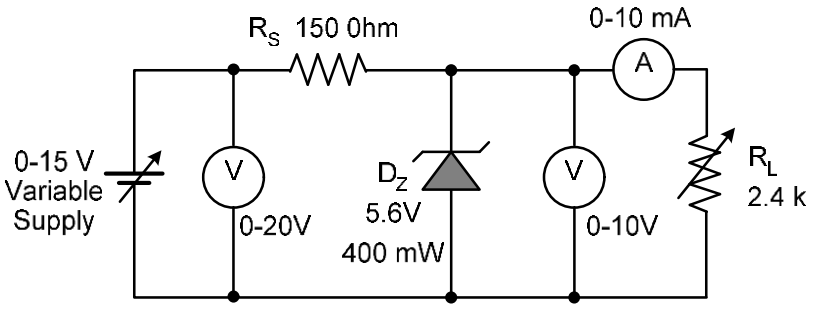
Select Rs= 150

Power rating of Rs

Max current through Rs $= Im = [V_{Imin} - V_z]/Rs = \frac{(14\text{-}5.6)V}{150\ \Omega} = 56mA$

Power rating of Rs = Im^2xRs = 0.4704W >> Select 150 ohms 0.5W resistor

CIRCUIT DIAGRAM



TABULAR COLUMNS

LINE REGULATION

Keeping load current constant at I_L= 5mA, The input voltage is varied from 8 V to 14V and corresponding observations are made.

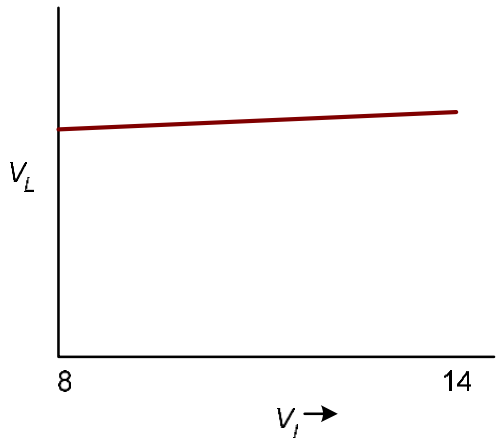
(volts)	**(volts)**

LOAD REGULATION

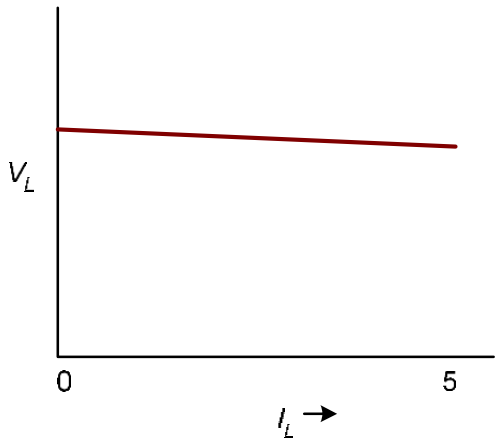
Keeping input voltage at 10V, the load current is varied from 0 to 5 mA and observations are made. For taking reading corresponding to no load (I_L = 0), the loading rheostat may be disconnected.

mA	**(volts)**

EXPECTED OUTPUT PLOTS



Line Regulation



Load Regulation

Result:

Ex. No: 4 **DATE:**

COMMON EMITTER (CE) INPUT-OUTPUT CHARACTERISTICS

AIM:

To plot the transistor characteristics of CE configuration

APPARATUS REQUIRED:

S.No.	Name	Range	Type	Qty
1	R.P.S	(0-30)V		2
2	Ammeter	(0–30)mA		1
		(0–250)uA		1
3	Voltmeter	(0–30)V		1
		(0–1)V		1

COMPONENTS REQUIRED:

S.No.	Name	Range	Type	Qty
1	Transistor	BC 107		1
2	Resistor	10kΩ 1KΩ		1
3	Bread Board			1
4	Wires			

THEORY:

A BJT is a three terminal two – junction semiconductor device in which the conduction is due to both the charge carrier. Hence it is a bipolar device and it amplifier the sine waveform as they are transferred from input to output. BJT is classified into two types – NPN or PNP. A NPN transistor consists of two N types in between which a layer of P is sandwiched. The transistor consists of three terminal emitter, collector and base. The emitter layer is the source of the charge carriers and it is heartily doped with a moderate cross sectional area. The collector collects the charge carries and hence moderate doping and large cross sectional area. The base region acts a path for the movement of the charge carriers. In order to reduce the recombination of holes and electrons the base region is lightly doped and is of hollow cross sectional area. Normally the transistor operates with the EB junction forward biased. In transistor, the current is same in both junctions, which indicates that there is a transfer of resistance between the two junctions. One to this fact the transistor is known as transfer resistance of transistor.

PROCEDURE:

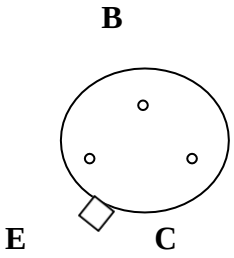
INPUT CHARECTERISTICS:

1. Connect the circuit as per the circuit diagram.
2. Set V_{CE} ,vary V_{BE} in regular interval of steps and note down the corresponding I_B reading. Repeat the above procedure for different values of V_{CE}.
3. Plot the graph: V_{BE} Vs I_B for a constant V_{CE}.
4. Input impedance $h_{ie}=\Delta V_{BE}/\Delta I_B$

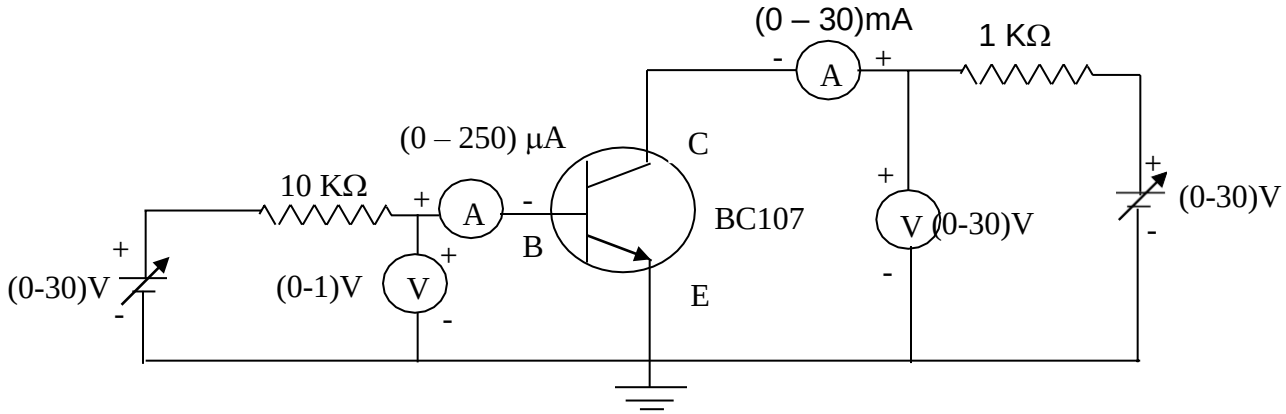
OUTPUT CHARACTERISTICS:

1. Connect the circuit as per the circuit diagram.
2. Set I_B, Vary V_{CE} in regular interval of steps and note down the corresponding I_C reading. Repeat the above procedure for different values of I_B.
3. Plot the graph: V_{CE} Vs I_C for a constant I_B.
4. Output admittance $h_{oe}=\Delta I_C/\Delta V_{CE}$

PIN DIAGRAM:

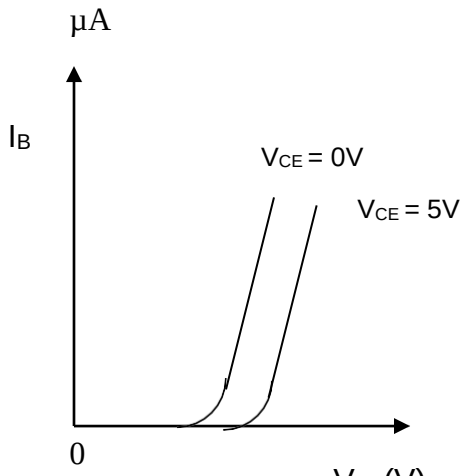


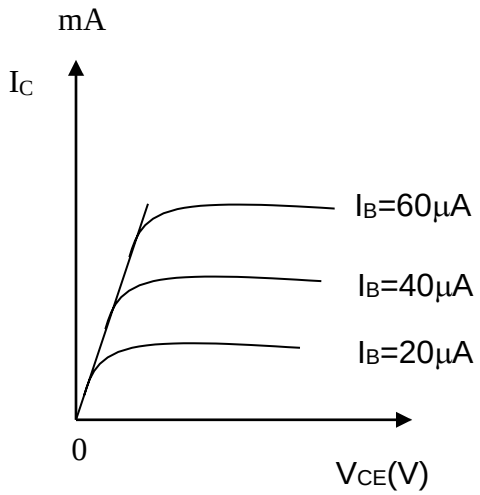
CIRCUIT DIAGRAM:



MODEL GRAPH:

INPUT CHARACTERISTICS: **OUTPUT CHARACTERISTICS:**





TABULAR COLUI

INPUT CHARACTERISTICS:

V_{CE}=1V		**V_{CE}=3V**	
V_{BE}(V)	**I_B(µA)**	**V_{BE}(V)**	**I_B(µA)**

OUTPUT CHARACTERISTICS:

I_B=40μA		I_B=60μA	
V_{CE}(V)	I_C(mA)	V_{CE}(V)	I_C(mA)

RESULT:

The transistor characteristics of a Common Emitter (CE) configuration were plotted

1) Input impedance=

2) Output admittance=

Ex.No: 5 **DATE:**

MOSFET DRAIN CURRENT AND TRANSFER CHARACTERISTICS

AIM:

To study the drain current and transfer characteristics of MOSFET

APPARATUS REQUIRED:

1. MOSFET Trainer Module
2. Ammeters (0-100) mA , (0-500 μ A)
3. Voltmeter (0-30) V DC-2 N0s.
4. Patch cord

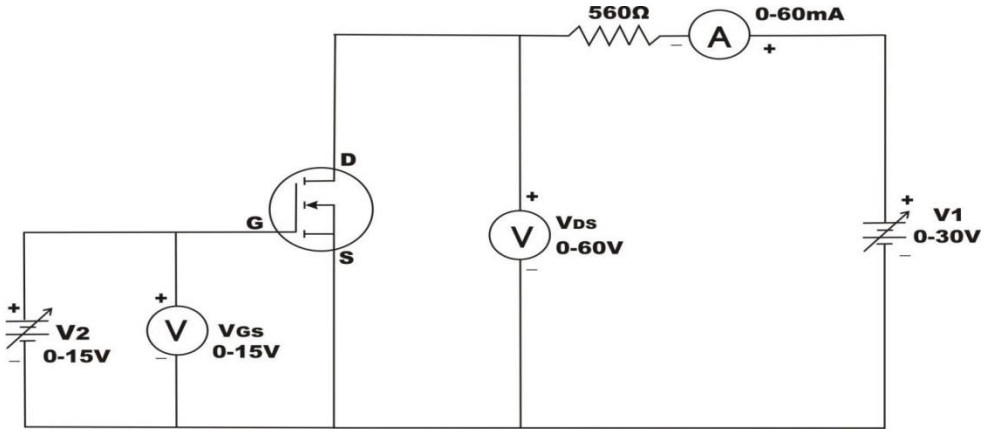
THEORY:

The power MOSFET has three terminals namely drain, source and gate.The drain and source are called as power terminals and the gate is called as control terminals. The control voltage to implement to turn on is applied between the gate & the source terminals. The direction of the direct current flow in an Nchannel device is from the drain to the source. This results from the flow of electrons from the source to the drain. If the drain terminal is made positive with respect to the source without gate voltage, no current flow from the drain to the source because the junction between the N drain region and the P region is reverse biased. Only a small reverse leakage current flows which is negligibly small. This is the off state of the power MOSFET. The power MOSFET is widely used in analog and digital signal processing circuits both in discrete and integrated circuits.

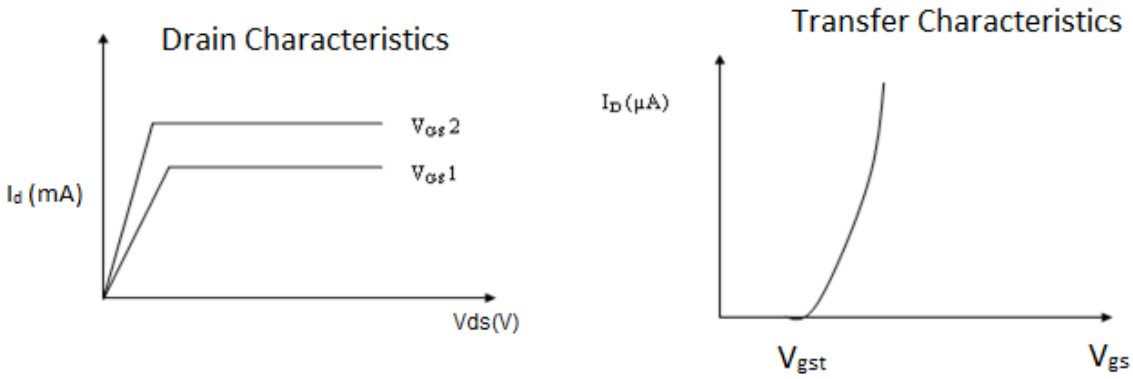
CONNECTION PROCEDURE:

1. Connect MOSFET drain, source, and gate terminal to MOSFET characteristic circuit.
2. Connect voltmeter across the gate –source terminal.
3. Connect Ammeter in drain terminal.
4. Connect Voltmeter across the drain and source terminal to measure V_{DS}.

CIRCUIT DIAGRAM:



MODEL GRAPH:



TABULAR COLUMN:

DRAIN CHARACTERISTICS

V_{GS}= V	
V_{DS}(V)	I_D (mA)

TRANSFER CHARACTERISTICS

V_{DS}= V	
V_{GS}(V)	I_D (mA)

EXPERIMENTAL PROCEDURE:

Output Characteristics

1. Switch on the 230 V supply.
2. Keep the gate to source –voltage (V_{GS}) at particular voltage by varying the pot.
3. Smoothly vary the drain to source voltage till the MOSFET gets turned on and note down the voltmeter (V_{DS}) and ammeter (I_D) reading.
4. Further increase the V_{DS} voltage and note down the current I_D.
5. Repeat the same procedure for different values of V_{GS}.
6. Draw a graph between V_{DS} & I_D keeping V_{GS} as a constant. Calculate the pinch-off voltage.

Transfer Characteristics

1. Switch on the 230V supply.
2. Keep the drain to source –voltage (V_{DS}) at particular voltage by varying the pot.
3. Smoothly vary the gate to source voltage till the MOSFET gets turned on and note down the voltmeter (V_{GS}) and ammeter (I_D) reading.
4. Further increase the V_{GS} voltage and note down the current I_D.
5. Repeat the same procedure for different values of V_{DS}
6. Draw a graph between V_{DS} & I_D keeping V_{GS} as a constant. Calculate the pinch-off voltage.

REVIEW QUESTIONS:

1. What is Forward Transconductance?
2. Mention the operating modes of MOSFET
3. Comparison of E – only MOSFET and DMOSFET
4. Why MOSFETs are never connected or disconnected in the circuit when power is ON?
5. List some advantages of MOSFETs.

RESULT:

Thus the drain current and transfer characteristics of MOSFET was studied.

Ex. No: 6 **DATE:**

FRQUENCY RESPONSE OF CE AND CS AMPLIFIERS

6(A). Frequency response of common emitter amplifier

AIM:

To observe input -output waveforms of common emitter (CE) amplifier .To measure gain of amplifier at different frequencies and plot frequency response.

APPARATUS REQUIRED:

S.No	Name of the apparatus	Range	Type	Quantity
1.	Signal Generator		(0-1)MHz	01
2.	Resistor		560Ω	02
3.	Capacitor		0.2uF	02
4.	CRO			01
5.	Inductor		35mH	01
6.	Breadboard			01

THEORY:

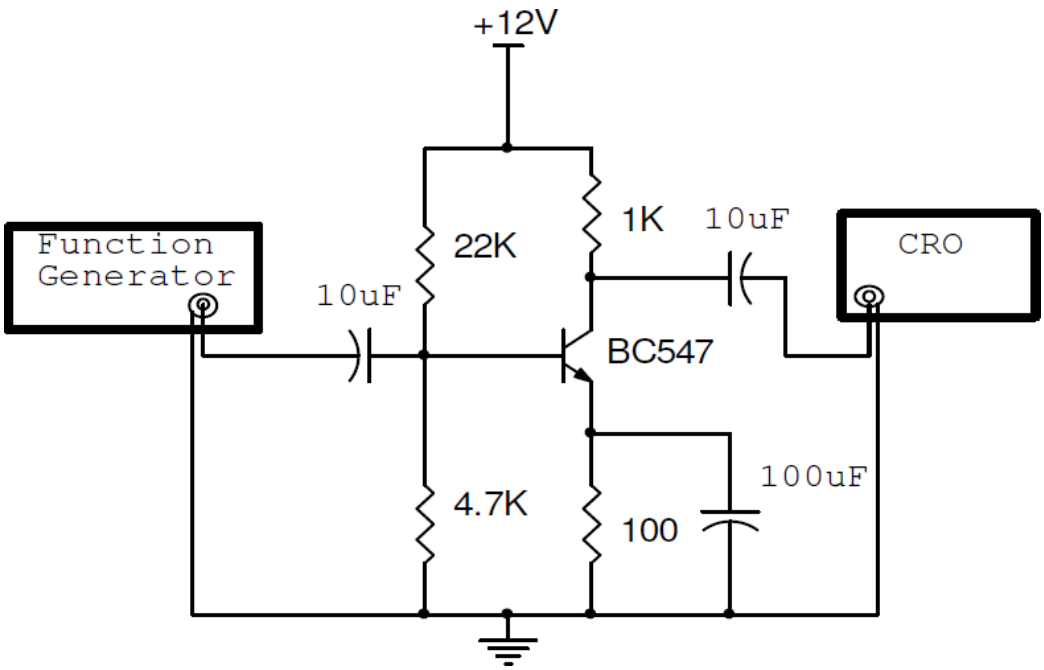
Common emitter amplifier is used to amplify weak signal. It utilizes energy from DC power supply to amplify input AC signal. Biasing of transistor is done to tie Q point at the middle of the load line. In the circuit shown, voltage divider bias I formed using resistors 10K and 2 .2K. During positive cycle, forward bias of base emitter junction increases and base current increases .Q point moves in upward direction on load line and collector current increases times than base current.(is current gain). Collector resistor drop IcRc increases due to increase in collector current Ic.This will reduce collector voltage. Thus during positive input cycle, we get negative output cycle.

When input is negative cycle, forward bias of base emitter junction and base current will reduce Collector current reduces (Q point moves down side). Due to decrease in collector current collector resistance voltage drop IcRc reduces and collector voltage increases Change in collector voltage is much higher than applied base voltage because less base current variation causes large collector current variation due to current gain *B.* This

large collector current further multiplied by collector resistance Rc which provides large voltage output. Thus CE amplifier provides voltage gain and amplifies the input signal

without emitter resistance gain of amplifier is highest but it is not stable. Emitter resistance is used to provide stability. To compensate effect of emitter resistance emitter bypass capacitor is used which provides AC ground to the emitter. This will increase gain of amplifier.

CIRCUIT DIAGRAM:



PROCEDURE:

- Connect function generator at the input of the amplifier circuit.
- Set input voltage 10 mV and frequency 100 Hz.
- Connect CRO at the output of the amplifier circuit.
- Observe amplified signal and measure output voltage
- Increase frequency from the function generator and repeat above step
- Note down readings of output voltage in the observation table for frequency range from 100 Hz to 10 MHz
- Calculate voltage gain for different frequencies and gain in dB. Plot frequency response.

TABULAR COLUMN:

Input voltage: Vi = 10 mV

Sr. No.	Frequency at the input	Output voltage Vo	Gain A = Vo/ Vi	Gain in dB= 20log10(A)
1.				
2.				
3.				
4.				
5.				
6.				
7.				
8.				
9.				
10.				
11.				
12.				

MODEL GRAPH:

RESULT:

6(B). FREQUENCY RESPONSE OF CS AMPLIFIER

Aim:

To measure the gain and to plot the frequency response and to determine the Gain Bandwidth product (GBW) of CS amplifier.

Components Required:

S.No	Component Name	Range	Quantity Required
1	Power Supply	0-30 V	1
2	Resistor	1MΩ,1.5,220Ω, 10KΩ	Each 1
3	Capacitor	100µF,0.01 µF	2
4	Transistor	BC107	1
5	Function generator	(0-1)MHz	1
6	CRO	(0-30) MHz	1
7	Breadboard		1

Theory:

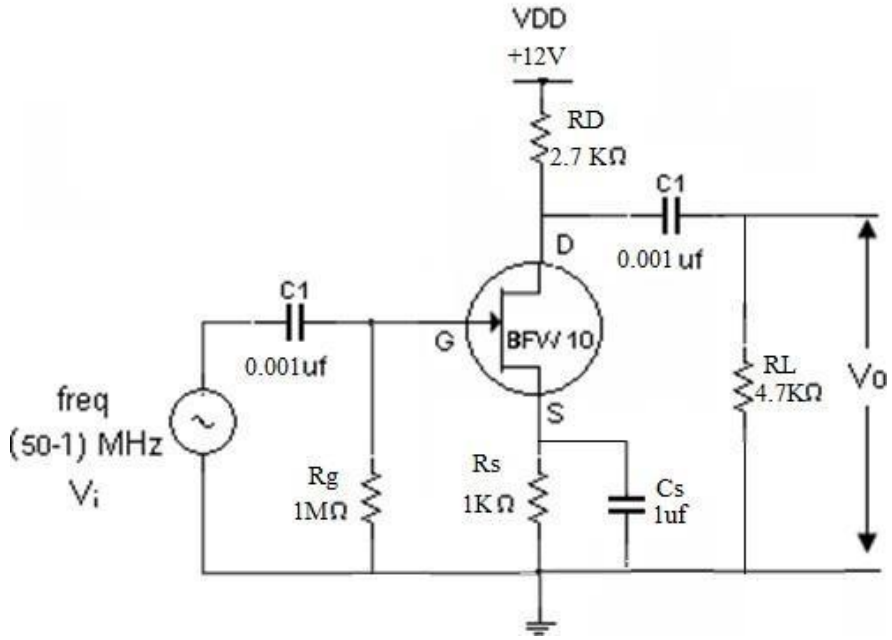
A weak signal is applied between gate and source and output is obtained at drain. For the proper operation of FET, gate must be reverse biased. A small change in reverse bias on the gate produces a large drain current. This fact makes FET capable of raising the strength of a weak signal. The gain of the common source FET amplifier is very high which is greater than unity.

Formula Used:

Voltage gain $A_V = g_m r_L$

Bandwidth $= f_2 - f_1$

Circuit Diagram:



Tabular Form:

Input voltage (Vi)=

Frequency	Output Voltage(Vo)	Gain Av=Vo/Vi	Gain in db 20 log (gain)

Procedure:

1. Connect the circuit as per the circuit diagram.
2. Set Vi =50 mV, using the signal generator.
3. Keeping the input voltage constant, vary the frequency from 0 Hz to 1M Hz in regular steps and note down the corresponding output voltage.
4. Plot the graph; Gain (dB) Vs Frequency (Hz).
5. A graph is drawn by taking frequency on X-axis and gain in dB on Y-axis on a Semi log graph sheet.

Theoreticalcalculations :

$$r_L = \frac{R_D \times R_L}{R_D + R_L} = \frac{1500 \times 10000}{1500 + 10000} = 1300\Omega$$

$$I_{DSS} = 10mA, V_{GS} = 4V$$

$$g_{mo} = \frac{2I_{DSS}}{-V_{GS(off)}} = \frac{2 \times 10mA}{4V} = 5mS$$

$$g_m = g_{mo}\left[1 - \frac{V_{GS}}{V_{GS(off)}}\right] = 5mS\left[1 - \frac{-1}{-4}\right] = 3.75mS$$

$$A_V = g_m \times r_L = 3.75mS \times 1300 = 4.875$$

$$V_{in} = 0.2V_{PP}$$

$$V_{out} = A_V \times V_{in} = 4.875 \times 0.2V_{PP} = 0.935\ V_{PP}$$

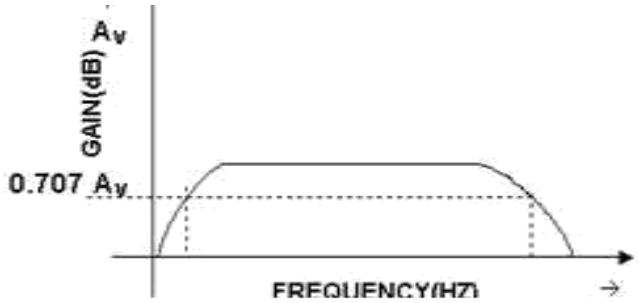
Practical calculations:

$$V_{in} = 0.2V_{PP}$$

$$V_{out} =$$

$$A_V = \frac{V_{out}}{V_{in}} =$$

Model Graph:



Result :

The frequency response of common source amplifier is obtained and the bandwidth is noted.

Ex.No: 7 **DATE:**

FREQUENCY RESPONSE OF CB AND CC AMPLIFIERS

7(A). FREQUENCY RESPONSE OF CB AMPLIFIER

Aim:

To measure the gain and to plot the frequency response and to determine the Gain Bandwidth product (GBW) of CB amplifier.

Components Required:

S.No	Component Name	Range	Quantity Required
1	Power Supply	0-30 V	1
2	Resistor	12KΩ,2.4KΩ,330Ω,1.5KΩ, 1KΩ, 600Ω	Each 1
3	Capacitor	10µF,100µF	2
4	Transistor	BC107	1
5	Function generator	(0-1)MHz	1
6	CRO	(0-30) MHz	1

Theory:

The common base amplifier configuration is not used as widely as transistor amplifier configurations. However it does find uses with amplifiers that require low input impedance levels. One application is for moving-coil microphones preamplifiers - these microphones have very low impedance levels. Another application is within VHF and UHF RF amplifiers where the low input impedance allows accurate matching to the feeder impedance which is typically 50Ω or 75Ω.

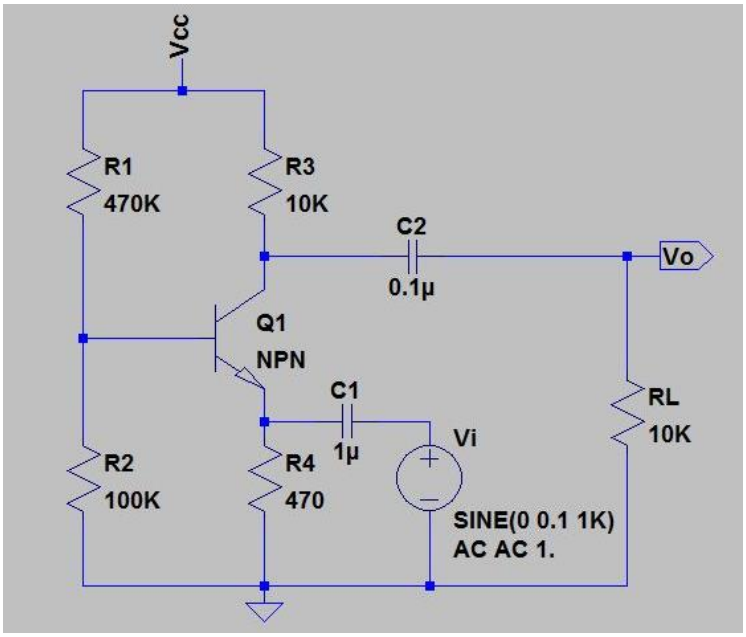
It is worth noting that the current gain of a common-base amplifier is always less than unity.

However the voltage gain may be more, but it is a function of input and output resistances (and also the internal resistance of the emitter-base junction). As a result, the voltage gain of a common-base amplifier can be very high.

Formula Used:

$A_V = 20\log(V_o/V_{in})$
Bandwidth = $f_2 - f_1$

Circuit Diagram:



Tabular Form:

Input voltage (Vi)=

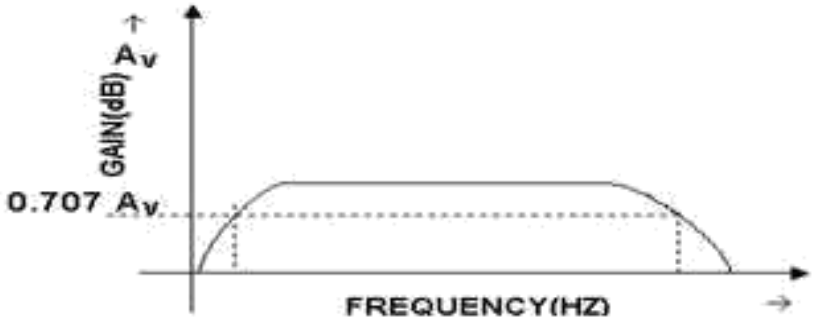
Frequency	Output Voltage(Vo)	Gain Av=Vo/Vi	Gain in db 20 log (gain)

Procedure

1. Connect the circuit as per the circuit diagram.
2. Give l00Hz signal and 20mv p-p as Vs from the signal generator
3. Observe the output on CRO and note down the output voltage.
4. Keeping input voltage constant and by varying the frequency in steps 100Hz-1MHz, note down the corresponding output voltages.
5. Calculate gain in dB and plot the frequency response on semi log sheet

Model Graph:

Frequency response :



Result:

The voltage gain and frequency response of the CB amplifier are obtained. Also gain bandwidth product of the amplifier is calculated.

Ex.No:7 (B) **DATE:**

FREQUENCY RESPONSE OF CC AMPLIFIER

Aim:

To construct a common collector amplifier circuit and to plot the frequency response characteristics.

Apparatus Required:

S.No.	Name	Range	Quantity
1.	Transistor	BC 107	1
2.	Resistor	15kΩ,10kΩ,680Ω,6kΩ	1,1,1,1
3.	Capacitor	0.1μF, 47μF	2, 1
4.	Function Generator	(0-3)MHz	1
5.	CRO	30MHz	1
6.	Regulated power supply	(0-30)V	1
7.	Bread Board		1

Theory:

The D.C biasing in common collector is provided by R1, R2 and RE .The load resistance is capacitor coupled to the emitter terminal of the transistor.

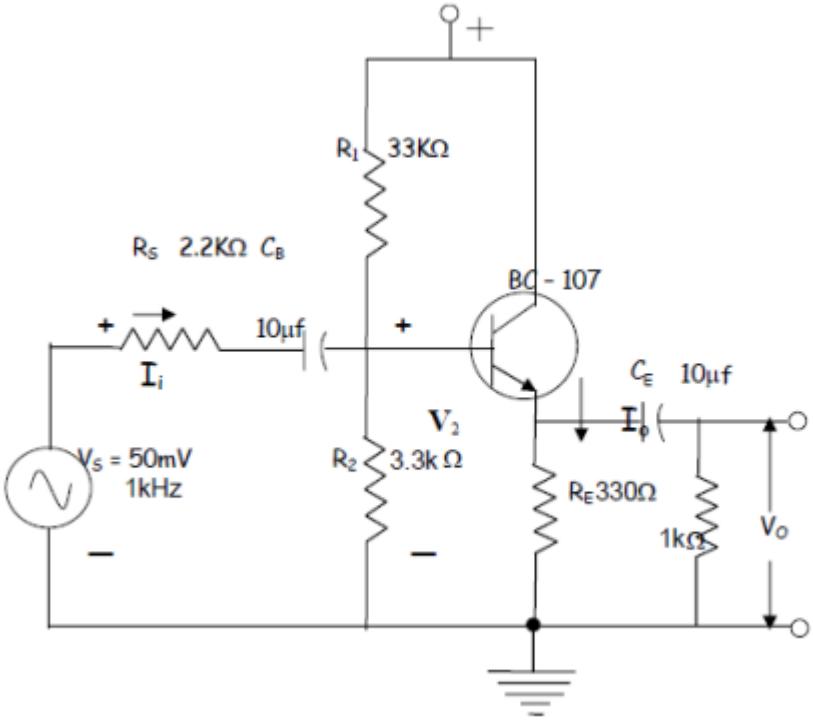
When a signal is applied to the base of the transistor ,VB is increased and decreased as the signal goes positive and negative, respectively. Considering VBE is constant the variation in the VB appears at the emitter and emitter voltage VE will vary same as base voltage VB . Since the emitter is output terminal, it can be noted that the output voltage from a common collector circuit is the same as its input voltage. Hence the common collector circuit is also known as an emitter follower.

Formula Used:

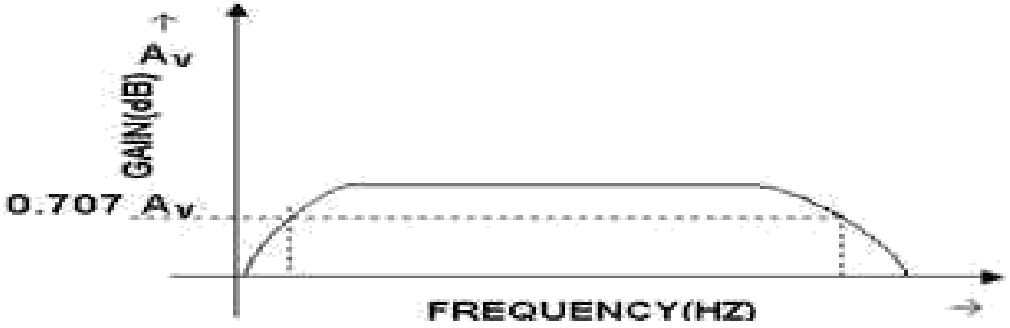
$A_V = 20\log(V_o/V_{in})$

Bandwidth = $f_2 - f_1$

Circuit Diagram:



Model Graph:



Tabular Form:

Input voltage (Vi)=

Frequency	Output Voltage(Vo)	Gain Av=Vo/Vi	Gain in db 20 log (gain)

Procedure:

1. Connect the circuit as per the circuit diagram.
2. Set Vi =50 mV, using the signal generator.
3. Keeping the input voltage constant, vary the frequency from 0 Hz to 1M Hz in regular steps and note down the corresponding output voltage.
4. Plot the graph; Gain (dB) Vs Frequency (Hz).
5. A graph is drawn by taking frequency on X-axis and gain in dB on Y-axis on a Semi log graph sheet.

Result

Thus, the Common collector amplifier was constructed and the frequency response curve is plotted. The Gain Bandwidth Product is found to be =

FREQUENCY RESPONSE OF CASCODE AMPLIFIER

EX.NO: 8 **DATE:**

AIM:

To design and construct a cascode amplifier circuit and to draw its frequency response graph.

EQUIPMENTS REQUIRED

S.NO	EQUIPMENT	RANGE	QUANTITY
1	Transistor	BC 547	2
2	RPS	(0-30)V	1
3	Resistor	1.2K, 33 K,22K, 12K	1
4	Resistor	680Ω	1
5	Capacitor	1 uf, 2.2uf	2
6	Bread Board	-	1
7	Single strand Wires	-	-
8	CRO	(0 - 30) MHz	1
9	CRO Probes	-	3
10	Function Generator	(0 - 3) MHz	1

PROCEDURE

1. Connect the circuit as per the circuit diagram
2. Set Vs = 50mV using signal generator.
3. Keep the input voltage constant; vary the frequency from 50 Hz to 1 MHz in steps.
4. Note down the corresponding output voltage.
5. Plot the graph gain Vs

frequency.Calculate the bandwidth
from the graph

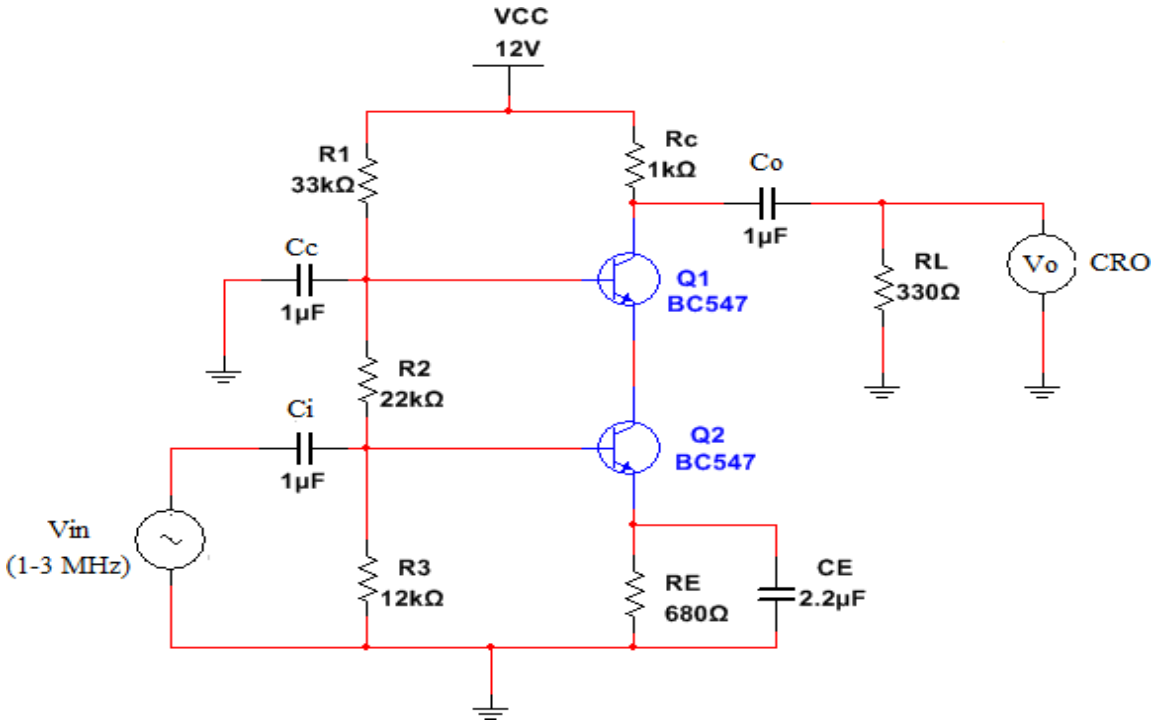
THEORY

A cascode amplifier comprises of a common emitter amplifier and a common base amplifierstages in cascade. In the circuit diagram Q1 common base configuration and Q2 is common

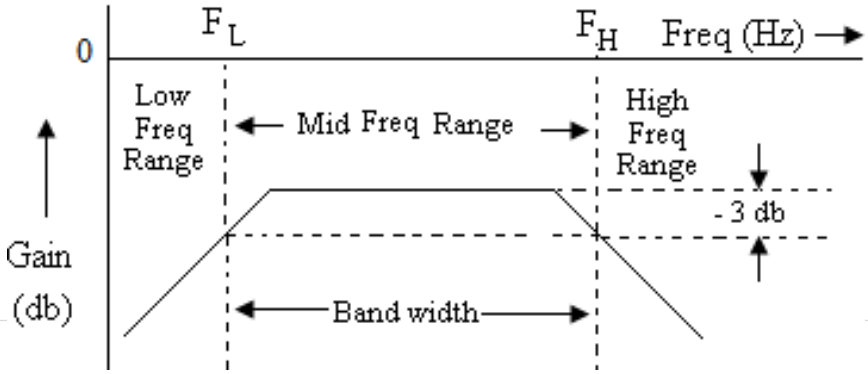
emitter configuration. Principal advantage of this circuit is its low internal capacitance which is a limiting factor gain at high frequencies. Cascode amplifier can able to amplify wide range of frequencies than that is possible with CE amplifier. This is because no high frequency feedback occurs from the output back to

input through the miller capacitance as it occurs in transistor CE configuration. Cascode amplifier provides same voltage gain of CE amplifier but in wide range of frequencies. The advantage of CE and CB stages are put together in cascode connection.

CASCODE AMPLIFIER CIRCUIT DIAGRAM



Model Graph



DESIGN OF FIXED BIAS COMMON EMITTER AMPLIFIER

Design parameters
Vcc=12V, Ic =2mA, h_{fe} (β) =100, Vbe =0.7V,V_{CE1}= V_{CE2}=35% of Vcc = 4.2V
V_{RE}=10% of V_{CC} =1.2VV_{RC}=20% of V_{CC}=2.4V

To find Rc

V_{RC} =Ic*Rc
=2.4V
Rc=1.2KΩ

To find R_E

V_{RE} =I_E*R_E
=1.2V
R_E=600Ω

To find R_1, R_2 and R_3
Vcc-V_{R1}-V_{BE1}-V_{CE2}-V_{RE}=0V_{R1}=Vcc-V_{BE1}-V_{CE2}-V_{RE} V_{R1}=12-0.6-4.2-12= 6V
I_B=Ic/Hfe = 20μA
If 10I_B assumed flowing through R_1 we get

$R1= V_{R1}/10\ I_B = 30K\Omega$

Vcc-V_{R1}-V_{R2}-V_{BE2}-V_{RE}=0V_{R2}=Vcc- V_{R1} -V_{BE2}-V_{RE} V_{R2}=12- 6-0.6-1.2= 4.2V
I_B=Ic/Hfe = 20μA
If 9I_B assumed flowing through R_2 we get

$R2= V_{R2}/9\ I_B = 23K\Omega$

V_{R3}-V_{BE2}-V_{RE}=0
V_{R3}= V_{BE2}+V_{RE}
V_{R3}= 0.6+1.2=
1.8V
I_B=Ic/Hfe = 20µA
If 8I_B assumed flowing through R_3 we get

R3= V_{R3}/8 I_B = 11.2KΩ

To find C_E (Bypass capacitor)X_{CE} =R_E / 10
X_{CE} = 600Ω /10 =60
X_{CE} =1 / 2π f C_E Let f=1000

C_E = 1 / 2*π *1000* 60 =2.2 µf

TABULATION

Vin = ____

SL.NO	Frequency (Hz)	Output Voltage (Vo)	Gain = 20 log (Vo / Vi) (db)

RESULT

Hence designed and constructed Cascode amplifier and plotted its frequency response.

CMRR MEASUREMENT OF DIFFERENTIAL AMPLIFIER

EX.NO:9 **DATE:**

Aim:

To construct differential amplifier in

i) Common mode

ii) differential mode, and to find the common mode rejection ratio (CMRR).

Components Required:

S.No	Component Name	Range	Quantity Required
1	Power Supply	0-30 V	1
2	Resistor	1KΩ,470Ω	2,1
3	Breadboard		1
4	Transistor	BC107	2
5	Function generator	(0-1)MHz	1
6	CRO	(0-30) MHz	1

Theory:

The differential amplifier amplifies the difference between two input signals. Hence it is called differential amplifier. V_1, V_2 are the input voltages then the output voltage V_o will be directly proportional to the difference between two input signals.

If we apply two input voltages equal in all respects then in ideal case output should be zero. But output voltage depends on the average common level of the inputs. Such an average level of two input signals is called common mode signal.

Higher the value of C.M.R.R, better the performance of the differential amplifier. To improve C.M.R.R we have to increase differential mode gain and decrease common mode gain

Formula Used:

C.M.R.R = Ad /Ac

C.M.R.R in dB = 20 log Ad /Ac

Ad= Differential mode gain

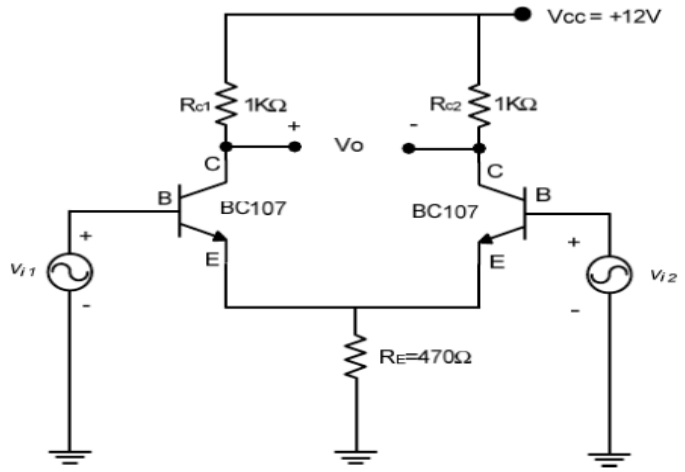
Ac = Common mode gain

$A_d = \frac{h_{fe}R_C}{h_{ie}}$

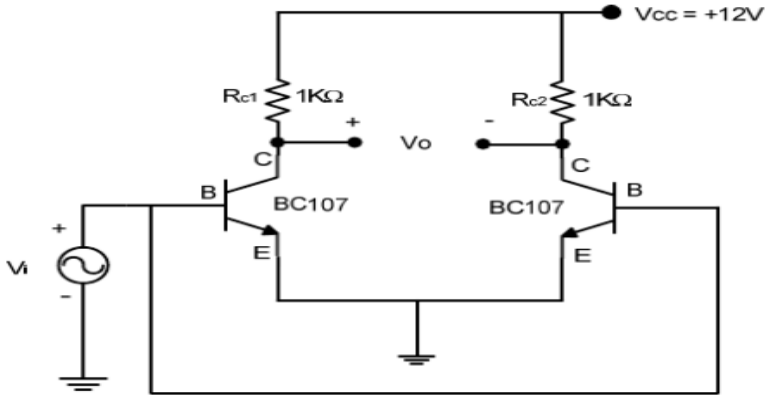
$A_C = \frac{-h_{fe}R_C}{h_{ie}+2R_E(1+h_{fe})}$

Circuit Diagram:

Differential Mode:



Common Mode:



Tabular Column:

Theoretical Value			Practical value						
A_d (Differential mode gain)	A_C (Common mode gain)	CMRR	Differential Mode			Common Mode			CMRR
			V_o	V_{in}	A_d	V_o	V_{in}	A_c	

Procedure:

1. Connections are given as per the circuit diagram
2. Set Vi=5mV and note down Vo in both differential mode & common mode
3. Calculate the gain for both the modes
4. Calculate C.M.R.R

Result

Thus a differential amplifier is constructed in both common mode and differential mode and the corresponding gains are obtained and the CMRR is calculated.

CMRR : Practical Value=

Theoretical Value=

CLASS -A POWER AMPLIFIER(TRANSFORMER COUPLED)

EX.NO: 10 **DATE:**

AIM: To observe the input and output waveforms and to calculate the efficiency.

EQUIPMENT REQUIRED:

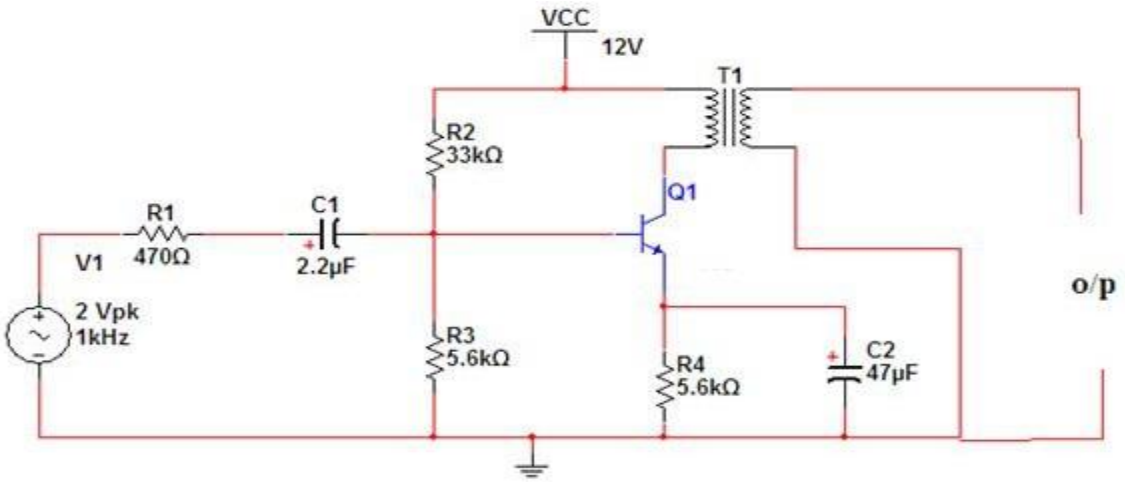
APPARATUS REQUIRED:

Power supply 0-30V- 1 No.
CRO 20MHz - 1 No.
Digital multimeter - 1 No.
Signal generator 1Hz - 1MHz - 1 No.

COMPONNTS REQUIRED:

Resistors 33KΩ - 1N0
5.6KΩ -2NO
470Ω -1NO
Capacitors 47uf -1NO
2.2uf - 1NO
TRANSFORMER -1NO

CIRCUIT DIAGRAM:



THEORY:

The amplifier is said to be class A power amplifier if the q point and the input signal are selected such that the output signal is obtained for a full input cycle . For this class the position of q point is approximately y at the mid point of the load line. For all the values of input signal the transistor remains in the active region and never entire into the cutoff or saturation region. The collector current flows for 3600 (life cycle) of the input signal in other words the angle of the collector current flow is 3600 the claa a amplifiers or furthers classified as directly coupled and transformer coupled and transformer coupled amplifiers in directly coupled type .The load is directly connected in the collector circuit while in the transformer coupled type, the load is coupled to the collector using the transformer.

Advantages:

1. Distortion analysis is very important
2. It amplifies audio frequency signals faithfully hence they are called as audio amplifiers

Disadvantages:

1. H parameter analysis is not applicable
2. Due to large power handling the transistor is used power transistor which is large in size and having large power rating

PROCEDURE:

1. CONNCECT the circuit as per the ciecuit diadram
2. Set Vs (say 250 to 300 mV), at 10 KHz using signal generator.
3. Connect milli ammeter to the ammeter terminals
4. By keeping the input voltage constant, vary the frequency from 0 to 1MHz

   in regular steps .
5. Note down the corresponding output voltage from CRO
6. Calculate the DC input power using the formula $P_{dc} = V_{cc} I_c$
7. Calculate the AC output power using the formula $P_{ac} = V_o^2 / 8R_L$
8. Calculate the efficiency $\eta = P_{ac} / P_{dc}$
9. Plot the graph between Gain (db) and frequency.
10. Calculate bandwidth from the graph.

OBSERVATIONS:

VO =_____, VI = _____

VCC = _____

RL = _____

CALCULATIONS:

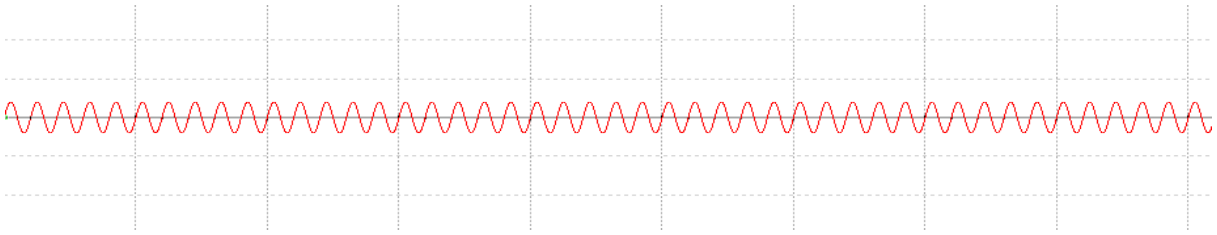
Efficiency (Pac/ Pdc) = _____

$P_{ac} = V_{cc}\ Ic$

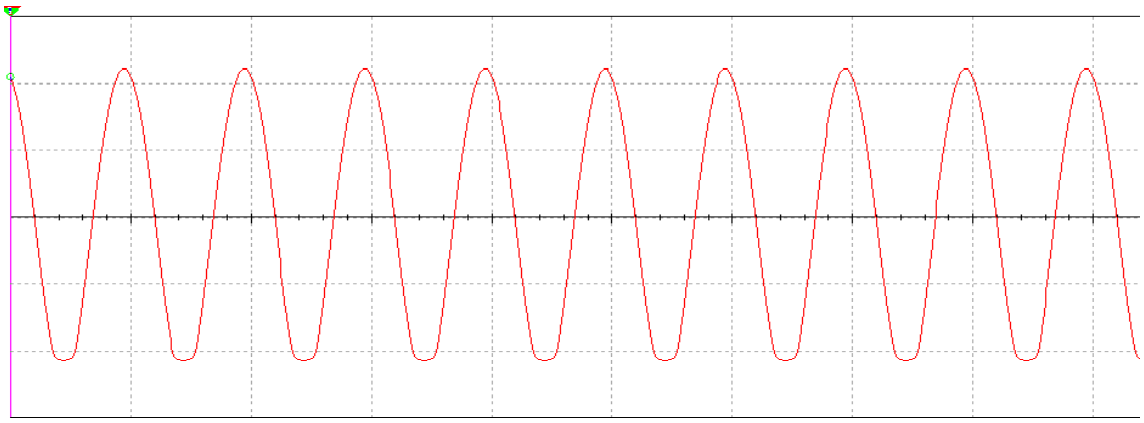
$P_{DC} = V_m/2R_L = V^2_{pp}/8R_L$

$\%n = P_{ac}/ P_{DC} \times 100$

GRAPH: I/P



O/P



RESULT: Gain and frequency as observed of Class A power amplifier.

$\%n = P_{ac}/ P_{DC} \times 100 =$