JEPPIAAR
ENGINEERING COLLEGE

JEPPIAAR NAGAR, CHENNAI – 600119

Department of Electronics & Communication Engineering

QUESTION BANK

EC3352 – DIGITAL SYSTEM DESIGN

II Year/III Semester ECE (Regulation 2021)

JEPPIAAR ENGINEERING COLLEGE		
Vision of the Institute	To build Jeppiaar Engineering College as an institution of academic excellence in technological and management education to become a world class University	
Mission of the Institute	**M1**	To excel in teaching and learning, research and innovation by promoting the principles of scientific analysis and creative thinking
	M2	To participate in the production, development and dissemination of knowledge and interact with national and international communities.
	M3	To equip students with values, ethics and life skills needed to enrich their lives and enable them to meaningfully contribute to the progress of society
	M4	To prepare students for higher studies and lifelong learning, enrich them with the practical and entrepreneurial skills necessary to excel as future professionals and contribute to Nation's economy
DEPARTMENT: ELECTRONICS AND COMMUNICATION ENGINEERING		
Vision of the Department	To become a centre of excellence to provide quality education and produce creative engineers in the field of Electronics and Communication Engineering to excel at international level.	
Mission of the Department	**M1**	Inculcate creative thinking and zeal for research to excel in teaching-learning process
	M2	Create and disseminate technical knowledge in collaboration with industries
	M3	Provide ethical and value based education by promoting activities for the betterment of the society
	M4	Encourage higher studies, employability skills, entrepreneurship and research to produce efficient professionals thereby adding value to the nation's economy

PROGRAM OUTCOMES (PO)	**PO 1**	**Engineering knowledge**: **Apply** the knowledge of mathematics, science, engineering fundamentals, and an engineering specialization to the solution of complex engineering problems.
	PO 2	**Problem analysis**: **Identify, formulate, review** research literature, and **analyze** complex engineering problems reaching substantiated conclusions using first principles of mathematics, natural sciences, and engineering sciences.
	PO 3	**Design/development of solutions**: **Design solutions** for complex engineering problems and **design** system components or processes that meet the specified needs with appropriate consideration for the public health and safety, and the cultural, societal, and environmental considerations
	PO 4	**Conduct investigations of complex problems**: **Use** research-based knowledge and research methods including **design** of experiments, **analysis** and **interpretation** of data, and **synthesis** of the information to provide valid conclusions.
	PO 5	**Modern tool usage**: **Create**, **select**, and **apply** appropriate techniques, resources, and modern engineering and IT tools including prediction and modeling to complex engineering activities with an understanding of the limitations.
	PO 6	**The engineer and society**: **Apply** reasoning informed by the contextual knowledge to assess societal, health, safety, legal and cultural issues and the consequent responsibilities relevant to the professional engineering practice.
	PO 7	**Environment and sustainability**: **Understand** the impact of the professional engineering solutions in societal and environmental contexts, and **demonstrate** the knowledge of, and need for sustainable development.
	PO 8	**Ethics**: **Apply** ethical principles and commit to professional ethics and responsibilities and norms of the engineering practice.
	PO 9	**Individual and team work**: **Function effectively** as an individual, and as a member or leader in diverse teams, and in multidisciplinary settings.
	PO 10	**Communication**: **Communicate effectively** on complex engineering activities with the engineering community and with society at large, such as, being able **to comprehend** and **write** effective reports and **design** documentation, **make** effective presentations, and **give** and **receive** clear instructions.
	PO 11	**Project management and finance**: **Demonstrate** knowledge and understanding of the engineering and management principles and **apply** these to one's own work, as a member and leader in a team, to **manage** projects and in multidisciplinary environments.
	PO 12	**Life-long learning**: **Recognize** the need for, and have the preparation and ability to **engage** in independent and life-long learning in the broadest context of technological change.

PROGRAM EDUCATIONAL OBJECTIVES (PEOS)	**PEO I**	Produce technically competent graduates with a solid foundation in the field of Electronics and Communication Engineering with the ability to analyze, design, develop, and implement electronic systems.
	PEO II	Motivate the students for choosing the successful career choices in both public and private sectors by imparting professional development activities.
	PEO III	Inculcate the ethical values, effective communication skills and develop the ability to integrate engineering skills to broader social needs to the students.
	PEO IV	Impart professional competence, desire for lifelong learning and leadership skills in the field of Electronics and Communication Engineering.
PROGRAM SPECIFIC OUTCOMES (PSOs)	**PSO 1**	Design, develop and analyze electronic systems through application of relevant electronics, mathematics and engineering principles.
	PSO 2	Design, develop and analyze communication systems through application of fundamentals from communication principles, signal processing, and RF System Design & Electromagnetics.
	PSO 3	Adapt to emerging electronics and communication technologies and develop innovative solutions for existing and newer problems.

SYLLABUS

EC3352	DIGITAL SYTEM DESIGN	L	T	P	C
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OBJECTIVES:

- To present the Digital fundamentals, Boolean algebra and its applications in digital systems
- To familiarize with the design of various combinational digital circuits using logic gates
- To introduce the analysis and design procedures for synchronous and asynchronous sequential circuits
- To explain the various semiconductor memories and related technology
- To introduce the electronic circuits involved in the making of logic gates

UNIT I DIGITAL FUNDAMENTALS 9

Number Systems – Decimal, Binary, Octal, Hexadecimal, 1„s and 2„s complements, Codes – Binary, BCD, Excess 3, Gray, Alphanumeric codes, Boolean theorems, Logic gates, Universal gates, Sum of products and product of sums, Minterms and Maxterms, Karnaugh map Minimization and Quine-McCluskey method of minimization.

UNIT II COMBINATIONAL CIRCUIT DESIGN 9

Design of Half and Full Adders, Half and Full Subtractors, Binary Parallel Adder – Carry look ahead Adder, BCD Adder, Multiplexer, Demultiplexer, Magnitude Comparator, Decoder, Encoder, Priority Encoder.

UNIT III SYNCHRONOUS SEQUENTIAL CIRCUITS 9

Flip flops – SR, JK, T, D, Master/Slave FF – operation and excitation tables, Triggering of FF, Analysis and design of clocked sequential circuits – Design - Moore/Mealy models, state minimization, state assignment, circuit implementation – Design of Counters- Ripple Counters, Ring Counters, Shift registers, Universal Shift Register.

UNIT IV ASYNCHRONOUS SEQUENTIAL CIRCUITS 9

Stable and Unstable states, output specifications, cycles and races, state reduction, race free assignments, Hazards, Essential Hazards, Pulse mode sequential circuits, Design of Hazard free circuits.

UNIT V MEMORY DEVICES AND DIGITAL INTEGRATED CIRCUITS 9

Basic memory structure – ROM -PROM – EPROM – EEPROM –EAPROM, RAM – Static and dynamic RAM - Programmable Logic Devices – Programmable Logic Array (PLA) - Programmable Array Logic (PAL) – Field Programmable Gate Arrays (FPGA) - Implementation of combinational logic circuits using PLA, PAL.

Digital integrated circuits: Logic levels, propagation delay, power dissipation, fan-out and fan-in, noise margin, logic families and their characteristics-RTL, TTL, ECL, CMOS

TOTAL: 45 PERIODS

TEXT BOOK:

1. M. Morris Mano and Michael D. Ciletti, “Digital Design”, 5th Edition, Pearson, 2014.

REFERENCES:

1. Charles H.Roth. “Fundamentals of Logic Design”, 6th Edition, Thomson Learning, 2013.
2. Thomas L. Floyd, “Digital Fundamentals”, 10th Edition, Pearson Education Inc, 2011
3. S.Salivahanan and S.Arivazhagan“Digital Electronics”, Ist Edition, Vikas Publishing House pvt Ltd, 2012.
4. Anil K.Maini “Digital Electronics”, Wiley, 2014.
5. A.Anand Kumar “Fundamentals of Digital Circuits”, 4th Edition, PHI Learning Private Limited, 2016.
6. Soumitra Kumar Mandal “ Digital Electronics”, McGraw Hill Education Private Limited, 2016.

UNIT I- DIGITAL FUNDAMENTALS

1. **What is the largest binary number that can be expressed with 14 bits? (Apr/May'19)**
   Solution: The largest binary number that can be expressed with 14 bits 11111111111111
   Decimal Equivalent=2^{14}-1= $(16.383)_{10}$
   Hexadecimal Equivalent= $(3FFF)_{16}$
2. **Find the complement of F =wx + yz and then show that FF' = 0. (Apr/May'19)**
   Solution:
   $(wx+yz)^{‘‘}=(wx)^{‘‘}.(yz)^{‘‘}=(w^{‘‘}+x^{‘‘})(y^{‘‘}+z^{‘‘})$
   $FF^{‘‘}=wx(w^{‘‘}+x^{‘‘})(y^{‘‘}+z^{‘‘})+yz(w^{‘‘}+x^{‘‘})(y^{‘‘}+z^{‘‘})=0$
3. **Subtract $(1010)_2$ from $(1000)_2$ using 2´s complement method. Subtract by direct method also and compare. (Nov/Dec 2018)**

2 ´ s complement method:

2 ´ s complement of $(1010)_2$ = 0110
Add $(1000)_2$ with $(0110)_2$ 1000

```
-----
 1110
-----
```

Direct method:

```
  1000
  1010
-------
 11110
-------
```

4. **Interpret the function Y=A+B´ C in canonical POS. (Nov/Dec 2018)**

In the above three-variable expression, the function is given as sum of product form. First, the function needs to be changed to product of sum form by applying distributive law as shown below.
Y = A + B′C = (A + B′) (A + C)
Now, in the above expression, C is missing from the first term and B is missing from the second term. Hence CC′ is to be added with the first term and BB′ is to be added with the second term as shown below.
Y = (A + B′) (A + C) = (A + B′ + CC′) (A + C + BB′)
Y = (A + B′ + C) (A + B′ + C′) (A + B + C) (A + B′ + C)

5. **State & prove De-Morgan ´ s theorem. (May/June '13,Nov/Dec '15, Nov/Dec 17)**

De-Morgan´s theorem 1: The complement of product of any number of variables is equivalent to sum of the individual complements.

De-Morgan´s theorem 2: The complement of sum of any number of variables is equivalent to product of the individual complements.

Proof:

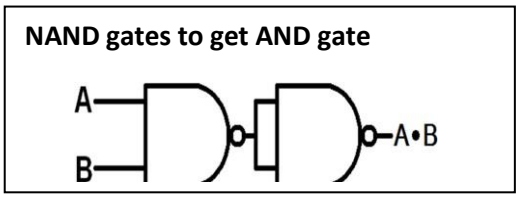
a) (AB) ´ = A´ + B´

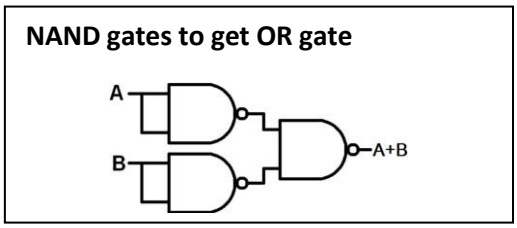
A	B	AB	**(AB)´**		A´	B´	**A´+B´**
0	0	0	**1**		1	1	**1**
0	1	0	**1**		1	0	**1**
1	0	0	**1**		0	1	**1**
1	1	1	**0**		0	0	**0**

b) (A+B) ´ = A´B´

A	B	A+B	**(A+B)´**		A´	B´	**A´B´**
0	0	0	**1**		1	1	**1**
0	1	1	**0**		1	0	**0**
1	0	1	**0**		0	1	**0**
1	1	1	**0**		0	0	**0**

6. Show how to connect NAND gates to get an AND gate and OR gate.(May/June '17)





7. Prove the Boolean theorems (a) x+x=x (b) x+xy=x (May/June 2016)

Solution: (a) x+x =x

LHS : x+x = x(1+1) = x

(b) x+xy = x

LHS : x+xy = x (1+y) = x

8. Simplify the following expression X.Y+X(Y+Z)+Y(Y+Z). (Nov/Dec 2016)

Solution: XY + XY + XZ + Y + YZ
= XY + XZ + Y + YZ
= XY + XZ + Y
= Y + XZ

9. Convert Y = A+BC'+AB+A'BC into canonical form (April/May 2015)

Solution: Y = A+BC'+AB+A'BC = A (B+B') +BC'(A+A') +AB(C+C') +A'BC
=> AB+AB'+ABC'+A'BC'+ABC+ABC'+A'BC
=> AB(C+C') +AB'(C+C') +ABC'+A'BC'+ABC+ABC'+A'BC
=> ABC+ABC'+AB'C+AB'C'+ ABC'+A'BC'+ABC+ABC'+A'BC
=> ABC+ABC'+AB'C+AB'C'+A'BC'+A'BC.

10. Express the function Y=A+B'C into canonical form. (Nov/Dec 2015)

A	B	C	B´	B´C	A+B´ C
0	0	0	1	0	0
0	0	1	1	1	1
0	1	0	0	0	0
0	1	1	0	0	0
1	0	0	1	0	1
1	0	1	1	1	1
1	1	0	0	0	1
1	1	1	0	0	1

Canonical Form

Y = A'B'C+AB'C'+AB'C+ABC'+ABC

11. Apply De-Morgan´s theorem to [(A+B) +C] ´ (May/June 2014)

= (A+B) ´C´ = (A´B´) C ´

12. Simplify the following Boolean expression into one literal (Nov/Dec 2014).

W ´ X (Z ´ +YZ ´) +X (W+YZ)

Solution: W'XZ'(1+Y) +X (W+YZ) => W'XZ'+WX+XYZ => X (W'Z'+W) +XYZ => (W+Z') X+XYZ => WX+XZ'+XYZ => WX+X (Z'+YZ) => WX+XZ'+YZ =>X (W+Z'+Y)

13. Use De Morgan´s theorem to convert the following expressions to one that has only single variable inversions?

Y = (RS´T+Q´) ´

Z = [(A+BC) (D+EF)] ´

X = [(A´+C) (B+D´)] ´

Ans: Y = (RS´T+Q´) ´ = (R´+S+T´) Q

Z = [(A+BC) (D+EF)] ´ = (A+BC) ´+ (D+EF) ´
Z = A´ (BC) ´ + D´ (EF) ´= A´ (B´+C´) + D´ (E´+F´) = A´B´+A ´ C ´ +D ´ E ´ +D ´ F ´
X = [(A ´ +C) (B+D ´)] ´ = (A ´ +C) ´ + (B+D ´) ´ = AC ´ +B ´ D

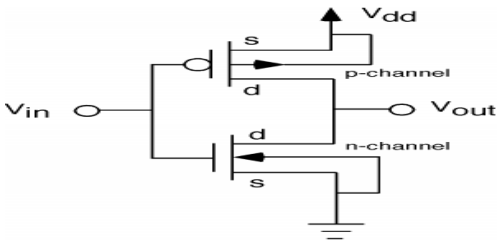
14. Define distributive law.

X (Y + Z) = XY + XZ X + YZ = (X + Y) (X + Z)

15. Simplify the expression: X = (A ´ +B) (A+B+D) D ´

X = (A ´ +B) (A+B+D) D ´ = (AA ´ + A ´ B + A ´ D + AB + BB + BD) D ´
X = (0 + A ´ B + A ´ D + AB + B + BD)D ´
= (A ´ D + B (A ´ + A + 1 + D)) D ´
= (A ´ D + B) D ´
X = A ´ DD ´ + BD ´ = 0 + BD ´ = BD ´

16. Draw the CMOS inverter circuit (Nov/Dec 2014).



17. Describe the importance of don´t care conditions. (May/June 2013)

Functions that have unspecified outputs for some input combinations are called incompletely specified functions. We simply don´t care, what value is assumed by the function for the specified minterms. The unspecified minterms are called don´t care conditions. These don´t care conditions can be used on a map to provide further simplification of the Boolean expression.

18. Convert 0.35 to equivalent hexadecimal number.

Given $(0.35)_{10}$ =0.35 x 16=5.60
=0.60 x 16=9.60
=0.60 x 16=9.60
$(0.35)_{10} = (0.599)_{16}$

19. How many bits are required to represent the decimal numbers in the range 0 to 999 using straight binary code? Using BCD codes?

$(999)_{10}$ = (1111100111)$_2$ → 10 bits are required using straight binary code
$(999)_{10}$ = (1001 1001 1001)$_{BCD}$ → 12 bits are required using BCD code

20. Show that the excess-3 code is self-complementing.

Self-complementing property: 1 ´ s complement of XS-3 code of a decimal digit is equal to XS-3 code of 9 ´ s complement of the corresponding decimal digit.

Example:

XS-3 code of the decimal digit 2	=	0101
1 ´ s complement of 0101	=	1010 ---------- (1)
9 ´ s complement of 2	=	9-2 = 7
XS-3 code of 7	=	1010 ---------- (2)

Self- complementing property of XS-3 code is proved from equations (1) & (2)

21. Add the decimals 67 and 78 using excess-3 code.

67 = (0110 0111) $_{BCD}$ = (1001 1010) $_{XS-3}$

78 = (0111 1000) $_{BCD}$ = (1010 1011) $_{XS-3}$

```
-------------------
  1 0100 0101 ( + )
  0011 0011 0011
-------------------
   ( 0100 0111 1000 ) XS-3
-------------------
```

22. What is meant by weighted and non-weighted code?

- **Weighted codes** are those that obey positional weighting principles. In weighted Code , each position of the number represents a specific weight.
  Example: 8421, 2421 & 84-2-1.
- **Non-Weighted codes** are codes that are not positionally weighted. Each position of the number is not assigned a fixed value. Example: Excess-3 & Gray code

23. State Distributive Law.

Distributive law of dot(.) over plus (+) is given by **a.(b+c) = a.b + a.c**

Distributive law of plus(+) over dot(.) is given by **a+b.c = (a+b).(a+c)**

24. Convert the gray code number 11011 to binary.

gray code 11011 binary code =10010

25. What is even parity?

A parity bit is an extra bit included with a message to make the total number of 1‟s either odd or even. If the total number of 1‟s is even then it is called even parity.

26. Find the 2‟s complement and 1‟s complement of 101101.

1‟s complement of 101101 = 010010

2‟s complement of 101101 = 010010

```
          +  1
-----------
  010011
-----------
```

27. Simplify X1 +X1 X2.

x1 + x1x2

= x1(1+x2)

= x1

28. Find the standard sum for the following function. (Apr/May2015, May 2006)

f = x1 x2 x3 + x1 x3 x4 + x1 x2 x4.

f = x1 x2 x3 + x1 x3 x4 + x1 x2 x4

= x1 x2 x3(x4+x4‟) + x1(x2+x2‟) x3x4+x1x2(x3+x3‟) x4

= x1x2x3x4 +x1x2x3x4‟+x1x2‟x3x4 + x1x2x3‟x4

29. Convert binary number 11011110 into its decimal equivalent. (May/June 2014May 2007)

1 1 0 1 1 1 1 0

```
---------- 0 * 2^0=0
---------- 1 * 2^1=2
---------- 1 * 2^2=4
---------- 1 * 2^3=8
---------- 1 * 2^4=16
---------- 0 * 2^5=0
---------- 1 * 2^6=64
---------- 1 * 2^7=128
--------
  222
```

30. Mention any two applications of Demorgan‟s theorem. (May 2007)

Simplification of Boolean expression and to convert AND to OR and vice versa

31. Simply the following Boolean function:(Nov/Dec 2014, Nov/Dec 2013,May 2007)

(a) $x(x''+y)$

(b) $xy + x''z + yz$

(a) $xx'' + xy$ $(xx'' = 0)$

$= xy$

(b) $xy + x''z + yz$ (by consensus theorem)

$= xy + x''z$

32. Convert the binary number 1011 to gray code. (May 2007)

Gray code of 1011 is 1110

33. Minimize the function using Boolean algebra f = x(y+w''z)+wxz. (Nov/Dec 2014, Nov/Dec 2013,May 2007)

$F = x(y+w''z) + wxz$

$= xy + xw''z + wxz$

$= xy + xz(w'' + w)$

$= xy + xz$

34. Determine a 2 bit Gray code and tabulate along with their equivalent decimal number(May2008)

Binary number	Gray code	Equivalent decimal
00	00	0
01	01	1
10	11	3
11	10	2

35. What are Universal Gates? Why are they called so?

Universal gates are NAND and NOR. These are called so because using these gates, any logical gate or logical expression can be derived.

36. Simplify Y = (A+B) (A´ +C)

Y = (A+B) (A´ +C) = AA´ + AC + A´ B + BC = 0 + AC + A´ B + BC

Y = AC + A´ B + BC

Y = AC + A´ B--------- using consensus theorem XY+X´ Z+YZ=XY+X´ Z

37. Define distributive law.

X (Y + Z) = XY + XZ X + YZ = (X + Y) (X + Z)

38. Simplify the expression: X = (A ´ +B) (A+B+D) D ´

X = (A ´ +B) (A+B+D) D ´ = (AA ´ + A ´ B + A ´ D + AB + BB + BD) D ´

X = (0 + A ´ B + A ´ D + AB + B + BD)D ´

= (A ´ D + B (A ´ + A + 1 + D)) D ´

= (A ´ D + B) D ´

X = A ´ DD ´ + BD ´ = 0 + BD ´ = BD ´

***39.* Convert *Y=A+BC'+AB+A'BC* into canonical form.**

Given *Y=A+BC'+AB+A'BC*

Y=A(B+B')(C+C')+(A+A')BC'+AB(C+C')+A'BC

Y=ABC+ABC'+AB'C+AB'C'+ABC'+A'BC'+ABC+ABC'+A'BC

Y=ABC+ABC'+AB'C+AB'C'+A'BC'+A'BC

40. Simplify the following Boolean Expression to a minimum number of literals.

(BC′+A′D)(AB′+CD′)

F=(BC′+A′D)(AB′+CD′)

F =BC′AB′+BC′CD′+A′DAB′+A′DCD′ (A.A′=0)

F = AB B′C′+BCC′D′+AA′ B′D+A′CDD′

F=0

41. Simplify the given Boolean Expression *F=x′+xy+xz′+xy′z′.*

F=x′+xy+xz′+xy′z′

= x′+x(y+z′+y′z′) (A+A′B=A+B)

= x′+y+z′+y′z′

= x′+y+z′(1+y′) (1+A′=1)

F = x′+y+z′

42. Simplify the following Boolean expression into one literal.

W′X(Z′+YZ)+X(W+ Y′Z)

F= *W′X(Z′+YZ)+X(W+ Y′Z)*

= *W′XZ′+W′XYZ+WX+XY′Z*

=*X(W′Z′+W′YZ+W+Y′Z)*

= *X(W′Z′+W+Z(Y′+W′Y))*

= *X(W′Z′+W+Z(Y′+ Y)(Y′+W′))*

= *X(W′Z′+W+Z(Y′+W′))*

= *X(W′Z′+W+ZY′+W′Z)*

= *X(W′+Z′+Z)+W+ZY′)*

= *X(1+ZY′)=X.1*

F =X

43. Apply De-Morgan's theorem to *[(A+B) + C] ′.*

Given *[(A+B)+C] ′ = (A+B) ′.C′*

= (A′.B′).C′

[(A+B)+C] ′ = A′B′C′

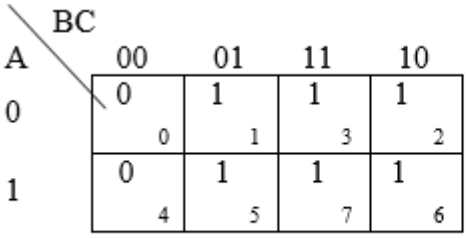
44. Simplify A+AB+A´ +B

A+AB+A ´ +B = A+A´ + AB + B

= 1+ AB + B---------- (X+X ´ =1)

= 1----------(X+1 = 1)

45. Minimize the function using K-map: F=∑m (1, 2, 3, 5, 6, 7)

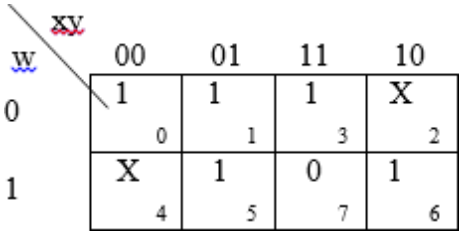


Quad (2,3,6,7) = B

Quad (1,3,5,7) = C

F = B + C

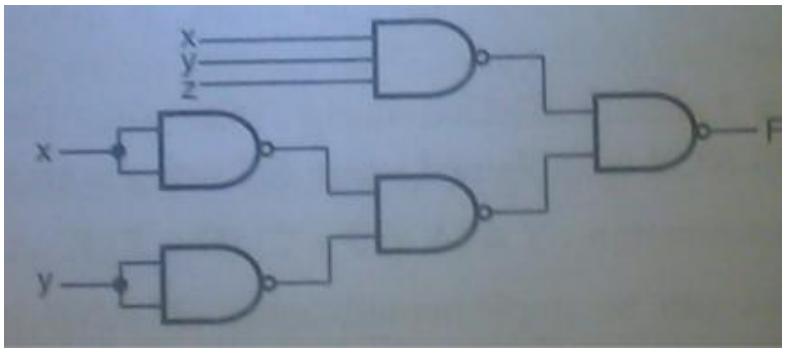
46. Plot the expression on K-map: F (w,x,y) =∑m (0, 1, 3, 5, 6) + d (2, 4)



47. What is Prime Implicant?

A prime implicant is a group of minterms which cannot be combined with any other minterms or groups.

48.* Implement using NAND gates only, *F = x y z + x′ y′.



49. Show that a positive logic NAND gate is a negative logic NOR gate.

Truth Table for NAND Gate		
A	B	Y
0	0	1
0	1	1
1	0	1
1	1	0

≡

Truth Table for Positive Logic NAND Gate		
A	B	Y
LOW	LOW	HIGH
LOW	HIGH	HIGH
HIGH	LOW	HIGH
HIGH	HIGH	LOW

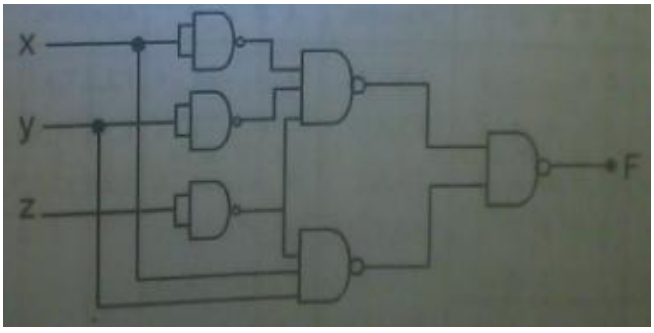
Truth Table for NOR Gate		
A	B	Y
0	0	1
0	1	0
1	0	0
1	1	0

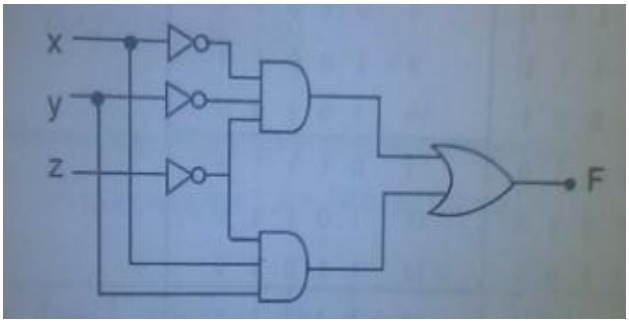
≡

Truth Table for Negtive Logic NOR Gate		
A	B	Y
HIGH	HIGH	LOW
HIGH	LOW	HIGH
LOW	HIGH	HIGH
LOW	LOW	HIGH

Truth table for positive logic NAND gate and negative logic NOR gates are same and hence a positive logic NAND gate is negative logic NOR gate.

50.* Implement the given function using NAND gates *F(x,y,z)= Σm(0,6).





F(x,y,z)=x′y′z′+xyz′

PART B&C

1. (a)Use Karnaugh map method to simplify the following Boolean function F(A,B,C,D)= ∑m(2,4,6,10,12)+ ∑d(0,8,9,13).Implement the booloean function ,F using not more than two NOR gates. (Apr/May'19)

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(b) Implement the following function using Quine McCluskey method F= ∑m(6 7 8 9) +∑d (10,11,12,13,14,15) (Apr/May'19)

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2.(i) Find the MSOP representation for F(A,B,C,D,E) = ∑m(1,4,6,10,20,22,24,26)+ ∑d(0,11,16,27) using K-Map. Draw the circuit of minimal expression using only NAND gates. (Nov/Dec 2018)

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(ii) Implement Y=(AB) ´ + A + (B+C) ´ using NAND gates only. (Nov/Dec 2018)

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3. What are the advantages of using Quine McCluskey method? Determine the minimal sum of products for the Boolean expression F(A,B,C,D) = ∑m(1,2,3,9,12,13,14)+ ∑d(0,7,10,15) using Quine McCluskey Tabular method. (Nov/Dec 2018)

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4. Using K-map find the MSP of F= (0-3, 12-15) +d (7, 11) (April/May17)

Refer"Digital Cicuits and Design " by S.Salivahanan &S.Arivazhagan 2ndEdition,Pg.No.70.

5 (i).State and prove Demorgon ´ s theorem.

Refer"Digital Cicuits and Design " by S.Salivahanan &S.Arivazhagan 2ndEdition,Pg.No.44.

(ii)Find a Min SOP and MinPOS for B ´ C ´ D+BCD+ACD ´ +A ´ B ´ C+A ´ BC ´ D. (Apr/May 17)

Refer"Digital Cicuits and Design " by S.Salivahanan &S.Arivazhagan 2ndEdition,Pg.No.56.

6 .Implement Y = (A+C) (A+D ´) (A+B+C ´) using NOR gates only. (April / May 2017)

Refer"Dig

7. Find the expression for the following function using Quine McCluskey method F=(0,2,3,5,9,11,13,14,16,18,24,26,28,30).(April/May 17)

Refer"Digital Cicuits and Design " by S.Salivahanan &S.Arivazhagan 2ndEdition,Pg.No.68

8. i)Simplify the Boolean expression using laws and rules of Boolean algebra Z = [AB ´ (C+BD)+(AB) ´]C (Nov/Dec 17)

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(ii)Define SOP and POS term. Convert the Boolean expression AB ´ C+B ´ CD+AC ´ D to SOP(Nov/Dec 17)

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9. Implement the Boolean expression using minimum number of 3 input NAND gate f(A,B,C,D)=Sum(1,2,3,4,7,9,10,12)

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10.Simplify the following Boolean function F, using Quine Mc Cluskey method and verify the results using K-map F(A,B,C,D)=∑(0,2,3,5,7,9,11,13,14). (May/June ´ 16)

Refer"Digital Cicuits and Design " by S.Salivahanan &S.Arivazhagan 2ndEdition,Pg.No.68

11. Find the MSOP representation for F(A,B,C,D,E)= ∑(1,4,6,10,20,22,24,26)+d(0,11,16,27) using K-map method. Draw the circuit of minimal expression using only NAND gates.

Refer"Digital Cicuits and Design " by S.Salivahanan &S.Arivazhagan 2ndEdition,Pg.No.67

12. What are the advantages of using tabulation method? Determine the minimal sum of products using for the Boolean expression F=∑(1,2,3,7,8,9,10,11,14,15)using tabulation method. (Nov/Dec 16)

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13. Minimize the following logic function using K-maps and realize using NAND and NOR gates. F(A,B,C,D) = ∑m(1,3,5,8,9,11,15)+d(2,13)

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14. Realize NOT, OR, AND gates using universal gates.

Refer"Digital Cicuits and Design " by S.Salivahanan &S.Arivazhagan 2nd Edition,Pg.No.84&85

15.Simplify using Quine McClusky method and verify the result using K-map F=∑(0,1,2,5,7,8,9,10,13,15) (April/May 2015)

Refer"Digital Cicuits and Design " by S.Salivahanan &S.Arivazhagan 2nd Edition,Pg.No.68

16. (i) Express the Boolean functions F=A+B'C in a sum of minterms.

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(ii)Simplify the following Boolean expression using Boolean algebra. (a) x'y'z+x'yz+xy' (b) xyz+x'z+yz (April/May 2015)

Refer"Digital Cicuits and Design " by S.Salivahanan &S.Arivazhagan 2nd Edition,Pg.No.46

17.(i).Given Y(A,B,C,D)= ∏M(0,1,3,5,7,10,14,15), draw the K-map and obtain the simplified expression. Realize the minimum expression using basic gates.

Refer"Digital Cicuits and Design " by S.Salivahanan &S.Arivazhagan 2nd Edition,Pg.No.63

(ii) Implement the expression Y(A,B,C)= ∏M(0,2,4,5,6) using only NOR-NOR logic.

Refer"Digital Cicuits and Design " by S.Salivahanan &S.Arivazhagan 2nd Edition,Pg.No.93

(iii)Implement EXOR gate using only NAND gate. (May/June '14)

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18. Simplify the following function using Tabulation method Y(A,B,C,D) =Σm(0,1,2,5,6,7,8,9,10,14) and implement using only NAND gates. (May/June '14)

Refer"Digital Cicuits and Design " by S.Salivahanan &S.Arivazhagan 2nd Edition,Pg.No.68&91

19. Draw the multiple- level two input NAND circuit for the following expression: F= (AB ´ +CD ´) E+BC (A+B) (Nov/Dec 2014)

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20 (i)Convert the following function into product of Max-terms.

F (A, B, C)=(A+B ´)(B+C) ´ (A+C ´)

Refer"Digital Cicuits and Design " by S.Salivahanan &S.Arivazhagan 2nd Edition,Pg.No.54

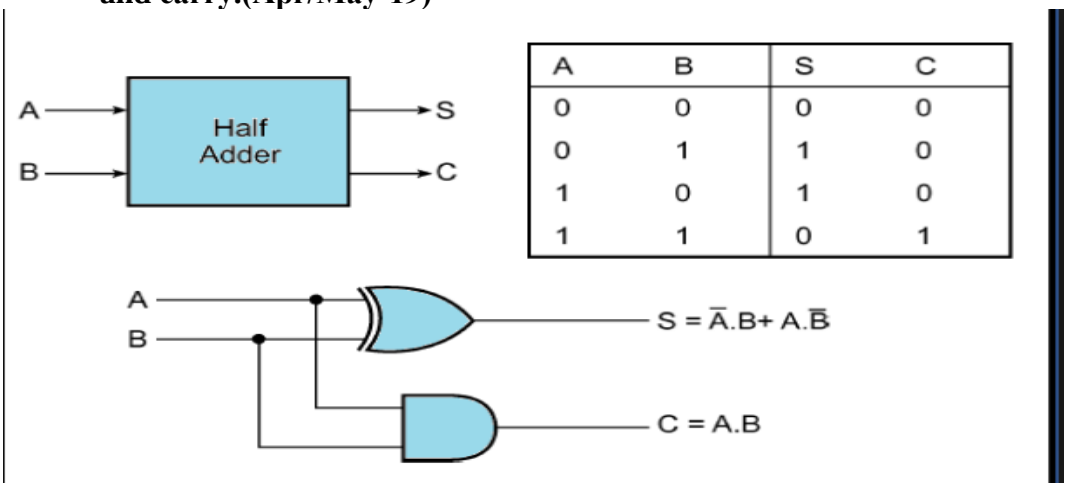
(ii) Using Quine McClusky method simplify the given function

F(A,B,C,D)=∑m(0,2,3,5,7,9,11, 13,14) (Nov/Dec 2014).

Refer"Digital Cicuits and Design "by S.Salivahanan &S.Arivazhagan 2nd Edition,Pg.No.68

UNIT – II COMBINATIONAL CIRCUIT DESIGN

1. Draw the truth table for a half adder circuit and write the Boolean expressions for sum and carry.(Apr/May'19)



A	B	S	C
0	0	0	0
0	1	1	0
1	0	1	0
1	1	0	1

2. What is meant by a decoder circuit?(Apr/May'19)

A binary decoder is a combinational logic circuit that converts binary information from the n coded inputs to a maximum of 2^n unique outputs

3. Draw the full adder using two half Adders (Nov/Dec 2017) (Nov/Dec 2018)

An adder is a digital circuit that performs addition of numbers. The half adder adds two binary digits called as augend and addend and produces two outputs as sum and carry; XOR is applied to both inputs to produce sum and AND gate is applied to both inputs to produce carry.

$S=A\oplus B\oplus C, \qquad C_{out}= AB + (A\oplus B)C_{in}.$

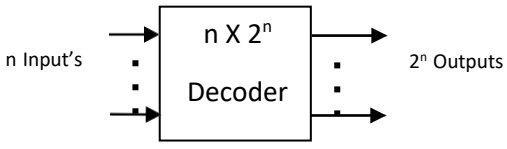
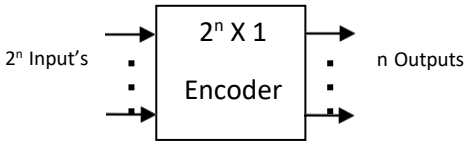
4. What do you mean by parity checker? (Nov/Dec 2018)

The parity checker is a combinational circuit that determines if the received data is correct or not. It is good for detecting a single bit error only. The parity checker can be built using Exclusive-OR gate.

5. Write the function of Magnitude comparator. (Nov/Dec 2017)

A digital comparator or magnitude comparator is a hardware electronic device that takes two numbers as input in binary form and determines whether one number is greater than, less than or equal to the other number. Comparators are used in central processing units (CPUs) and microcontrollers (MCUs).

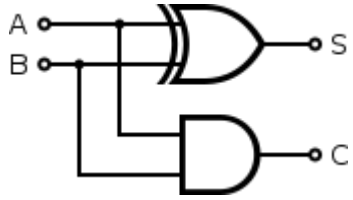
6. Compare the function of Decoder and Encoder. (April/May 2017)

S.No	Decoder	Encoder
1	Block diagram: 	
2	A decoder is a combinational circuit that converts binary information from n input lines to a maximum of 2^n unique output lines.	An encoder is a digital circuit that performs the reverse operation of a decoder. An encoder has 2^n input lines and n output lines.
3	A decoder accepts a set of binary inputs and activates only the output that corresponds to that input number.	An encoder generates the binary code corresponding to the input activated.
4	Example: Binary to Octal decoder	Example: Octal to Binary encoder.

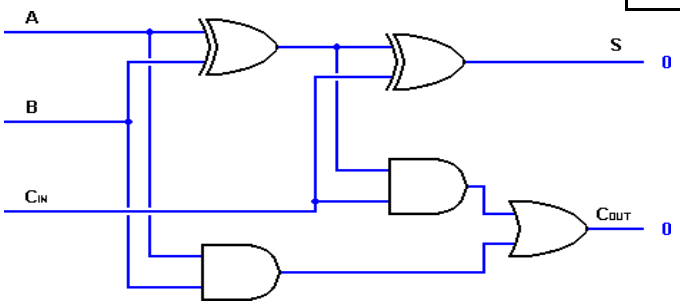
7. Give the truth table for half adder and write the expression for sum and carry. (Nov/Dec 2015) or Draw the truth table and logic circuit of half adder. (April/May 2017)

A half adder is a logical circuit that performs an addition operation on two binary digits. The half adder produces a sum and a carry value which are both binary digits. The drawback of this circuit is that in case of a multibit addition, it cannot include a carry. $S=A\oplus B$ and $C= AB$. Following is the logic table

for a half adder:



A	B	C	S
0	0	0	0
0	1	0	1
1	0	0	1
1	1	1	0

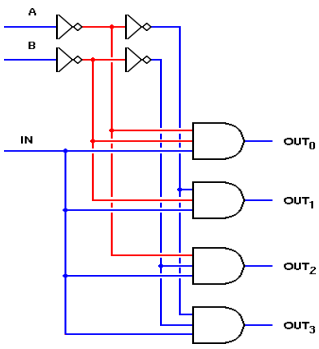


8. Write the design procedure of combinational circuit. (May/June 2016) (Nov/Dec 2016)

The design procedure for combinational logic circuits starts with the problem specification and comprises the following steps:

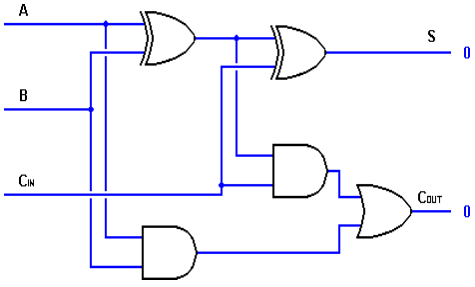
1. Determine required number of inputs and outputs from the specifications.
2. Derive the truth table for each of the outputs based on their relationships to the input.
3. Simplify the Boolean expression for each output. Use Karnaugh Maps or Boolean algebra.
4. Draw a logic diagram that represents the simplified Boolean expression. Verify the design by analyzing or simulating the circuit.

9. Convert a two-to-four line decoder with enable input to 1X4 demultiplexer (Nov/Dec 2014). Draw the combinational circuit that converts 2 coded inputs into 4 coded outputs. (May/June '16)



10. Draw the logic diagram and truth table of Full adder. (Nov/Dec 2016)

INPUT			OUTPUT	
A	**B**	**Cin**	**S**	**Cout**
0	0	0	0	0
0	0	1	1	0
0	1	0	1	0
0	1	1	0	1
1	0	0	1	0
1	0	1	0	1
1	1	0	0	1
1	1	1	1	1



11. Write about the design procedure for combinational circuits(Nov/Dec 2016)

A combinational circuit consists of logic gates whose outputs at any time are determined from the present combination of inputs.

Design procedure

Step 1: Problem definition

Step 2: Determine the no. of available input variables and output variables.

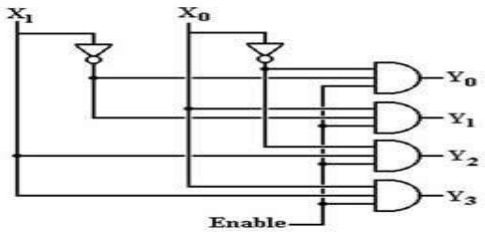
Step 3: Assigning letter symbols to I/O variables.

Step 4:Obtain simplified Boolean expression for each o/p.

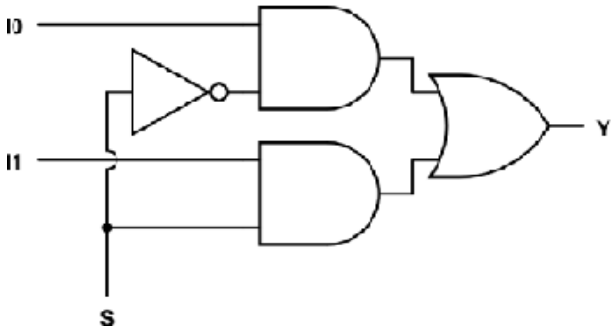
Step 5: Draw the logic diagram.

12. What is priority encoder? (May/June 2014, Nov/Dec 2015)

A priority encoder is an encoder circuit that includes the priority function. The operation of the priority encoder is such that if two or more inputs are activated at the same time, the output binary code will be generated to the highest-numbered input.

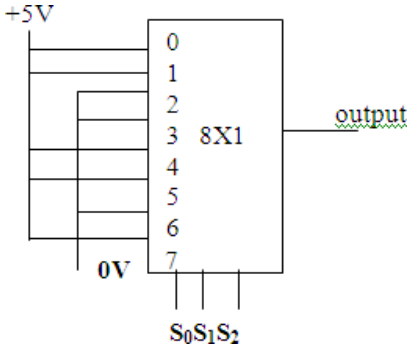


13. Draw a 2 to 1 multiplexer circuit (Apr/May 2015)(May/June 2013)



S	Y
0	$I0$
0	$I1$

14. Implement the function f = ∑ m(0,1,4,5,7) using 8:1 MUX . (Nov/Dec 2014)

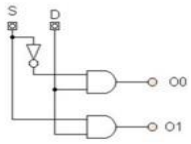


15. Draw a 1 to 2-demultiplexer circuit. (Nov/Dec 2013)

- Truth Table

S	D	O_1	O_0
0	0	0	0
0	1	0	1
1	0	0	0
1	1	1	0

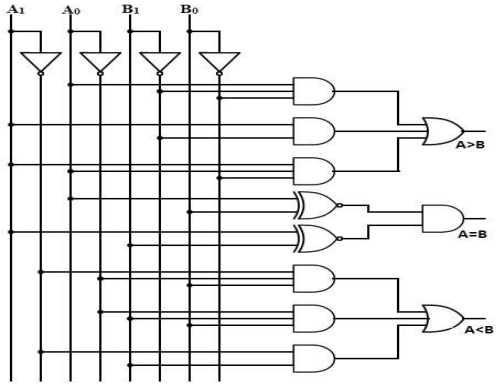
- Circuit



16. What is demux? (Nov//Dec 13)

Demultiplexer is a circuit that receives information on a single line and transmits this information on one of 2n possible output lines. A demultiplexer is a decoder with an enable input.

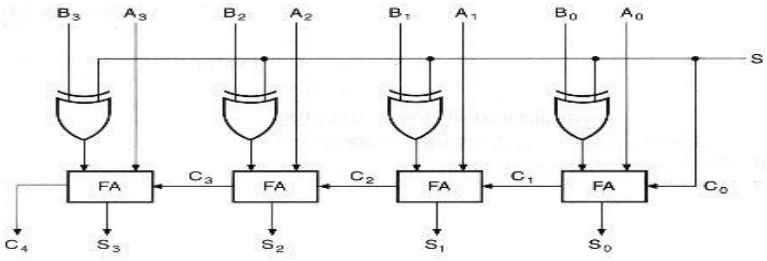
17. Draw the two bit comparator circuit using logic gates. (May/June 2015).



18. Distinguish between a decoder and a demultiplexer. (May/June 2015)

S.No	DEMUX	DECODER
1.	A demultiplexer is a circuit that receives information on a single line and transmits this information on one of many output lines	A decoder accepts a set of binary inputs and activates only the output that corresponds to that input number.
2.	Data Distributor	Decoder with enable input is used as demultiplexer.

19. Construct a 4-bit parallel adder/subtractor circuit using Full adders and XOR gates. (Nov/Dec 2014).



S-Select input. S=0 addition operation, S=1 subtraction operation.

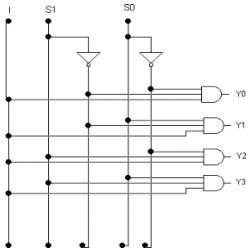
20. Define priority encoder. (May/June 2014)

Encoders establish an input priority to ensure that only the highest-priority input line is encoded. If priority is given to an input with higher subscript number over one with lower subscript number, then if both D2 and D5 are logic-1 simultaneously, the output will be 101 because D5 has a higher priority over D2.

Inputs								Outputs		
D0	D1	D2	D3	D4	D5	D6	D7	X	y	z
1	0	0	0	0	0	0	0	0	0	0
X	1	0	0	0	0	0	0	0	0	1
X	X	1	0	0	0	0	0	0	1	0
X	X	X	1	0	0	0	0	0	1	1
X	X	X	X	1	0	0	0	1	0	0
X	X	X	X	X	1	0	0	X	1	0	1
X	X	X	X	X	1	0	X	1	1	0
X	X	X	X	X	X	1		1	1	1

21. Draw the logic diagram of a one to four line demultiplexer. (May/June 2013)

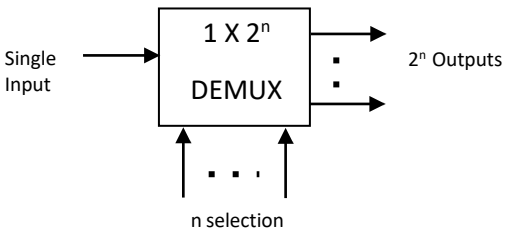
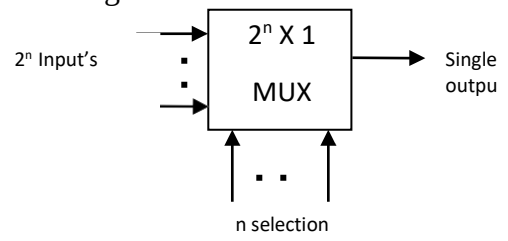
1 to 4 line Demultiplexer:



22. Distinguish between combinational logic and sequential logic.

S.No	Combinational logic circuit	Sequential logic circuit
1	It consists of input signal, gates and output signals	It consists of a combinational circuit to which memory elements are connected to form a feedback path.
2	The outputs at any instant of time are entirely dependent upon the inputs present at that time.	The outputs dependent not only on the present input variables, but also depend upon the past value of the input variables.
3	Combinational circuits are faster in speed	Sequential circuits are slower than the combinational circuits.
4	Combinational circuits are easy to design	Sequential circuits are comparatively harder to design
5	Example: Parallel adder, Code converter, Decoder	Example: Serial Adder, Counter, shift register

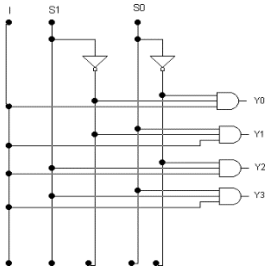
23. Mention the difference between a DEMUX and a MUX

S.No	DEMUX	MUX
1	A demultiplexer is a circuit that receives information on a single line and transmits this information on one of many output lines	A digital multiplexer is a combinational circuit that selects binary information from one of many input lines and directs it to a single output line.
2	Data Distributor	Data selector
3	Block diagram 	Block diagram 

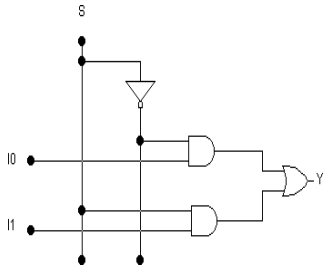
24. State the condition to check the equality of two n-bit binary numbers A and B.

A = A_{n-1} ……. A_3 A_2 A_1 A_0, B = B_{n-1} ……. B_3 B_2 B_1 B_0. The two numbers are equal if all pairs of significant bits are equal. The equality relation of each pair of bits can be expressed logically with an equivalence function (X-NOR): $\mathbf{X_i = A_iB_i + A_i' B_i'}$, where

i = 0, 1, 2, 3, …….(n-1). The condition to check the equality of two n-bit binary numbers is $\mathbf{R_{(A=B)} = X_{n-1} X_{n-2} ..... X_3X_2X_1X_0}$. If $R_{(A=B)}$ =1, the two numbers A and B are equal, otherwise they are unequal.



25. Draw a 2 to 1 multiplexer circuit.

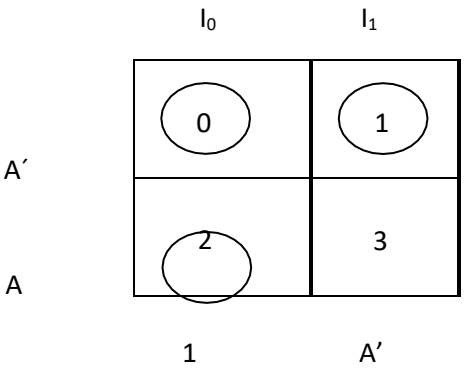


26. Implement 2 input NAND gate function y = (AB)´ using a 2:1 MUX.

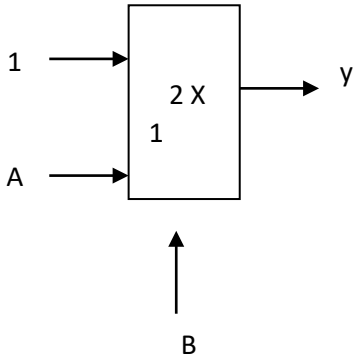
Truth table

A	B	y
0	0	1
0	1	1
1	0	1
1	1	0

Implementation table



Logic diagram



27. Give some of the major applications of multiplexers.

Data selection, Data routing, Operation sequencing, Parallel to serial conversion, Waveform generation, Logic-function generation.

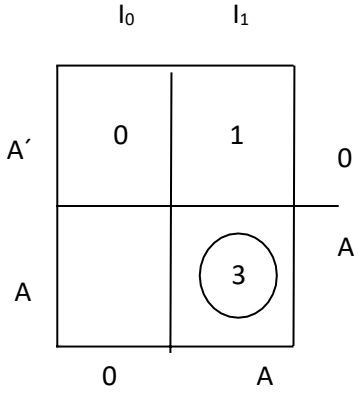
28. How can a DEMUX be used as a decoder?

The selection lines of the DEMUX can be used as input lines of decoder and if the data input of the demultiplexer is used as the enable input of the decoder then we can use the demultiplexer as a decoder.

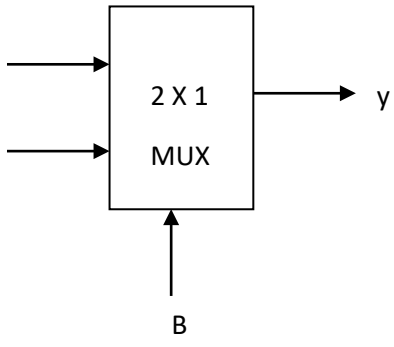
29. Realize AND and OR function using 2:1 MUX.

Implementation of AND function:

A	B	y
0	0	0
0	1	0
1	0	0
1	1	1



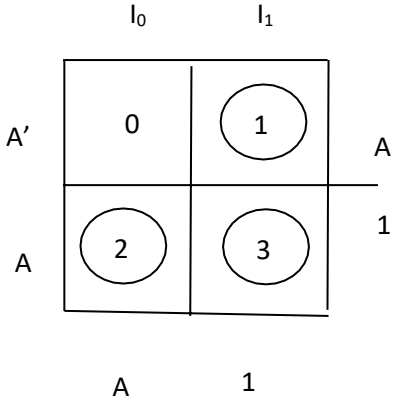
Logic diagram



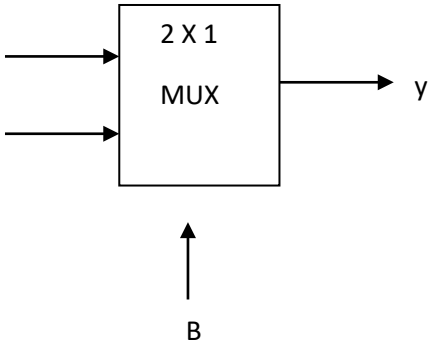
Implementation of OR function:

Truth table

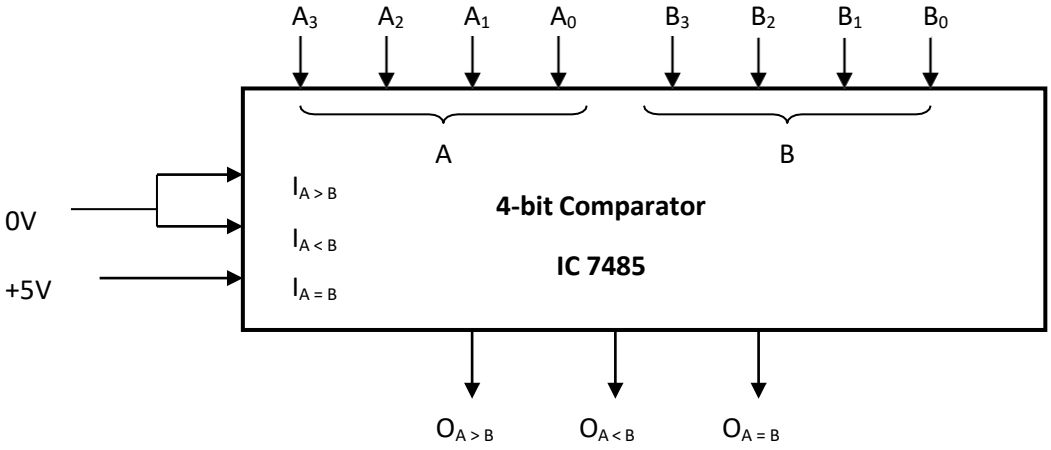
A	B	y
0	0	0
0	1	1
1	0	1
1	1	1



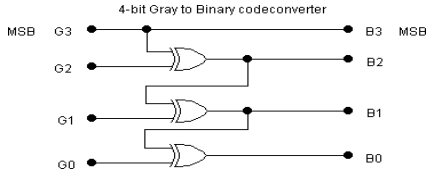
Logic diagram

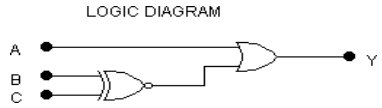


30. Using a single IC 7485, draw the logic diagram of a 4-bit comparator.

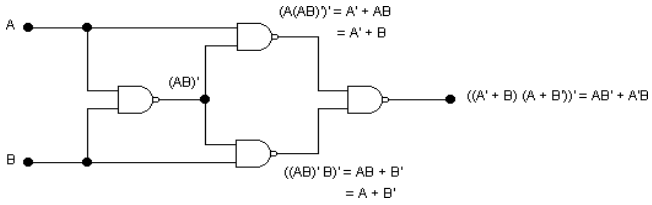


31. Draw the 4 bit Gray to Binary code converter.

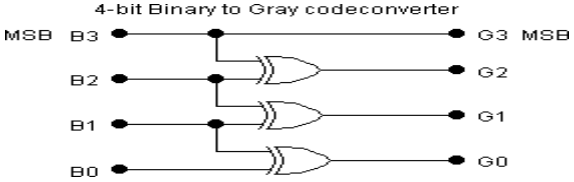




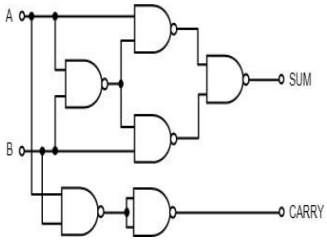
32. Realize XOR function using only NAND gates.

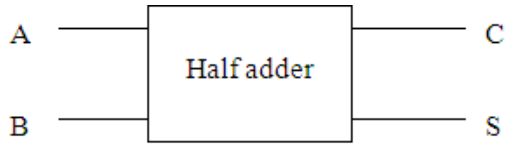


33. Draw the 4 bit Binary to Gray code converter.

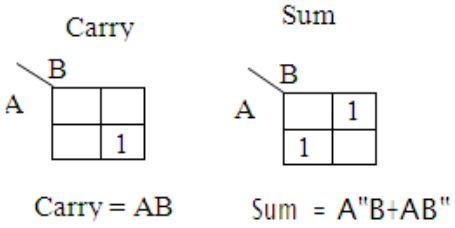


34. Implement half Adder using NAND Gates. (May/June 2013)





Inputs		Y = A+ B	
A	B	carry	Sum
0	0	0	0
0	1	0	1
1	0	0	1
1	1	1	0

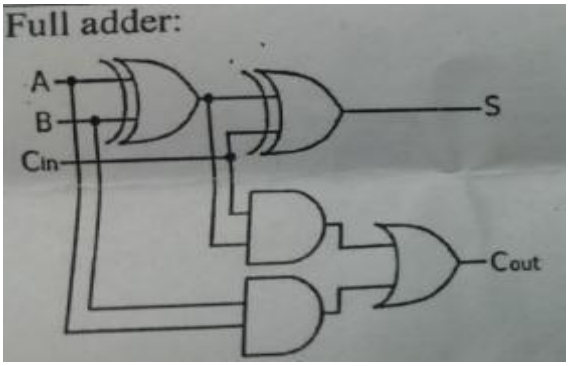


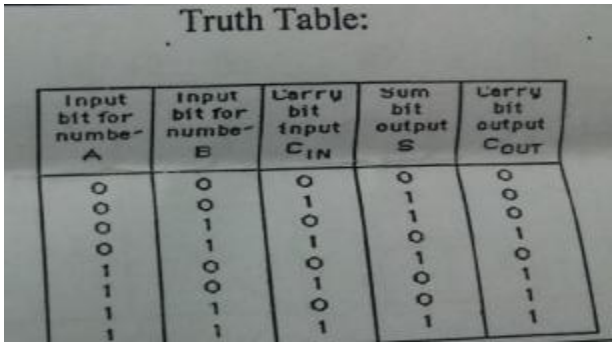
35. List the applications of decoders.

Decoders are used in counter systems, A/D conversion, D/A conversion and in seven segment digital displays.

36. Derive the expression for sum and carry of a half adder.

37. Draw the logic diagram and truth table of Full adder.



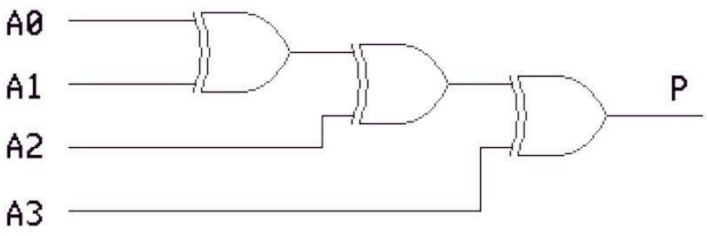


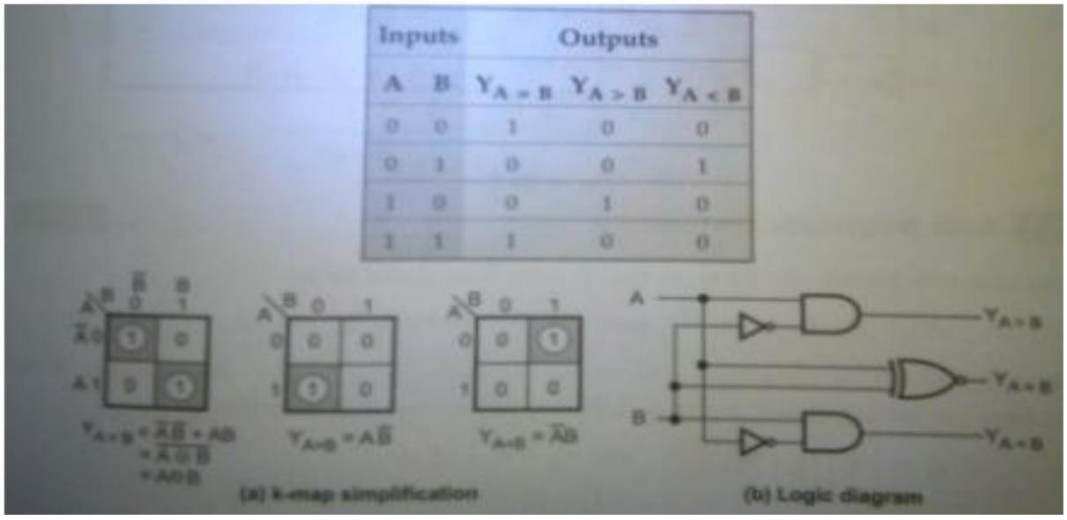
38. Write an expression for borrow and difference in a full subtractor circuit.

Difference = A′B+AB′=A⊕B

Borrow = A′B

39. Design a single bit magnitude comparator to compare two words A and B.





40. What is an encoder?

An encoder has 2^n input lines and n output lines. In encoder the output lines generate the binary code corresponding to the input value.

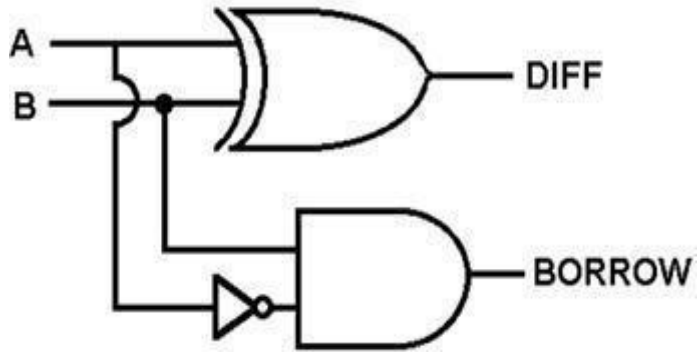
41. Define a Decoder.

A **binary decoder** is a combinational logic circuit that converts binary information from the n coded inputs to a maximum of 2^n unique outputs.

42. List few applications of multiplexer.

- □ Data Selector.
- □ Implement combinational logic circuit.
- □ Time multiplexing systems
- □ Frequency multiplexing systems.
- □ D/A and A/D converter
- □ Data acquisition systems.

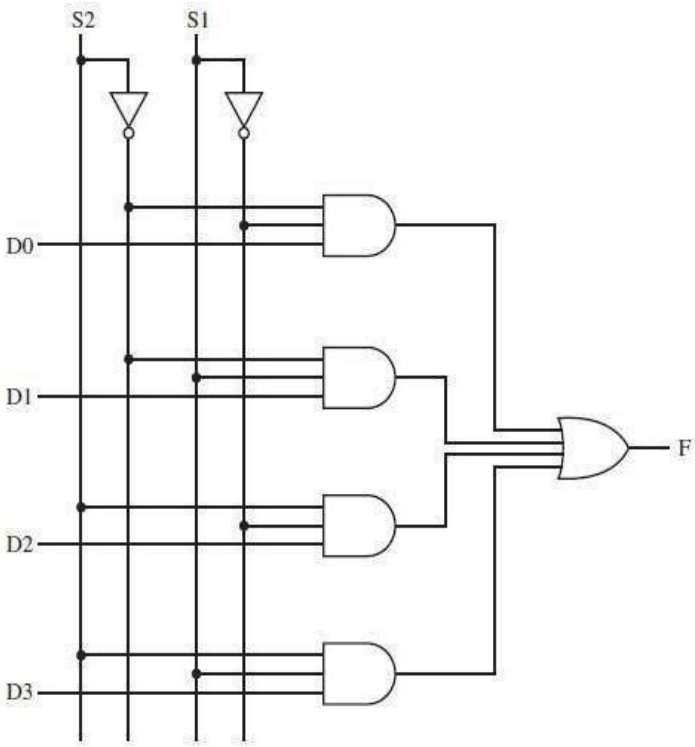
43. Design a half subtractor using basic gates.



Difference=A′B+AB′=A⊕B

Borrow=A′B

44. Draw the logic diagram of a 4 line to 1 line multiplexer.



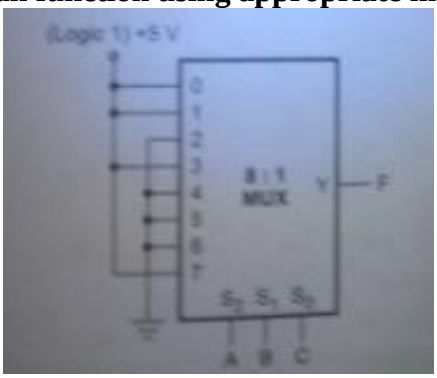
45. Suggest a solution to overcome the limitation on the speed of an adder.

It is possible to increase speed of adder by eliminating inter-stage carry delay. This method utilizes logic gates to look at the lower-order bits of the augend and addend to see if a higher-order carry is to be generated.

46. Relate carry generate, Carry propagate, Sum and Carry-out of a Carry look a head adder.

$$P_i = A_i \oplus B_i$$
$$G_i = A_i \cdot B_i$$
$$C_{i+1} = G_i + (P_i \cdot C_i)$$
$$C_1 = G_0 + P_0 \cdot C_0$$
$$C_2 = G_1 + G_0 \cdot P_1 + C_0 \cdot P_0 \cdot P_1$$
$$C_3 = G_2 + G_1 \cdot P_2 + G_0 \cdot P_1 \cdot P_2 + C_0 \cdot P_0 \cdot P_1 \cdot P_2$$
$$C_4 = G_3 + G_2 \cdot P_3 + G_1 \cdot P_2 \cdot P_3 + G_0 \cdot P_1 \cdot P_2 \cdot P_3 + C_0 \cdot P_0 \cdot P_1 \cdot P_2 \cdot P_3$$

47. **Realize the Boolean function using appropriate multiplexer *F(A,B,C)= Σ (0,1,3,7)***



48. Compare the performance of binary serial and paralleladders.

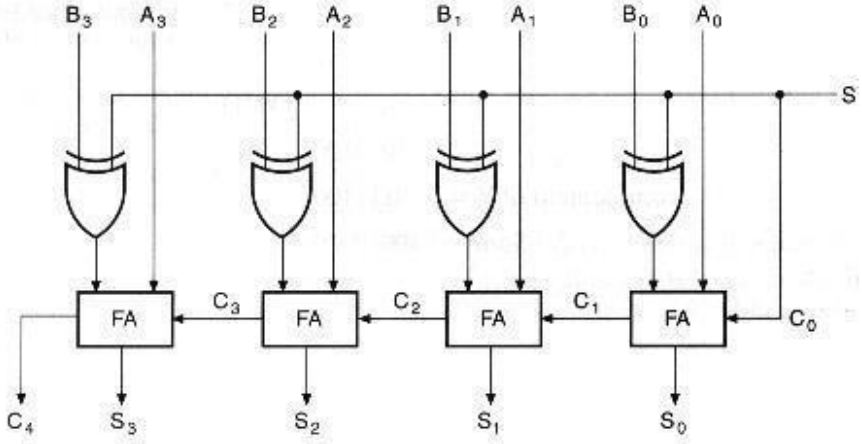
- □ Serial adder uses shift registers
- □ The serial adder requires only one full adder circuit

- □ The serial adder is a sequential circuit
- □ Time required for addition depends on the number of bits
- □ It is slower

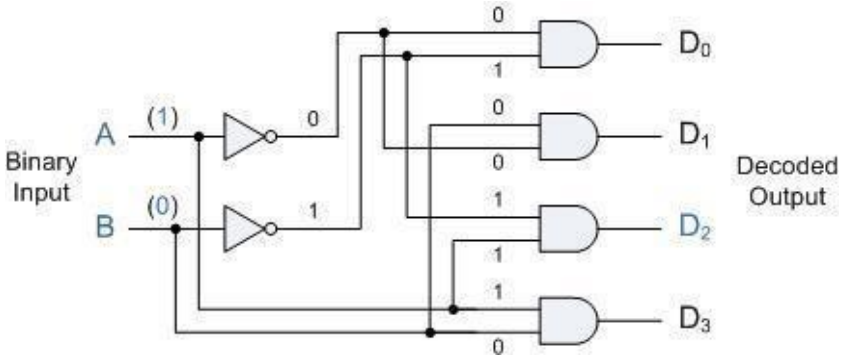
Parallel
Adder

- □ Parallel adder uses registers with parallel load capacity
- □ It is faster
- □ Time required for addition does not depend on number of bits
- □ Excluding the registers, the parallel adder is a purely combinational circuit

49. Construct a two-4-bit parallel adder/subtractor using Full Adders and XOR gates.



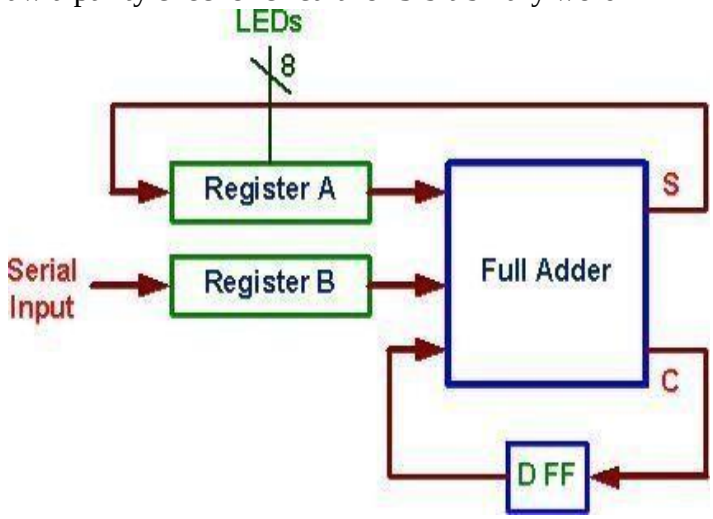
50. Convert a two-to-four line decoder with enable input to 1X4 Demultipexer



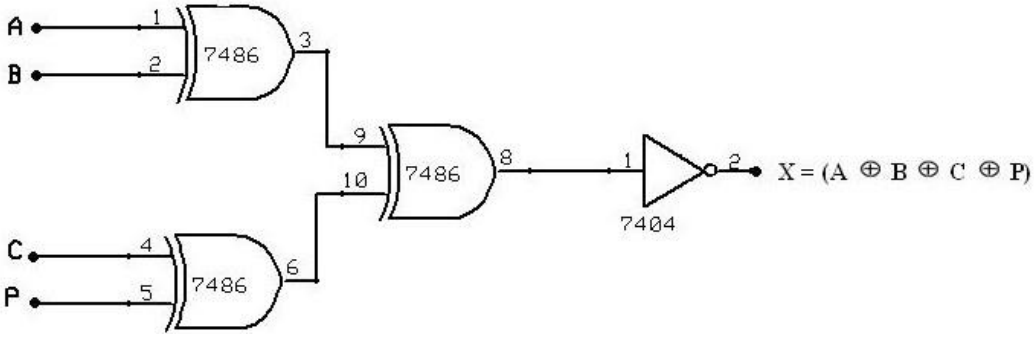
51. Draw the logic diagram of serial adder.

Draw a parity checker circuit for 3 bit binary word x1 x2 x3.

Draw a parity checker circuit for 3 bit binary word x1 x2 x3.



52. Draw a parity checker circuit for 3 bit binary word x1 x2 x3.



53. Define BCD adder.

A 4-bit binary adder that is capable of adding two 4-bit words having a BCD (binary-coded decimal) format. The result of the addition is a BCD-format 4-bit output word, representing the decimal sum of the addend and augend, and a carry that is generated if this sum exceeds a decimal value of 9.

54. Why carrylookahead adder is called as fast adder?

A **carry-lookahead adder** (**CLA**) or **fast adder** is a type of adder used in digital logic. A carry-look ahead adder improves speed by reducing the amount of time required to determine carry bits. It can be contrasted with the simpler, but usually slower, ripple-carry adder (RCA), for which the carry bit is calculated alongside the sum bit, and each stage must wait until the previous carry bit has been calculated to begin calculating its own sum bit and carry bit. The carry-lookahead adder calculates oneor more carry bits before the sum, which reduces the wait time to calculate the result of the larger-value bits of the adder.

PART B&C

1. With a neat diagram explain the working of a four bit adder – subtractor circuit . (Apr/May'19)

Refer "Digital Design " by Morris Mano,4th Edition Pg.No:541

2. With a truth table and logic diagram explain the operation of a four input priority encoder. (Apr/May'19)

Refer "Digital Design " by Morris Mano,4th Edition Pg.No:167

3 (i) With neat circuit diagram, explain the working principle of 4-bit parallel Adder/Subtractor? (Nov/Dec 2018)

Refer "Digital Design " by Morris Mano,4th Edition Pg.No:143

(ii) Illustrate the concept of basic 4-input Multiplexer. (Nov/Dec 2018)

Refer "Digital Design " by Morris Mano,4th Edition Pg.No:169

4. Design and describe the operation of 3-bit magnitude comparator. (Nov/Dec 2018)

Refer "Digital Design " by Morris Mano,4th Edition Pg.No:169

5. Design an even parity generator, that generates an even parity bit for every input string of 3-bits. (Nov/Dec 2018)

Refer"Digital Cicuits and Design " by S.Salivahanan &S.Arivazhagan 2nd Edition,Pg.No.229

6. Design a 4 bit BCD adder using full adder and explain its structure and compute the circuit to add 1001 and 0101. Write the sum and carry output of the given binary number.(Nov/Dec 2017)

Refer"Digital Cicuits and Design " by S.Salivahanan &S.Arivazhagan 2nd Edition,Pg.No.178

7. i)Explain the operation and need of priority encoder. (Nov/Dec 2017)

Refer"Digital Cicuits and Design " by S.Salivahanan &S.Arivazhagan 2nd Edition,Pg.No.223

(ii)Design a 5 X 32 decoder using 3 X 8 decoder and summarize how many decoders are required for the design? (Nov/Dec 2017)

Refer"Digital Cicuits and Design " by S.Salivahanan &S.Arivazhagan 2nd Edition,Pg.No.212

8. (i)Why does a good logic designer minimize the use of NOT gates?

(ii)Show that if all the logic gates in a two level AND-OR gate networks are replaced by NAND gates the output function does not change. (April/May ´ 17)

Refer"Digital Cicuits and Design " by S.Salivahanan &S.Arivazhagan 2nd Edition,Pg.No.99

9.(i)Design a 4-bit magnitude comparator with 3 outputs: A>B,A<B,A=B.

Refer "Digital Design " by Morris Mano,4th Edition Pg.No:160

(ii) Design a 4-bit binary to gray code converter. (May/June 2016)

Refer"Digital Cicuits and Design " by S.Salivahanan &S.Arivazhagan 2nd Edition,Pg.No.236

10.(i)Implement the following Boolean function using 8×1 multiplexer. F(A,B,C,D)= ∑(1,3,4,11,12,13,14,15).

Refer"Digital Cicuits and Design " by S.Salivahanan &S.Arivazhagan 2nd Edition,Pg.No.195

(ii)Explain the concept of carry look ahead adder with neat diagram. (May/June 2016)

Refer"Digital Cicuits and Design " by S.Salivahanan &S.Arivazhagan 2nd Edition,Pg.No.173

11. (i)Design and explain 1 of 8 demultiplexer

Refer"Digital Cicuits and Design " by S.Salivahanan &S.Arivazhagan 2nd Edition,Pg.No.200

(ii)What is parity checker? (Nov/Dec 2016)

Refer"Digital Cicuits and Design " by S.Salivahanan &S.Arivazhagan 2nd Edition,Pg.No.228

12.Explain with the neat diagram the function of the Binary multiplier

(i) using shift method

Refer"Digital Cicuits and Design " by S.Salivahanan &S.Arivazhagan 2nd Edition,Pg.No.181

(ii) parallel multiplier (Nov/Dec 2015)

Refer"Digital Cicuits and Design " by S.Salivahanan &S.Arivazhagan 2nd Edition,Pg.No.182

13.Design a BCD to excess-3 code converter using minimum number of NAND gates. (Nov/Dec 2015)

Refer"Digital Cicuits and Design " by S.Salivahanan &S.Arivazhagan 2nd Edition,Pg.No 236

14.(i)Design 4 * 1 multiplexer circuit.

Refer"Digital Cicuits and Design " by S.Salivahanan &S.Arivazhagan 2nd Edition,Pg.No.382

(ii) Implement the function using multiplexer F = ∑(0,1,3,4,8,9,15) (April/May 2015)

Refer"Digital Cicuits and Design " by S.Salivahanan &S.Arivazhagan 2nd Edition,Pg.No.195

15 (i) Draw the logic diagram of binary to octal decoder and explain the working in detail.

Refer"Digital Cicuits and Design " by S.Salivahanan &S.Arivazhagan 2nd Edition,Pg.No.206

(ii) How is carry look ahead adder faster than a ripple carry adder? Explain in detail with neat sketches. (April/May 2015)

Refer"Digital Cicuits and Design " by S.Salivahanan &S.Arivazhagan 2nd Edition,Pg.No.173

16. (i)Design a 3:8 decoder using basic gates.

Refer"Digital Cicuits and Design " by S.Salivahanan &S.Arivazhagan 2nd Edition,Pg.No. 206

(ii) Design a binary to gray code converter. (May/June 2014)

Refer"Digital Cicuits and Design " by S.Salivahanan &S.Arivazhagan 2nd Edition,Pg.No. 236

17. (i)Design a Full subtractor using Demultiplexer.

Refer"Digital Cicuits and Design " by S.Salivahanan &S.Arivazhagan 2nd Edition,Pg.No. 201

(ii)Explain the working of carry-look ahead adder. (May/June 2014)

Refer"Digital Cicuits and Design " by S.Salivahanan &S.Arivazhagan 2nd Edition,Pg.No. 173

18. (i).Design 4-bit magnitude comparator with three outputs A>B, A<B and A=B.

Refer “Digital Design “ by Morris Mano,4th Edition Pg.No:160

(ii)Construct a 4-bit even parity generator circuit using logic gates.(Nov/Dec 2014).

Refer”Digital Cicuits and Design “ by S.Salivahanan &S.Arivazhagan 2nd Edition,Pg.No. 229

19. (i) Design a BCD adder to add two BCD digits.(or) Design a 4-bit decimal adder using 4-bit binary adders. (May/June 2013, Nov/Dec 2014).

Refer”Digital Cicuits and Design “ by S.Salivahanan &S.Arivazhagan 2nd Edition,Pg.No. 178

(ii) Implement the following function using Multiplexers

F(A,B,C,D)= ∑m(0,1,3,4,8,9,15)

Refer”Digital Cicuits and Design “ by S.Salivahanan &S.Arivazhagan 2nd Edition,Pg.No.195

20.Design and explain the working of a half Subtractor and full subtractor. (Nov/Dec 2012)

Refer”Digital Cicuits and Design “ by S.Salivahanan &S.Arivazhagan 2nd Edition,Pg.No.165&166

21. (i) Explain in detail a 4 – bit parallel adder/subtractor.

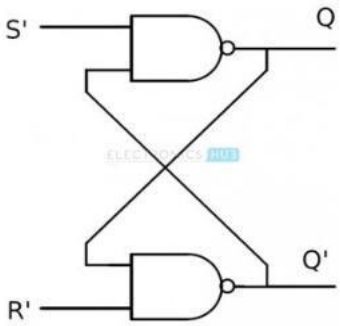
Refer “Digital Design “ by Morris Mano,4th Edition Pg.No:541

(ii) How can a full adder be constructed with two half adders and one OR gate.

Refer”Digital Cicuits and Design “ by S.Salivahanan &S.Arivazhagan 2nd Edition,Pg.No.163

UNIT – III SYNCHRONOUS SEQUENTIAL CIRCUITS

1. Draw the logic diagram and function table of a SR latch implemented using NAND gates. (Apr/May'19)



$\bar{S}$	$\bar{R}$	Q	State
1	1	Previous State	No change
1	0	0	Reset
0	1	1	Set
0	0	?	Forbidden

2. How many flip flops will be complemented in a 10- bit ripple counter to reach the next count after this count of '1001100111'?(Apr/May'19)

4 flipflops need to be complemented.

To calculate the number of flip-flops that will be complemented in a 10-bit binary counter to reach the next count after the given one is:

- Add 1 to the given binary number.
- And see how many bits have toggled to generate the next sequence.
- The number of bits that has changed is the number of flip-flops required to reach the next counter.

Add 1 to the binary number 1001100111.

```
1001100111
+          1
----------
1001101000
----------
```

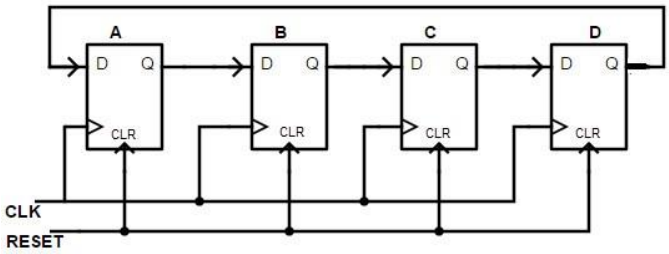
- Four bits have toggled to generate the next sequence.
- Therefore **four** flip-flops must be complemented to reach the next sequence.

3. Define shift register. (Nov/Dec 2018)

Shift register: A register capable of shifting its binary information either from right to left or left to right is known as shift register. It consists of flip-flops connected in cascade. All flip-flops receive a common clock pulse which causes the shift from one stage to the next stage. It is of four basic types: 1. Serial in serial out register, 2. Serial in parallel out register 3. Parallel in serial out register and 4. Parallel in parallel out register. Bi-directional shift register and Universal shift registers are also used fordifferent applications.

4. Draw the circuit diagram of 4-bit ring counter using D ´ -flip flop. (Nov/Dec 2018)

A ring counter is a digital circuit which consists of a series of flip flops connected together in a feedback manner. The circuit is special type of shift register where the output of the last flip-flop is fed back to the input of first flip-flop. When the circuit is reset, except one of the flip-flop output, all others are made zero. For n-flip-flop ring counter we have a **MOD-n counter**. That means the counter has n different states. The circuit diagram for a 4 bit ring counter is shown below:



5. **What are the classifications of sequential circuits? (Nov /Dec 2015),(Nov/Dec 2017)**

Mealy and Moore machines are two models of clocked or synchronous sequential circuit.

Mealy machine: The output depends on both the present state of the flip-flops and on the inputs.

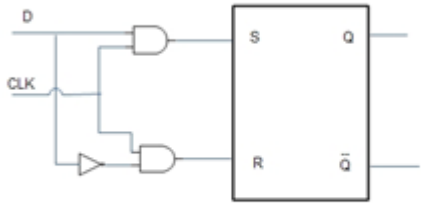
Moore machine: The output depends only on the present state of the flip-flops.

6. **How does ripple counter differ from synchronous counter? (May/June 2014) (May/June 2016), Nov/Dec 2017)**

Synchronous Counter	**Asynchronous Counter**
1. Simultaneous clock pulse is given to all the flip-flops.	1. Clock pulse is given to first flip-flop and the output of first flip-flop acts as a clock to the next and so on.
2. Fast compared to asynchronous counters.	2. Slow compared to synchronous counters because 2nd flip-flop has to wait until the 1st flip-flop gives the output.
3. Additional combinational circuit is required for its designing. This circuit becomes complex.	3. Circuit is simple compared to synchronous counters.
4. Frequency of operation can be much higher than the asynchronous counters.	4. Frequency of operation is lesser than the synchronous counters.
5. Parallel Counter	5.Serial counter

7. **Derive the characteristic equation of a D – Flip flop. (April/May 2017)**

D Flip Flop Circuit



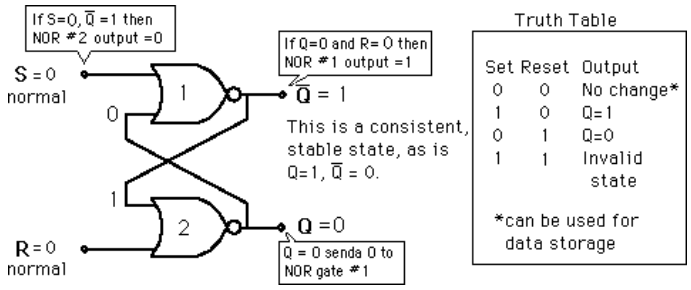
Characteristic Equation

$Q_{t+1} = D\bar{Q} + DQ$

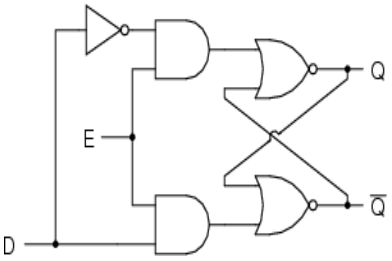
D Flip Flop Characteristic Table

Input	Present State	Next State
D	Q_t	Q_{t+1}
0	0	0
0	1	0

8. **Draw the NOR gate Latch and write its truth table.(Nov/Dec .17)**



9. Give the truth table of transparent latch. (May/June 2016)



E	D	Q	$\overline{Q}$
0	0	latch	latch
0	1	latch	latch
1	0	0	1
1	1	1	0

10. Differentiate synchronous and asynchronous sequential circuits (May/June 2016)

Synchronous Circuits	Asynchronous Circuits
1. Simultaneous clock pulse is given to all the flip-flop.	1. Clock pulse is given to first flip-flop and the output of first flip-flop acts asa clock to the next and so on.
2. Fast as compared to asynchronous circuits.	2. Slow as compared to synchronous circuits because 2nd flip-flop has to wait until the 1st flip-flop gives the output.
3. Additional combinational circuit is required for its designing. This circuit becomes complex.	3. Circuit is simple as compared to synchronous circuits.

11. With reference to a JK flip-flop, what is racing? (Nov/Dec 2016)

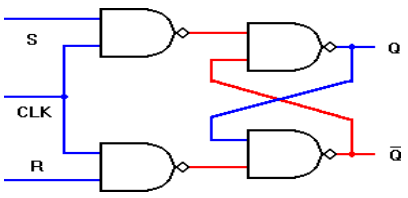
Because of the feedback connection in JK flip-flop, when both J & K are equal to 1 at the same time, output is complemented while activating the clock pulse. The output is complemented again and again if the pulse duration of the clock signal is greater than the signal propagation delay of the JK flip-flop for this particular input combination (J=K=1).

There is a race between 0 and 1 within a single clock pulse. This condition of the JK FF is called race-around condition or racing.

12. What is the edge - triggered flip - flop? (Nov / Dec 2015)

Output transitions occur at a leading edge or a trailing edge of the clock pulse

13. Draw the logic diagram of clocked SR flip-flop. Draw the truth table of RS flip flop. (Nov/Dec 2015, May/June 2014)



S	R	Output / Action

0	0	No Change
0	1	0 Reset
1	0	1 Set
1	1	Forbidder

14. Differentiate between sequential and combinational circuits (April/May 2015)

S.No.	Combinational Circuits	Sequential Circuits
1	Output depends only on the present values of the input.	Output depends on the present and past values of the input.
2	Feedback path is not used in combinational circuits.	Feedback path is used in Sequential circuits.
3	Memory element is not present.	Memory element is present.
4	Clock is not used in combinational circuits.	Clock is used in combinational circuits.
5	Circuit is simple.	Circuit is complex.
6	Example: Adders, Subtractors, code converters, comparator etc.	Example: Flip flops, counters, registers etc.

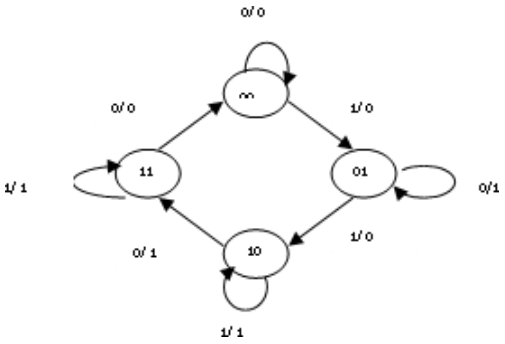
15. What is the minimum number of flip-flops needed to build a counter of modulus 60? (April/May 2015)

Modulus $N \leq 2^k$, where k is the number of flip-flops , Modulus $60 < 2^6 = 64$, k = 6. The minimum number of flip-flops needed to build a counter of modulus 60 is 6.

16. What is a state diagram? (May/June 2014).

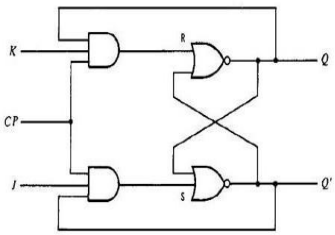
State diagram is the graphical representation of state table of sequential logic circuits. In the state diagram, a state is represented by a circle and the transition between states is indicated by directed lines connecting the circles. The directed lines are labeled with two binary numbers separated by a slash. The input value during the present state is labeled first and the number after the slash gives the output during the present state.

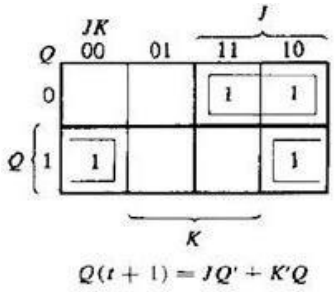
Example:



17. Realize JK flip flops (Nov/Dec 2014).

Logic Diagram: Characteristic Equation:





$Q(t+1) = JQ' + K'Q$

18. Give the excitation table of a J-K flip flop.

Q	Q(t+1)	J	K
0	0	0	X
0	1	1	X
1	0	X	1
1	1	X	0

19. Give the truth table for a J-K flip-flop.

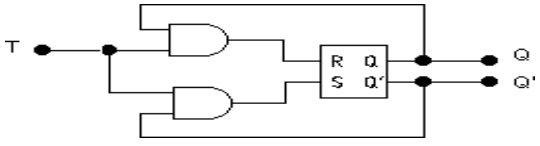
Q	J	K	Q(t+1)
0	0	0	0
0	0	1	0
0	1	0	1
0	1	1	1
1	0	0	1
1	0	1	0
1	1	0	1
1	1	1	0

20. Write the characteristic table of a D flip flop.

Q	D	Q(t+1)
0	0	0
0	1	1
1	0	0
1	1	1

21. Show the T flip-flop implementation from S-R flip-flop. (May/June 2013)

T Flip-Flop Implementation using SR Flip-Flop:



22. Give the truth table of a T flip flop.

Q	T	Q(t+1)
0	0	0
0	1	1
1	0	1
1	1	0

23. Why is D FF known as Delay FF?

The binary information present at the data input of the D FF is transferred to the Q output when the CP input is enabled. The output follows the data input as long as the pulse remains in its 1 state. When the pulse goes to 0, the binary information that was present at the data input at the time the pulse transition occurred is retained at the Q output until the pulse i/p is enabled again. So D FF is known as Delay FF.

24. When is a counter said to suffer from lockout?

In a counter, if the next state of some unused state is again an unused state and if by chance the counter happens to find itself in the unused states and never arrived at a used state then the counter is said to be in the lockout conditions.

25. What is a ripple counter?

Ripple counter is an asynchronous counter in which each flip-flop is triggered by output of the previous flip- flop.

26. What is a universal shift register?

A register may operate in any of the following five modes: SISO, SIPO, PIPO, PISO and bidirectional. If a register can be operated in all five possible modes, it is known as Universal Shift Register.

27. How race around condition can be eliminated?

Race around condition can be eliminated in a JK latch by two ways:

1. Using the edge triggered J-K flip-flop
2. Using the master slave J-K flip-flop

28. Mention the uses of shift registers.

(i) Storage Device: The primary use of shift register is temporary data storage.

(ii) Time delay generation: A SISO shift register can be used to introduce time delay T_D between the input and the output digital signals. The time delay can be given as $T_D = N \times (1/f_c)$, where N is the number of stages and f_c is the clock frequency. **(iii)**SIPO & PISO (iv) **Shift register counter:** A shift register with the serial output connected back to the serial input is called shift register counter. Because of such a connection, special specified sequences are produced as the output. The most common shift register counters are the ring counter and the Johnson counter.

29. The clock frequency is 2MHz. How long will it take to serial load the eight shift register?

(Given) $f_{CLK} = 2MHz$. $n = 8$

Time taken to load serially the eight bit will be given by

$$= n \times \frac{1}{f_{CLK}} = 8 \times \frac{1}{2 \times 10^6} = 4 \times 10^{-6} = 4\,\mu sec$$

30. What is a flip-flop?

Flip-flop : Flip-flop is a sequential circuit which is used to store single bit of information at a time i.e. either „1′ or „0′ at a time. It has two stable output states. It can stay in one of the two stable states unless state is changed by applying external inputs. Thus, it is a basic memory element for storage of data in binary form. There are various types of flip-flops:1. SR flip flop 2. JK flip-flop 3. D flip flop 4. T flip-flop

31. What do you meant by the term state reduction problem?

The reduction of the number of flip-flops in a sequential circuit is referred to as the state – reduction problem. State– reduction algorithms are concerned with procedures for reducing the number of states in a state table while keeping the external input – output requirements unchanged.

32. Differentiate between latch and flip-flop.

Latch	Flip-Flops
1. Latch has an enable input.	1. Flip-flops have a clock signal.
2. As long as enabled input is active, the latch output will keep changing according to the input.	2. Flip-flop samples its inputs and changes its outputs only at a particular instant of time i.e. when clock is provided.

33. Give expression for maximum frequency of operation of n-bit Asynchronous and synchronous counters.

Time period of clock (T_{clk}) ≥ N * $t_{pd,}$ where N = no. of FFs & t_{pd} = Propagation delay

Maximum frequency of operation for asynchronous counter is $f_{max} = \frac{1}{T_{clk}} = \frac{1}{N \times t_{pd}}$

Maximum frequency of operation of synchronous counter is

$$f_{max} = \frac{1}{N\ t_{pd}}$$

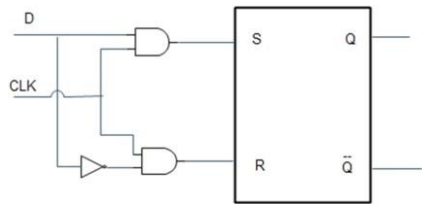
34. Write the characteristic table of JK Flipflop

Characteristic Table:

Q	J	K	Q(t+1)
0	0	0	0
0	0	1	0
0	1	0	1
0	1	1	1
1	0	0	1
1	0	1	0
1	1	0	1
1	1	1	0

35. Draw D-latch with truth table. (Nov/Dec 2016)

D Flip Flop Circuit



Characteristic Equation

D Flip Flop Characteristic Table

Input	Present State	Next State
D	**Q_t**	**Q_{t+1}**
0	0	0
0	1	0
1	0	1
1	1	1

36. Mention any two differences between the edge triggering and level triggering.

Level Triggering:

1) The input signal is sampled when the clock signal is either HIGH or LOW.
2) It is sensitive to Glitches.

Example: Latch.

Edge Triggering:

1) The input signal is sampled at the RISING EDGE or FALLING EDGE of the clock signal.
2) It is not-sensitive to Glitches.

Example: Flipflop.

37. Write the characteristic equation of a JK flip-flop.

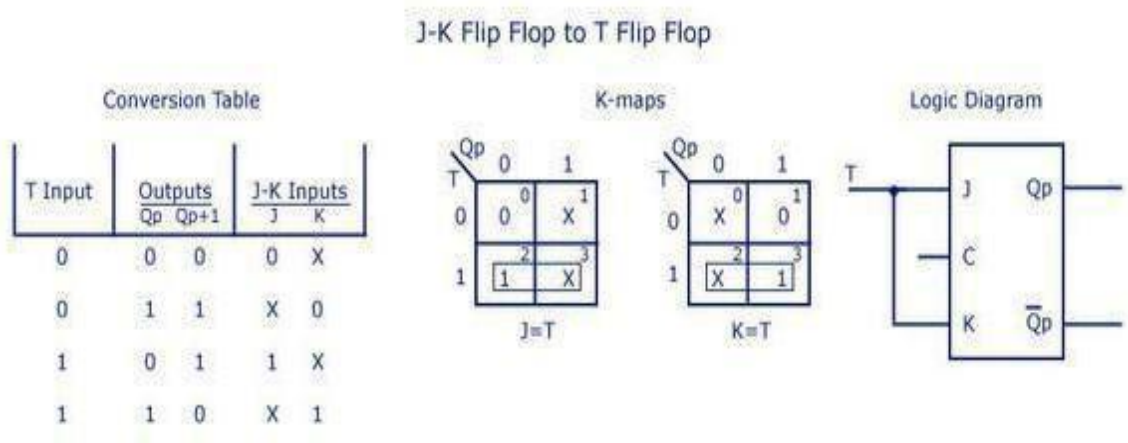
The characteristic equation of a JK flip-flop is given by

$$Q(next) = JQ' + K'Q$$

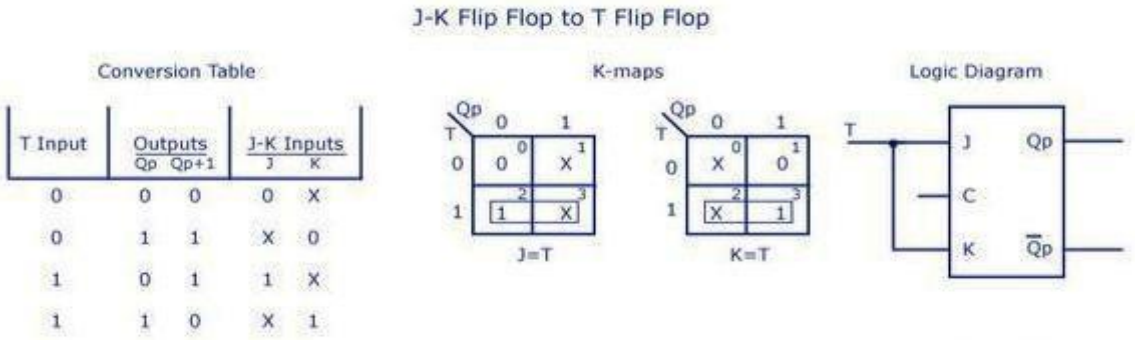
38. State the differences between Moore and mealy state machine.

S.No.	MOORE FSM	MEALY FSM
1.	Outputs of Moore FSM are a function of its present state.	Outputs of Moore FSM are a function of its present input and present state.
2.	Outputs change only at triggering clock edge.	Outputs change as soon as any of its input changes. However, states cannot change until triggering clock edge.
3.	Conceptually simpler but usually require more states.	Require fewer states than Moore FSM as output can have different values in a single state.
4.	Since, it has more circuit delays, more logic is needed to decode the output(s) and therefore it reacts slower to input(s) in comparison with Mealy FSM.	React faster to inputs.

39. Realise T-FF from JK-FF.



40. **Convert JK flip-flop to T flip-flop.**



41. **How many flip-flops are required to build a binary counter that counts from 0 to 1023?**

If the number of flip-flops required is n, then 2^n-1=1023 **n=10** since 2^{10}=1024

42. **Compare the logics of synchronous counter and ripple counter.**

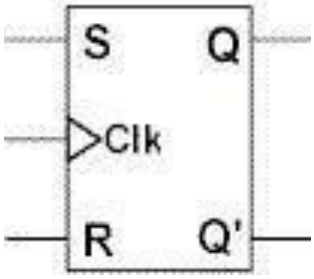
Asynchronous counter:

1. In this type of counter flipflop are connected in such a way that output of first flip-flop drives the clock for next flip-flop.
2. All the flip-flop are not clocked simultaneously.
3. Logic circuit is very simple even for more number of states.

Synchronous counter:

1. In this type there is no connection between output of first flip-flop and clock input of the next flip-flop.
2. All the flip-flop are clocked simultaneously.
3. Design involves complex logic circuit as number of states increases.

43. **Sketch the logic diagram of a clocked SR flip-flop.**



44. **How do you eliminate the race around condition in a JK flip-flop?**

- When the input to the JK flip-flop is j=1 and k=1, the race around condition occurs, i.e it occurs when the time period of the clock pulse is greater than the propagation delay of the flip flop.
- The output changes or toggles in a single clock period. If it toggles even number of times the output is same but if it toggles odd number of times then the output is complimented.

  To avoid race around condition we cant make the clock pulse smaller than the propagation delay so we use

  1. Master slave JK flip flop
  2. Positive or negative edge triggering

45. **Differentiate Flip-Flop from Latches**

Flip-flop	Latch
A flip-flop samples the inputs only at a clock event (rising edge, etc.)	A Latch samples the inputs continuously *whenever it is enabled*, that is, only when the enable signal is on. (or otherwise, it would be a wire, not a latch).
Flip-Flop are edge sensitive.	Latches are level sensitive.
Flipflop is sensitive to signal change and not on level. They can transfer data only at the single instant and data cannot be changed until next signal change.	Latch is sensitive to duration of pulse and can send or receive the data when the switch is on.
A flip-flop continuously checks its inputs and correspondingly changes its output only at times determined by clocking signal.	Latch is a device which continuously checks all its input and correspondingly changes its output, independent of the time determined by clocking signal.
It work's on the basis of clock pulses.	It is based on enable function input
It is a edge trigerred , it mean that the output and the next state input changes when there is a change in clock pulse whether it may a +ve or -ve clock pulse.	It is a level trigerred , it mean that the output of present state and input of the next state depends on the level that is binary input 1 or 0.

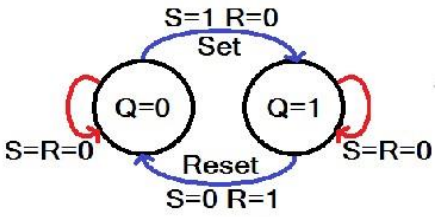
46. Draw the excitation table and state diagram for JK and SR Flip-Flop. [APRIL/MAY 2010. NOV/DEC 2011]

Excitation table: State diagram:

SR Flip Flop

("X" is "don't care")

States		Inputs	
Previous	Present	S	R
0	0	0	X
0	1	1	0
1	0	0	1
1	1	X	0

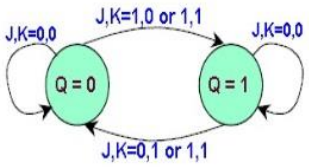


The characteristic equation of a SR flip-flop is $Q(\text{next}) = S + QR'$

JK Flip Flop

("X" is "don't care")

States		Inputs	
Previous	Present	J	K
0	0	0	X
0	1	1	X
1	0	X	1
1	1	X	0



The characteristic equation of a JK flip-flop is $Q(\text{next}) = JQ' + K'Q$

47. Draw the state table and excitation table of T flip-flop.

Q[t]	T	Q[T+1]	J	K
0	0	0	0	X
0	1	1	1	X
1	0	1	X	0
1	1	0	X	1

48. A 4-bit binary ripple counter is operated with clock frequency of 1KHz. What is the output frequency of its third Flip flop?

The output frequency of third flip-flop is: $½^3$ = **1/8KHz.**

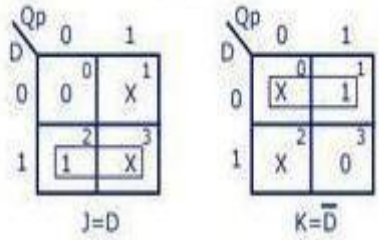
49. Realize JK flip-flop using D flip-flop.

J-K Flip Flop to D Flip Flop

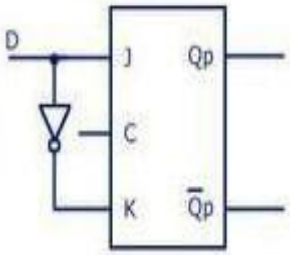
Conversion Table

D Input	Outputs Qp	Outputs Qp+1	J-K Inputs J	J-K Inputs K
0	0	0	0	X
0	1	0	X	1
1	0	1	1	X
1	1	0	X	0

K-maps



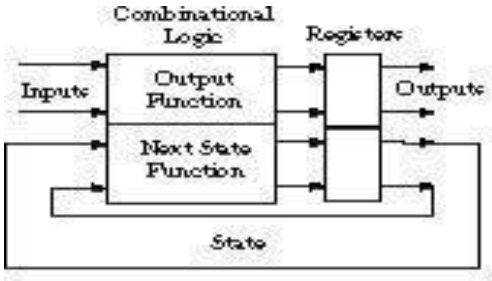
Logic Diagram

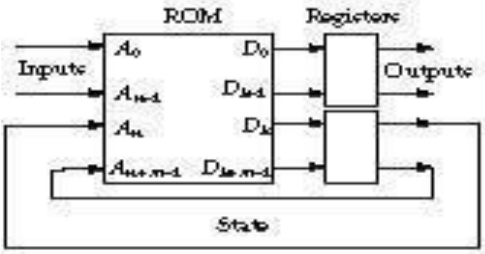


50. Define latches.

Latch is a simple memory element, which consists of a pair of logic gates with their inputs and outputs inter connected in a feedback arrangement, which permits a single bit to be stored.

51. Draw the block diagram for Moore model.





ROM implementation of a synchronous Mealy finite state machine.

PART B&C

1. Draw the neat diagram of a 4 – bit universal shift register and explain it's Operation. (Apr/May'19)

Refer"Digital Cicuits and Design " by S.Salivahanan &S.Arivazhagan 2nd Edition,Pg.No.359

2. A sequential circuit has two JK flip – flops A and B , two inputs x and y and one Output equation are: (Apr/May'19)

$J_A = Bx + B'_Y'$ $J_B = A'x$

$K_A = B'xy'$ $K_B = A + xy'$

Draw the logic diagram and state table of the circuit .Also derive the state Equations for A and B. (Apr/May'19)

Refer"Digital Cicuits and Design " by S.Salivahanan &S.Arivazhagan 2nd Edition,Pg.No.484

3(i) Explain the operation of JK flip-flop with neat diagram. (Nov/Dec 2018) (Nov/Dec 2015)

Refer"Digital Cicuits and Design " by S.Salivahanan &S.Arivazhagan 2nd Edition,Pg.No.267

(ii)Explain the operation of master slave flip flop and show, how the race around condition is eliminated. (Nov/Dec 2018) (Nov/Dec 2015)

Refer"Digital Cicuits and Design " by S.Salivahanan &S.Arivazhagan 2ndEdition,Pg.No.276

4. Explain the operation of synchronous MOD-6 counter. (Nov/Dec 2018)(Nov/Dec 2016)

Refer"Digital Cicuits and Design " by S.Salivahanan &S.Arivazhagan 2nd Edition,Pg.No.314

5. Design a synchronous sequence detector that produces an output 1, whenever the non overlapping sequence 1011 is detected. (Nov/Dec 2018)

Refer"Digital Cicuits and Design " by S.Salivahanan &S.Arivazhagan 2ndEdition,Pg.No.460

6. Draw a RS flip-flop circuit and explain its operation with truth table and suggest how to eliminate the undetermined stage? Write some RS Flip-flop applications.(Nov/Dec 2017)

Refer"Digital Cicuits and Design " by S.Salivahanan &S.Arivazhagan 2nd Edition,Pg.No.256

7.Design a 4 bit binary counter and explain its counting process. Discuss how to use this circuit to perform both up and down counting. (Nov/Dec 2017)

Refer"Digital Cicuits and Design " by S.Salivahanan &S.Arivazhagan 2nd Edition,Pg.No.288

8.Design a serial 2´s complement circuit with a shift register and a flip-flop. The binary number is shifted out from one side and its 2 ´ s complement shifted into other side of the shift register. (Nov/Dec 2017)

Refer"Digital Cicuits and Design " by S.Salivahanan &S.Arivazhagan 2nd Edition,Pg.No.284

9.Using SR flip flops design a parallel counter which counts in the sequence 000,111,101,110,001,010,000… (Apr/May 2017) 11.Design a 3-bit synchronous counter using D- Flip flop.

Refer"Digital Cicuits and Design " by S.Salivahanan &S.Arivazhagan 2ndEdition,Pg.No.313

10.(i)Draw and explain the 4-bit SISO,SIPO,PISO and PIPO shift register with its waveforms.

Refer"Digital Cicuits and Design " by S.Salivahanan &S.Arivazhagan 2nd Edition,Pg.No.346

(ii)Realize D flip- flop using SR flip-flop. (May/June '16)

Refer"Digital Cicuits and Design " by S.Salivahanan &S.Arivazhagan 2nd Edition,Pg.No.278

11.(i) Explain the operation of JK flip flop with neat diagram.

Refer"Digital Cicuits and Design " by S.Salivahanan &S.Arivazhagan 2nd Edition,Pg.No.267

(ii)Explain the operation of serial –in –serial- out shift register.

Refer"Digital Cicuits and Design " by S.Salivahanan &S.Arivazhagan 2nd Edition,Pg.No.347

12. Design a synchronous up/down counter. (Nov/Dec ´ 16)

Refer"Digital Cicuits and Design " by S.Salivahanan &S.Arivazhagan 2nd Edition,Pg.No.304

13.Using D flip flops design a synchronous counter which counts in the sequence. 000,001,010, 011,100,101,110,111,000. (April/May 2015)

Refer"Digital Cicuits and Design " by S.Salivahanan &S.Arivazhagan 2nd Edition,Pg.No.315

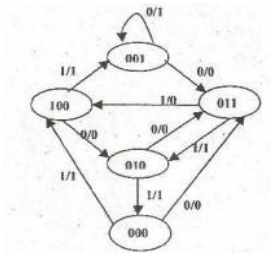
14.Explain the operation of synchronous counter. (Nov/Dec 2015)

Refer"Digital Cicuits and Design " by S.Salivahanan &S.Arivazhagan 2nd Edition,Pg.No.311

15. Design a Moore type sequence detector to detect a serial input sequence of 101.(May/June 2014)

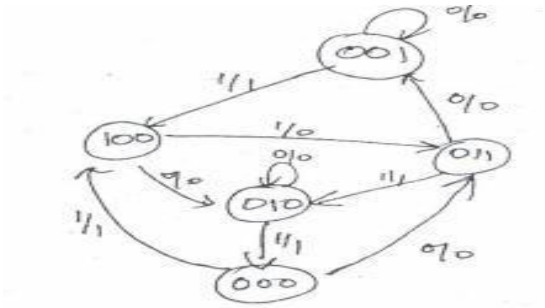
Refer"Digital Cicuits and Design " by S.Salivahanan &S.Arivazhagan 2nd Edition,Pg.No.460

16. Design the sequential circuit specified by the following state diagram using T flip-flops. Check whether your design is self-correctable. (Nov/Dec 2014).



Refer Notes

17.Design a sequential circuit that has 3 flip-flops A, B and C, one input 'x ´ and one output 'y ´ . The circuit is to be designed by treating the unused states as don ´ t care conditions. Use JK flip-flops in the design. State diagram is given below. (May/June 2014)



Refer Notes

18 (i) Realize a JK flip flop using SR flip flop.

Refer"Digital Cicuits and Design " by S.Salivahanan &S.Arivazhagan 2nd Edition,Pg.No.279

(ii) Draw the logic diagram for SR, JK, D&T flip flops.

Refer"Digital Cicuits and Design " by S.Salivahanan &S.Arivazhagan 2nd Edition,Pg.No.256,263,269&264

19 (i) Design and explain the working of a asynchronous Decade counter.

Refer"Digital Cicuits and Design " by S.Salivahanan &S.Arivazhagan 2nd Edition,Pg.No.301

(ii) Design and explain the working of a 4 bit synchronous binary counter and draw its timing diagram.

Refer"Digital Cicuits and Design " by S.Salivahanan &S.Arivazhagan 2nd Edition,Pg.No.288

UNIT – IV ASYNCHRONOUS SEQUENTIAL CIRCUITS

1. Define a 'flow table".(Apr/May'19)

In the design of asynchronous sequential circuits,it is more convenient to name the states by letter symbols without making specific reference to their binary values.Such a table is called flowtable.

2. Distinguish between non-critical face and critical race.(Apr/May'19)

A **non-critical race** condition occurs when the sequence in which internal variables' changes do not have any impact on the final state of the machine. **Race** conditions are notorious for being difficult to troubleshoot, as reproduction depends on the relative timing **between the different** elements.

3.What is critical race condition in asynchronous sequential circuits? Give an example (Nov/Dec 2014). (May/June 2016) (Nov/Dec 2016) (Nov/Dec 2018)

Critical race in asynchronous circuits occur between two signals that are required to change at the same time when the next stable state is dependent on the delay paths in the circuit. If it is possible to end up in two or more different stable states, depending on the order in which the state variable change, then it is called a critical race.

4.Draw the general model of ASM. (Nov/Dec 2015), (Nov/Dec 2018)

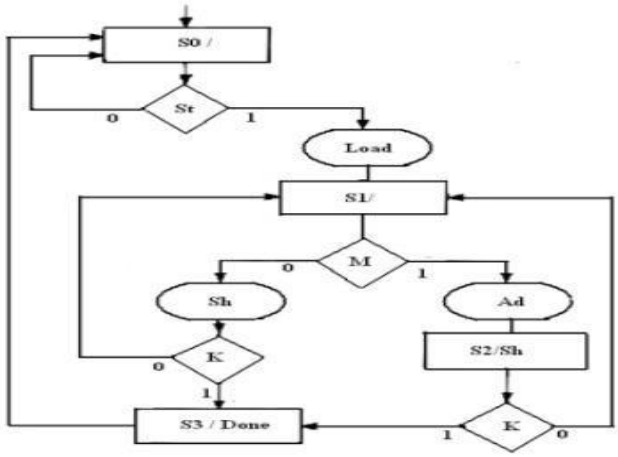


Figure: ASM chart

5. What is the significance of state assignment? (April/May 2017)

In synchronous circuits, state assignments are made with the objective of circuit reduction. In Asynchronous circuits, state assignments are made to avoid critical races.

6. What are the steps for the analysis of asynchronous sequential circuit? (April/May 2017)

- Reduce the flow table by merging rows in the primitive flow table.
- Assign binary states variables to each row of the reduced flow table to obtain the transition table.
- Assign output values to the dashes associated with the unstable states to obtain the output maps.
- Simplify the Boolean functions of the excitation and output variables and draw the logic diagram.

7.Define critical race and give methods for critical race Free State assignment.(May/June 2016)

A race condition is said to exist in asynchronous sequential circuit when two or more binary state variables change value in response to change in an input variable. When unequal delays are encountered, a race condition may cause the state variables to change in an unpredictable manner. If it ispossible to end with more than one state depending on the order of the state change, then it is a critical race. A critical race must be avoided. The technique commonly used for making a critical race-free network is state assignment. State assignments are classified as follows: Shared state assignment,Multiple row state assignment, One hot state assignment.

8.What do you meant by the term Hazard? Define Static -1 Hazard. (Nov/Dec 2015) (May/June ´ 16) (Nov/Dec ´ 16),(Nov/Dec 2017)

Hazards are unwanted switching transients that may appear at the output of a circuit because different paths exhibit different propagation delays. Hazards occur in combinational circuits, where they may cause a temporary false output value. When this condition occurs in asynchronous sequential circuits, it may result in a transition to a wrong stable state. Steps must be taken to eliminate this effect. **Static 1-hazard:** The output may momentarily go to 0 when it should remain 1.

9.Differentiate Static & Dynamic Hazard. (Nov/Dec 2012)(May/June 2016)

(Nov/Dec 2016)

Static 1-hazard: The output may momentarily go to 0 when it should remain 1.

Static 0-hazard: The output may momentarily go to 1 when it should remain 0.

Dynamic hazard causes the output to change three or more times when it should change from 1 to 0 or from 0 to 1.

10.Explain non- critical race. (Nov/Dec 2016)

The order by which the state variables change may not be known in advance. If the final stable state that the circuit reaches does not depend on the order in which the state variable change, the race is called a non-critical race.

11.What is State Assignment? (Or) What is the most important consideration in making state assignments for asynchronous network? (April/May 2015)

State assignment is assigning binary value to each state. It is represented by a letter symbol in the flow table of sequential circuit. The primary objective in choosing a proper binary state assignment in asynchronous circuit is the prevention of critical races

12.Define ASM chart. List its three basic elements. (Nov/Dec 2014)

The **algorithmic state machine (ASM)** method is a method for designing finite state machines. It is used to represent diagrams of digital integrated circuits. The ASM diagram is like a state diagram but less formal and thus easier to understand. An ASM chart is a method of describing the sequential operations of a digital system. Three basic elements are 1.State box 2.Decision box and 3.Conditional output box.

13. Explain the fundamental mode of operation.

Asynchronous sequential circuits must be allowed to attain a stable state before the input is changed to a new value. Because of delays in the wires & the gate circuits, it is impossible to have two or more input variables change at exactly the same instant of time without an uncertainty as to which one changes first. Therefore, simultaneous changes of two or more variables are usually prohibited. This restriction means that only one input variable can change at any one time & the time between two input changes must be longer than the time it takes the circuit to reach a stable state. This type of operation is defined as fundamental mode.

14. What is asynchronous sequential circuit?

Asynchronous sequential circuit is a system which depends upon the order in which its input signals change and can be affected at any instant of time. The memory elements used are time delay devices.

15. What is the difference between synchronous and asynchronous sequential circuits?

S.No	Synchronous sequential circuits	Asynchronous sequential circuits
1	The change of internal state occurs in response to a clock pulse.	The change in internal state occurs whenever there is a change in input variable.
2	Memory elements are clocked flip-flops	Memory elements are unclocked flip-flops or Time delay units.
3	The present state is totally specified by FF values and does not change if input changes while clock pulse is inactive	There is no clock pulse. Because of absence of clock, asynchronous circuits are faster than synchronous circuits.
4	Design is easy.	Design is more difficult because of the timing problems involved in the feedback path.

16. Distinguish between fundamental mode circuits and pulse-mode circuits.

Fundamental Mode Circuit

The input variables change only when the circuit is stable; only one input variable can change at a given time; Inputs are levels and not pulses.

Pulse mode circuit

The input variables are pulses instead of levels; the width of the pulses is long enough for the circuit to respond to the input; the pulse width must not be so long that it is still present after the new state is reached and cause a faulty change of state; No two pulses should arrive at the input lines simultaneously.

17. Why is the pulse mode operation of asynchronous sequential circuits not very popular?

Because of the input variable pulse width restrictions, pulse mode circuits are difficult to design.

For this reason the pulse mode operation of asynchronous sequential circuits is not very popular.

18. Define Flow table.

During the design of asynchronous sequential circuits, it is more convenient to name the states by letter symbols without making specific reference to their binary values, such a table is called a Flow table.

19. What do you understand by Race condition?

A race condition is said to exist in an asynchronous sequential circuit when two or more binary state variables change value in response to a change in an input variable. When unequal delays are encountered, a race condition may cause the state variables to change in an un predictable manner.

20. Define the term Maximal compatible.

The maximal compatible is a group of compatibles that contains all the possible combinations of compatible states. The maximal compatible can be obtained from a merger diagram

21. Define closed covering.

The condition that must be satisfied for row merging is that the set of chosen compatibles must cover all the states that must be closed. The set will cover all the states if it includes all the states of the original state table. The closure condition is satisfied if there are no implied states or if the implied states are included within the set. A closed set of compatibles that covers all the states is called a closed covering.

22. Explain Shared Row method.

The method of making race free assignment by adding extra rows in the flow table is sometimes referred to as Shared Row method.

23. Define Merger diagram.

The merger diagram is a graph in which each state is represented by a dot placed along the circumference of a circle. Lines are drawn between any two corresponding dots that form a compatible pair. All possible compatibles can be obtained from the merger diagram by observing thegeometry.

24. Define Essential Hazard. What is the reason for essential hazard to occur?

An essential Hazard is caused by unequal delays along two or more paths that originate from the same input. An excessive delay through an inverter circuit in comparison to the added redundant gates as in static hazards. To avoid essential hazard, each feedback loop must be handled with individual care to ensure that the delay in the feedback path is long enough compared to delays of other signals that originate from the input terminals.

25. Explain the use of SR latches in asynchronous sequential circuits.

The use of SR latches in asynchronous circuits produce a more orderly pattern, which may result in a reduction of the circuit complexity. An added advantage is that the circuit resembles the synchronous circuit in having distinct memory elements that store & specify the internal states. One of the ways to avoid static hazards in asynchronous sequential circuits is to implement the circuit with SR latches.

26. Define Primitive Flow table.

A primitive flow table is a flow table with only one stable total state in each row.

27. What is finite state Machine?

A finite state machine (or finite automation) is an abstract model describing the synchronous sequential machine and its spatial counterpart, the iterative network.

28. What is the need of state reduction in sequential circuit design?

To reduce the number of flip-flops and to reduce number of gates in the combinational circuit that drives the flip-flop inputs.

29. Define compatible states.

Two states are compatible (equivalent) if in every column of the corresponding rows in the flow table, there are identical or equivalent next states and there is no conflict in the output values.

30. What is One-Hot assignment?

One hot state assignment is made so that only one variable is active or “hot” for each row in the original flow table. This technique requires as many state variables, as there are rows in a flow table. Additional rows are introduced to provide single variable changes between internal state transitions.

31. Define cycle.

A cycle occurs when an asynchronous machine makes a transition through a series of unstable states. Care must be taken to make sure whether the cycle terminated with a stable state or not. If a cycle does not terminate with a stable state, the circuit will keep going from one unstable state to another, making the entire circuit unstable.

32. What are hazard free digital circuits?

A circuit which has no hazard like static-0-hazard and static-1-hazard is called hazard free digital circuit.

33. What are the two types of asynchronous sequential circuits?

- □ Fundamental mode circuit
- □ Pulse mode circuit

34. What is state table?

The state table representation of a sequential circuit consists of three sections labelled present state, next state and output. The present state designates the state of flip-flops before the occurrence of a clock pulse. The next state shows the states of flip-flops after the clock pulse, and the output section lists the value of the output variables during the present state.

35. What are Hazards?

The unwanted switching transients (glitches) that may appear at the output of acircuit are called Hazards.

36. What is a state diagram? Give an example.

A state diagram is a type of diagram used in computer science and related fields to describe the behaviour of systems. State diagrams require that the system described is composed of a finite number of states; sometimes, this is indeed the case, while at other times this is a reasonable abstraction. Many forms of state diagrams exist, which differ slightly and have different semantics.

37. Under what circumstances asynchronous circuits are prepared.

(i) Fundamental mode asynchronous circuits
(ii) Pulse mode asynchronous circuit

38. Differentiate fundamental mode and pulse mode asynchronous sequential circuits.

	Fundamental mode sequential circuits	**Pulse mode sequential circuits.**
1	Memory elements are clocked flip-flops	Memoryelementsareeitherunlockedflip - flops or time delay elements.
2	Easier to design	More difficult to design

PART B&C

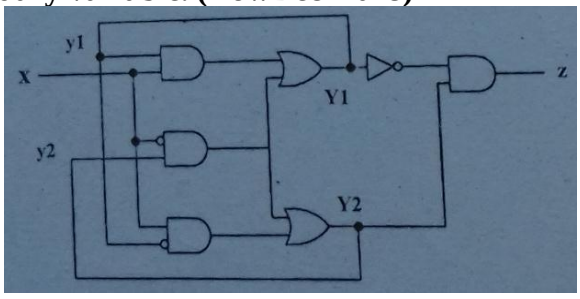
1. An asynchronous sequential circuit is described by the excitation function, $Y=x_1x_2'+(x_1+x2')y$ and the output function z= y .Draw the logic diagram of the circuit . Derive the transition table and output map. Also discuss about the behavior of the circuit. (Apr/May'19)

Refer"Digital Cicuits and Design " by S.Salivahanan &S.Arivazhagan 2nd Edition,Pg.No.484

2. Briefly explain about race –free state assignment with relevant examples. (Apr/May'19)

Refer "Digital Design " by Morris Mano,4th Edition Pg.No:464

3 (i) Write logical equations and construct transition table for the circuit output in terms of the circuit inputs and secondary variable. (Nov/Dec 2018)



Refer"Digital Cicuits and Design " by S.Salivahanan &S.Arivazhagan 2ndEdition,Pg.No.484

(ii) Explain Race-Free state Assignment in detail, with an example. (Nov/Dec 2018)

Refer"Digital Cicuits and Design " by S.Salivahanan &S.Arivazhagan 2nd Edition,Pg.No.464

4. (i) Draw timing diagram and explain the types of hazard in detail. (Nov/Dec 2018)

Refer"Digital Cicuits and Design " by S.Salivahanan &S.Arivazhagan 2nd Edition,Pg.No.507

(ii) Explain pulse mode sequential circuit in detail. (Nov/Dec 2018)

Refer"Digital Cicuits and Design " by S.Salivahanan &S.Arivazhagan 2nd Edition,Pg.No.484

5. Illustrate the design procedure of algorithmic state machine with neat flow chart. (Nov/Dec 2017

Refer "Digital Design " by Morris Mano,4th Edition Pg.No:375

6. Discuss the design steps of asynchronous sequential circuits. (Nov/Dec 2017)

Refer"Digital Cicuits and Design " by S.Salivahanan &S.Arivazhagan 2nd Edition,Pg.No.480

7(i).Summarize the design procedure for a synchronous sequential circuit.

Refer"Digital Cicuits and Design " by S.Salivahanan &S.Arivazhagan 2nd Edition,Pg.No.456

(ii).Derive the state table of a serial binary adder. (April/May17)

Refer"Digital Cicuits and Design " by S.Salivahanan &S.Arivazhagan 2nd Edition,Pg.No.175

8. What is the objective of state assignment in an asynchronous sequential circuit? Give the Hazard free realization for the Boolean function f(A,B,C,D)=M(0,2,6,7,8,10,12). (April/May ´ 17)

Refer"Digital Cicuits and Design " by S.Salivahanan &S.Arivazhagan 2nd Edition,Pg.No.509

9. A sequential machine has one input line where 0 ´ s and 1 ´ s are being incident. The machine has to produce a output of '1 ´ only when exactly two '0 ´ s followed by a ´ 1 ´ or exactly two '1 ´ s followed by a ´ 0 ´ .Using any state assignment and JK flip flop, synthesize the machine. (April/May ´ 17)

Refer"Digital Cicuits and Design " by S.Salivahanan &S.Arivazhagan 2nd Edition,Pg.No.175

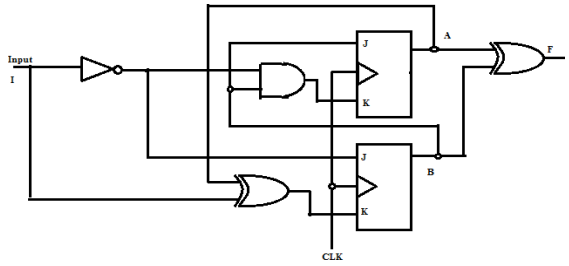
10. Design an asynchronous circuit that will output only the second pulse received and ignore any other pulse. (Nov/Dec '16)

Refer"Digital Cicuits and Design " by S.Salivahanan &S.Arivazhagan 2nd Edition,Pg.No.498

11.Design an asynchronous sequential circuit with two inputs X1 and X2 and with one output Z. When X1 is 0 the output Z is 0.The first change in X2 that occurs while x1 is 1 will cause output Z to be 1.The output Z will remain 1 until X1 returns to 0. (May/June '16)

Refer"Digital Cicuits and Design " by S.Salivahanan &S.Arivazhagan 2nd Edition,Pg.No.488

12.Construct the transition table , state table and state diagram for the Moore sequential circuit given below. (May/June '16)



Refer"Digital Cicuits and Design " by S.Salivahanan &S.Arivazhagan 2nd Edition,Pg.No.474

13. Design an asynchronous sequential circuit with 2 inputs T and C. The output attains a value of T = 1 and C moves from 1 to 0. Otherwise the output is 0. (Nov/Dec 2015)

Refer"Digital Cicuits and Design " by S.Salivahanan &S.Arivazhagan 2nd Edition,Pg.No.491

14. Design an asynchronous sequential circuit with inputs A and B and an output Y. Initially and at any time if both the inputs are 0, the output, Y is equal to 0. When A or B becomes 1 and Y becomes 1. And other input also becomes 1, Y becomes 0.The output stays at 0 until circuit goes back to initial state. (Nov/Dec 2014).

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15. Design a T flip-flop using logic gates. Derive the state table, state diagram, and primitive flow table and transition table and merger graph. Draw the logic circuit. (May/June 2014)

Refer"Digital Cicuits and Design " by S.Salivahanan &S.Arivazhagan 2nd Edition,Pg.No.476

16. Design a asynchronous sequential circuit that has 2 inputs x1 and x2 and one output z. When x1=0, output is 0.The change in x2 that occurs while x1 is 1 will cause output z=1. The output z will remain 1 until x1 returns to 0. (May/June 2014)

Refer"Digital Cicuits and Design " by S.Salivahanan &S.Arivazhagan 2nd Edition,Pg.No.480

17. A sequential circuit has two JK flip flops A and B. The flip flop input functions are Ja=B+X Ka=1 Jb=A ´ +X ´ , Kb=1 and output equation Y=XA ´ B,

(a) Draw the logic diagram of the circuit.

(b)Tabulate the state table.

(c)Draw the state diagram. (Nov/Dec 2012)

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UNIT – V MEMORY DEVICES AND DIGITAL INTEGRATED CIRCUITS

1. A standard TTL gate has the following current specifications
I_{OH}=400 µA,I_{IH}=40µA,I_{OL}=16 mA,I_{IL}=1.6mA.Calculate fanout.(Apr/May'19)
Solution:
a)Fanout(HIGH)= I_{OH}/ I_{IH}=400µA/40 µA
Fanout(HIGH)=10 µA
b)Fanout(LOW)= I_{OL}/ I_{IL}=**16 mA /1.6mA**
Fanout(LOW)=10 mA

2.A DRAM ship uses two dimensional address multiplexing. It has 13 common address pins with the row address having one bit more than the column address. What is the capacity of the memory? (Apr/May'19)

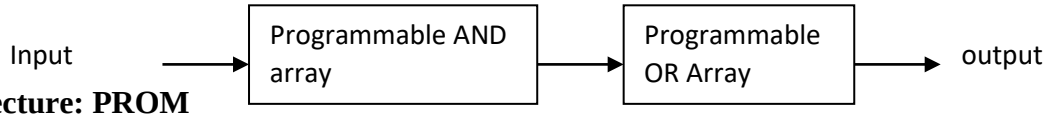
Solution:
13+12 = 25 Address lines, => Memory Capacity = 225 words

3. Interpret Read and Write operation. (Nov/Dec 2018)

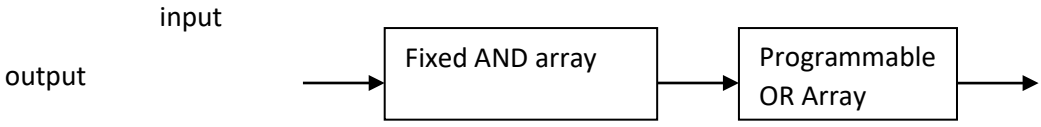
Write operation: puts data into a specified address in the memory. Read operation: takes data out of a specified address in the memory

4. How does the architecture of a PLA differ from a PROM? (or) What is programmable logic array? How it differs from ROM? (Nov / Dec 2015) (Nov/Dec 2016) (Nov/Dec 2018)

The programmable logic array (PLA) is a programmable logic device with a programmable ORarray and a programmable AND array. The Programmable Read Only Memory (PROM) is a programmable logic device with a fixed AND array and a programmable OR array. Architecture: PAL



Architecture: PROM



5. How does ROM retain information? (April/May 2017)

ROM chips contain a grid of columns and rows. ROM uses a diode to connect the lines if the value is 1. If the value is 0, then the lines are not connected at all. A diode normally allows current to flow in only one direction and has a certain threshold, known as the forward break over, that determines how much current is required before the diode will pass it on. A ROM chip can send a charge that is above the forward break over down the appropriate column with the selected row grounded to connectat a specific cell. If a diode is present at that cell, the charge will be conducted through to the ground, and, under the binary system, the cell will be read as being "on" (a value of 1).

6. Differentiate between PAL and PLA? (April/May 2017)

PLA	PAL
In case of PLA i.e. programmable logic array both AND and OR arrays are programmable.	In case of PLA i.e. programmable array logic AND array are programmable and OR arrays are fixed.
It is costlier as compared to PAL.	It is cheaper.
It is complex than PAL.	It is simple.
It can't easily be programmed.	It is easy to program a PAL

7. Give the classification of Programmable logic devices. (May/June 2016) or Write the types

of Programmable logic devices (Nov/Dec 2017)

Programmable logic array (PLA),Programmable array logic (PAL),Generic array logic (GALS),Complex programmable logic device (CPLD),Field-programmable gate array (FPGA)

8. Compare and contrast EEPROM and flash memory (Nov/Dec2014) (Nov/Dec 2016).

Flash and EEPROM are very similar, but there is a subtle difference. Flash and EEPROM both use quantum cells to trap electrons. Each cell represents one bit of data. The presence or absence of electrons in a cell indicates whether the bit is a 1 or 0. The cells have a finite life - every time a cell is erased, it wears out a little bit. In EEPROM, cells are erased one-by-one. The only cells erased are those which are 1 but need to be zero. But Flash can erase an entire block of data. Flash memory can only write to an entire chunk, or "sector", of memory at a time.

9. How many data inputs, data outputs and address inputs are needed for a 1024 × 4 ROM? (Or) What is the memory capacity of Random Access memory if it has 10 address lines? (Nov/Dec 2017)

No. of data inputs and outputs = 4, $1024 = 2^{10}$, No of address inputs = 10

10. How the bipolar RAM cell is different from MOSFET RAM cell. (May/June 2016)

1.MOS have less leakage current than BJT. So power consumption is less. 2.MOS transistor has smaller size than BJT. So it gives high packing density. 3.MOS fabrication has less number of fabrication steps than BJT. Also fabrication of MOS is much simpler than BJT.

11. Define noise margin. What is its importance? (MAY/JUNE 2016)

Noise margin is also known as noise immunity. It is defined as the ability of a logic circuit to tolerate noise without causing any unwanted changes in the output. Also, the quantitative measure of noise immunity is known as noise margin. It is important because it cause the voltage to drop into the invalid range so as to avoid the effects of noise voltage.

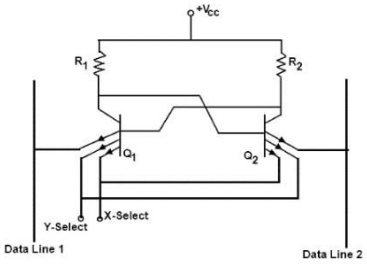
12. Why totem pole outputs cannot be connected together? (Nov/Dec 2016)

Two outputs cannot be tied together in totem – pole i.e. it does not support wired logic. If the gate of transistor A is high and the output of gate of transistor B is low, the low load resistance offered draws high current. This current might not damage the transistors immediately but over a period of time can cause overheating and deterioration in performance and eventual device failure.

13. Compare a static and dynamic RAM cell. (April/May 2015)

Static RAM: No refreshing, 6 to 8 MOS transistors are required to form one memory cell, Information stored as voltage level in a flip flop.
Dynamic RAM: Refreshed periodically, 3 to 4 transistors are required to form one memory cell; Information is stored as a charge in the gate to substrate capacitance.

14. Draw the structure of a Static RAM cell. (May/June 2014)



15. What is Field Programmable Gate Array device (FPGA) device (Nov/Dec 2014).

A **field-programmable gate array** (**FPGA**) is an integrated circuit designed to be configured by a customer or a designer after manufacturing – hence "field-programmable". The FPGA configuration is generally specified using a hardware description language (HDL), similar to that used for an application-specific integrated circuit (ASIC).FPGAs contain an array of programmable logic blocks, and a hierarchy of reconfigurable interconnects that allow the blocks to be "wired together" – , like many logic gates that can be inter-wired in different configurations. Logic blocks can be configured to perform complex combinational functions, or merely simple logic gates like AND and XOR. In most FPGAs, logic blocks

also include memory elements, which may be simple flip-flops or more complete blocks of memory.

16. Describe the basic functions of ROM and RAM. (or) What is the basic difference between RAM and ROM circuitry. (April / May 2015)

ROM: Read only memory is used to store information permanently. The information cannot be altered. *RAM:* Random Access Memory is used to store information. The information can be read form it and the new information can be written into the memory.

17. What is volatile and non-volatile memory?

The memory which cannot hold the data when power is turned off is known as volatile memory.

The memory which can hold the data when power is turned off is known as non-volatile memory

18. What is a PLA? Describe its uses.

PLA (Programmable Logic Array) is a programmable logic device with a Programmable AND array and a programmable OR array.PLA can be used to implement complex logic circuits. It is more economical to use PLA rather than PROM to implement logic circuits that have more number of don ´ t care conditions in order to reduce number of gates. PLA is flexible compared to PROM & PAL.

19. Distinguish between EPROM and EEPROM

S.No	EPROM	EEPROM
1	Erasable Programmable Read Only Memory	Electrically Erasable Programmable Read Only Memory
2	Placing the EPROM chip under a special ultraviolet erases the stored information.	Applying electrical signal erases the stored information.
3	It can also be called as UV EPROM	It can also be called as Electrically Alterable ROM (EAROM).

20. What are the major drawbacks of the EEPROM?

COST: In EEPROM, the erasing and programming of an EEPROM can be done in circuit. (Without using separate UV light source and special PROM programmer unit). Because of this on- chip support circuitry the EEPROM is available with more cost.

DENSITY: The high level integration of the EEPROM occupies more space. For example, 1-Mbit EEPROM requires about twice as much silicon as a 1-Mbit EPROM.

21. Define Bit time & Word time.

The time interval between clock pulses is called the bit time, and the time required to shift the entire contents of a shift register is called the word time.

22. What does burning a ROM mean?

The process of entering data into the ROM by burning internal fuses is called programming or burning a ROM.

23. How long will it take to erase UV erasable EPROM completely?

15 to 20 min.

24. What is an EAROM?

EAROM: Erasable Alterable Read Only Memory. The stored information is erased by applying electrical signal.

25. What is Configurable Logic Block?

The programmable logic blocks in the Xilinx family of FPGAs are called configurable logic blocks

(CLBs). The CLB of Xilinx 3000 series can be configured to perform any logic function of up to a maximum of seven variables.

26. Give the different types of RAM.

RAM can be classified into two types:

Static RAM: The storage elements used in this type RAM are latches (unclocked FFs).

Dynamic RAM: A dynamic RAM is one in which data are stored on capacitors which require periodic recharging (refreshing) to retain the data. RAMs are manufactured with either bipolar or MOS technologies. Bipo

27. What is Memory refresh?

Dynamic RAMs are fabricated using MOS technology. These store 1s and 0s as charges on a small MOS capacitor (typically a few Pico farads). Because if the tendency for these charges to leak of after a period of time, dynamics require periodic recharging of the memory cells This is called refreshing the dynamic RAM or memory refresh.

28. Distinguish between Bipolar RAM cell and MOSFET RAM cell.

Bipolar RAM cell is a latch which is manufactured with bipolar technology (using BJT). They are all static RAMs. MOSFET RAM cell a storage element which is manufactured with MOS technology (MOSFET). Capacitors are provided by metal oxide semiconductor (MOS).

29. What do you mean by PLD´s? (Or) List the advantages of PLDs (May/June 2014)

PLDs: Programmable logic devices are the special type of IC ´ s and are programmed before use. Different type of logic functions can be implemented using a single programmable IC chip of PLD ´ s. PLD s can be reprogrammed because these are based on re-writable memory technologies.

30. On what basis do we characterize various types of memories?

Memories can be characterized on various parameters.

1. Characterize based on Principle of operation. 2. Characterize based on Physical characteristics. 3. Characterize based on Mode of Access 4. Characterize based on Fabrication Technology.

31. What are the characteristics of memories?

Memory organization and capacity, Physical dimensions, Packing of memory, Power consumption, Cost etc

32. How does the architecture of a PAL differ from a PROM.?

Programmable Array Logic (PAL) is a programmable logic device with a fixed OR array and a programmable AND array. Because only the AND gates are programmable, the PAL is easier to program, is not flexible as the PLA. It uses array logic symbol. The Programmable Read Only Memory (PROM) is a programmable logic device with a fixed AND array and a programmable OR array.

33. What is meant by memory Expansion? Mention its limit.

The memory expansion can be achieved in two ways: by expanding word size and expanding memory capacity.

Limitations:

1. Memory capacity upto 16Mbytes.
2. 24 address lines and 16 data lines.

34. What are the advantages of static RAM and Dynamic Ram?

Static RAM:

- □ Access time is less.
- □ Fast operation.

Dynamic Ram

- □ It consumes less power.

- Cost is low.

35. Implement the exclusive or function using ROM.

- Can implement multi-input/multi-output logic functions inside of ROM.
- Data outputs are the logic functions and the address lines are the logic function inputs.
- We create a ROM Table to store the logic functions.
- When an input (or address) is presented, the value stored in the specified memory location appears at the data outputs.
- Each data output represents the correct value for its logic function

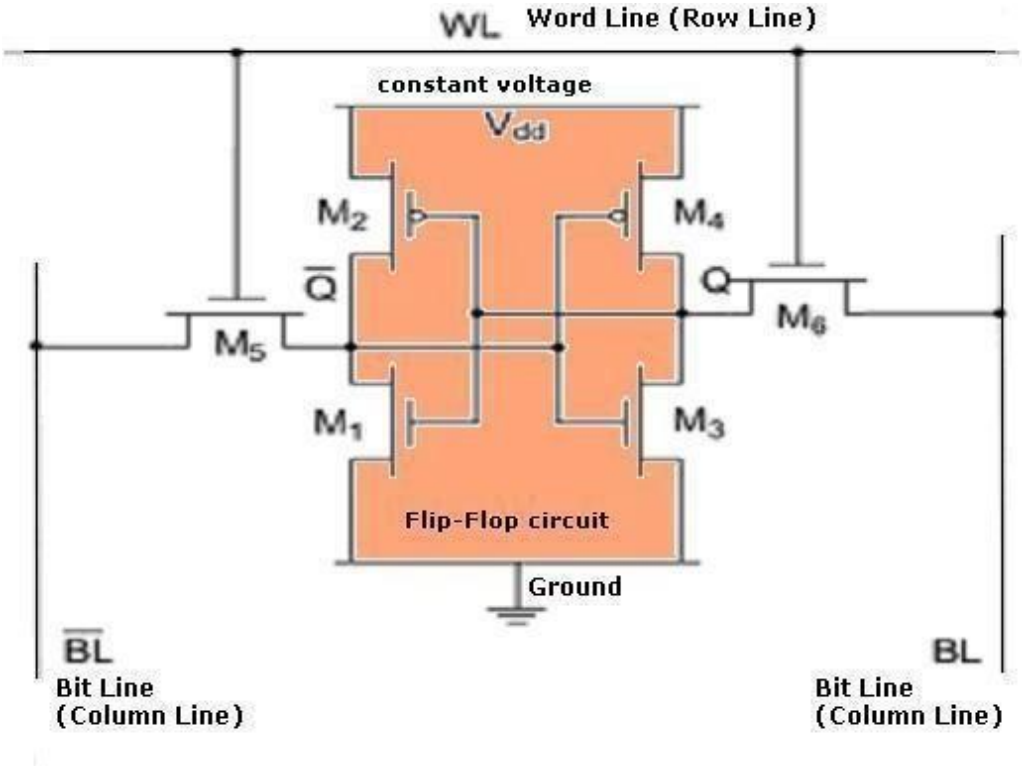
36. Mention few applications of PLA and PAL.

- Implement combinational circuits
- Implement sequential circuits
- Code converters
- Microprocessor based systems

37. What are the different types of programmable logic devices?

PROM,PLA,PAL,FPGA

38. Draw the structure of a static RAM cell.



39. List the advantages of PLDs.

Low and fixed (two gate) propagation delays (typically down to 5 ns),simple,low-cost (free),Design tools.

40. What is PAL?

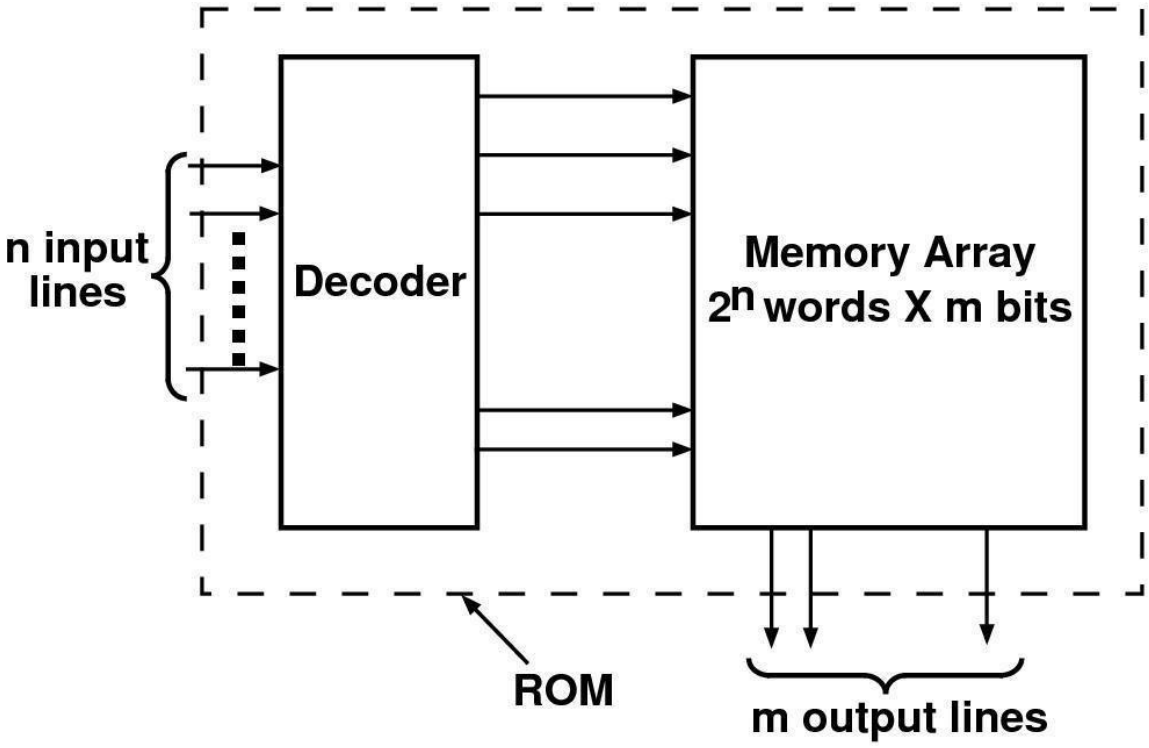
PAL is programmable array logic, PAL consists of a programmable AND array and a fixed OR array with output logic.

41. What is access time and cycle time of a memory?

Access time is the maximum specified time within which a valid new data is put on the data bus after an address is applied.

Cycle time is the minimum time for which an address must be held stable on the address bus in read cycle**.**

42. Implement a 2-bit multiplier using ROM. [Nov/Dec-2010]

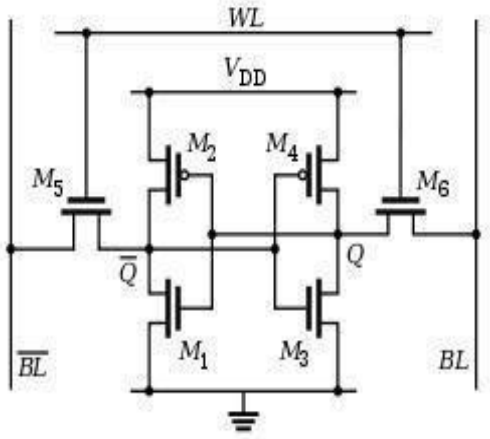


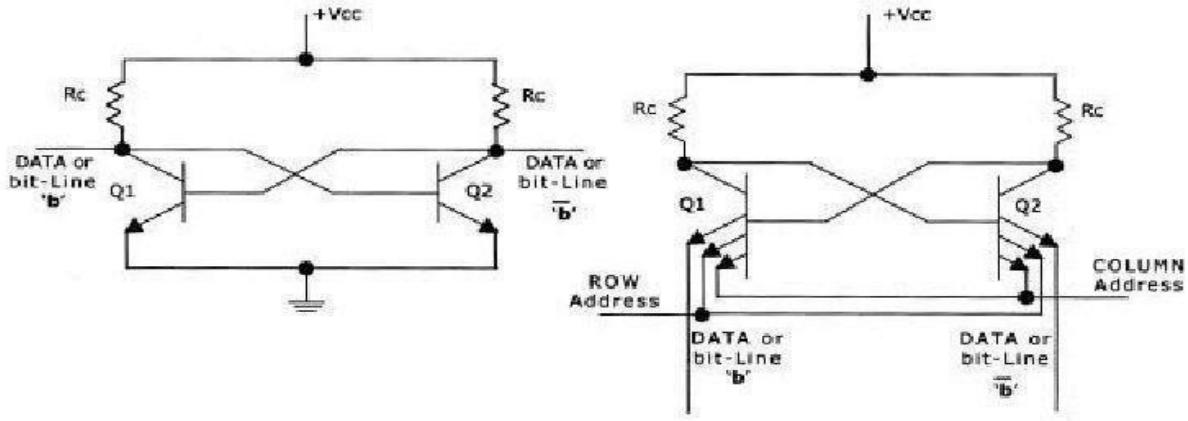
43. How the memories are classified?

It is classified into two types:

Volatile & Non-volatile memory

44. Draw the logic diagram of a static RAM cell and Bipolar cell.





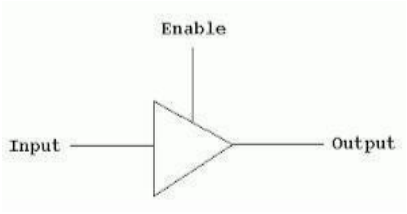
45. Give the advantages of RAM.

Read and write the data.

Data is accessed by using address of the memory location.

Higher speed.

46. Draw an active-high tri-state buffer and write its truth table.



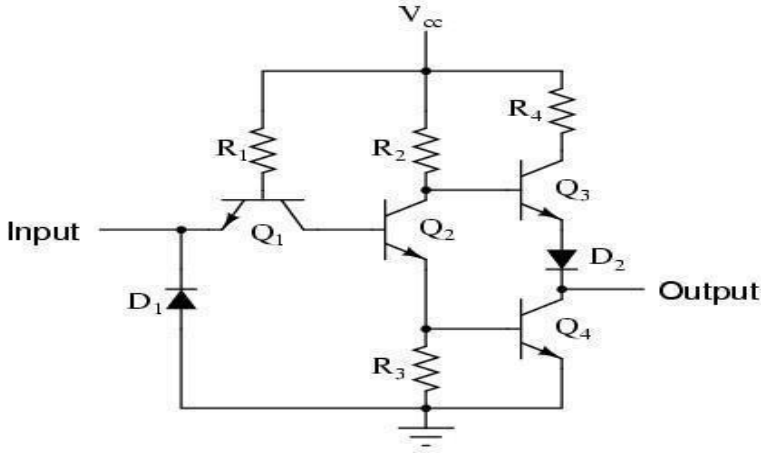
Enable	Input	Output
0	X	Z
1	0	0
1	1	1

47. What is a totem pole output?

Totem pole output is a standard output of a TTL gate. It is specifically designed to reduce the propagation delay in the circuit and to provide sufficient output power for high fan-out.

48. Draw the TTL Inverter (NOT) Circuit.

Practical inverter (NOT) circuit



49. State the advantages of CMOS logic.

Consumes less power.

Can be operated at high voltages, resulting in improved noise immunity.

Fan-out is more.

Better noise margin.

50. Write a note on tri-state gates.

It is a digital circuit that exhibits three states. Two of the states are signals equivalent to logic1 and logic 0. The third state is high impedance state. High impedance state behaves like a open circuit.

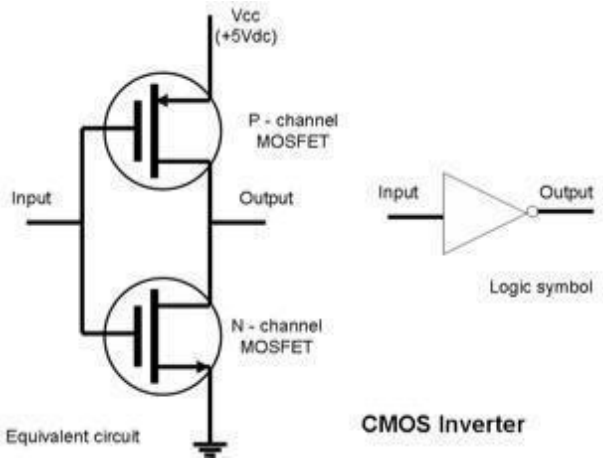
51. What is the significance of high impedance state in tri-state gates?

High impedance state of a three-state gate provides a special feature not available in other gates.Because of this features a larger number of three state gate output can be connected with wires to form a common line without endangering loading effects.

52. Define the term Fan out.

It is the maximum number of inputs which have same family that the gate can drive maintaining its output within the specified limits.

53. Draw the CMOS inverter circuit.



PART B&C

1. Implement the full adder circuit using PLA by deriving the PLA programming table. (Apr/May'19)

Refer"Digital Cicuits and Design " by S.Salivahanan &S.Arivazhagan 2nd Edition,Pg.No.434

2. Explain about the tri- state TTL output configuration with a neat diagram(Apr/May'19)

Refer "Digital Design " by Morris Mano,4th Edition Pg.No:505

3.Differentiate static and dynamic RAM. Draw the circuits of one cell of each and explain its working. (Nov/Dec 2018)

Refer"Digital Cicuits and Design " by S.Salivahanan &S.Arivazhagan 2nd Edition,Pg.No.412&419

4. Illustrate the circuit operation and characteristics of TTL NAND logic gate in detail. (Nov/Dec 2018)

Refer"Digital Cicuits and Design " by S.Salivahanan &S.Arivazhagan 2nd Edition,Pg.No.121

5.Describe the classification of semiconductor memories. (Nov/Dec 2017)

Refer"Digital Cicuits and Design " by S.Salivahanan &S.Arivazhagan 2nd Edition,Pg.No.387

6.Discuss the features and functional blocks of FPGA. (Nov/Dec 2017)

Refer"Digital Cicuits and Design " by S.Salivahanan &S.Arivazhagan 2nd Edition,Pg.No.443

7(i).Compare static and dynamic RAM.

Refer"Digital Cicuits and Design " by S.Salivahanan &S.Arivazhagan 2nd Edition,Pg.No.412

(ii).Implement the switching functions.

Z1=ab ´ d ´ e+a ´ b ´ c ´ e ´ +bc+de
Z2=a ´ c ´ e
Z3=bc+de+c ´ d ´ e ´ +bd and
Z4=a ´ c ´ e+ce using a 5*8*4 PLA. (April/May17)

Refer"Digital Cicuits and Design " by S.Salivahanan &S.Arivazhagan 2nd Edition,Pg.No.412

8. (i).Distinguish between Boolean addition and binary addition. (April/May17)

(ii).Design a combinational circuit using ROM that accepts a 3 bit binary number and generates an output binary number equal to the square of the given number.

Refer"Digital Cicuits and Design " by S.Salivahanan &S.Arivazhagan 2ndEdition,Pg.No.399

9.(i)Draw and explain Tri-state TTL inverter circuit diagram with its operation.

Refer"Digital Cicuits and Design " by S.Salivahanan &S.Arivazhagan 2nd Edition,Pg.No.127

(ii)Implement the following functions using NAND and inverter gates.

F=AB+A ´ B ´ +B ´ C (May/June ´ 16)

10.(i)Implement the following function using PLA.

F1(X,Y,Z)= ∑m(1,2,4,6)
F2(X,Y,Z)= ∑m(0,1,2,6,7)
F3(X,Y,Z)= ∑m(2,6)

Refer"Digital Cicuits and Design " by S.Salivahanan &S.Arivazhagan 2nd Edition,Pg.No.434

(ii)Write short notes on FPGA. (May/June 2016)

Refer"Digital Cicuits and Design " by S.Salivahanan &S.Arivazhagan 2nd Edition,Pg.No.412

11. Write short notes on : (i)PAL (ii)FPGA (Nov/Dec 2016)

Refer"Digital Cicuits and Design " by S.Salivahanan &S.Arivazhagan 2nd Edition,Pg.No.440&443

12. Write short notes on with suitable schematic: (i) Programmable Logic Array (PLA). (ii) Field Programmable Gate Arrays. (FPGA) (April/May 2015)

Refer"Digital Cicuits and Design " by S.Salivahanan &S.Arivazhagan 2nd Edition,Pg.No.432&443

13. (i) Explain memory decoding.

Refer "Digital Design " by Morris Mano,4th Edition Pg.No:314

(ii) Draw a RAM cell and explain its working in detail. (April/May 2015)

Refer"Digital Cicuits and Design " by S.Salivahanan &S.Arivazhagan 2nd Edition,Pg.No.411

14.(i)Write short notes on EAPROM and static RAM cell using MOSFET (Nov/Dec 2014).

Refer"Digital Cicuits and Design " by S.Salivahanan &S.Arivazhagan 2nd Edition,Pg.No.409,411

(ii)Using 8 64X8 ROM chips with an enable input and decoder construct a 512X8 ROM.

Refer"Digital Cicuits and Design " by S.Salivahanan &S.Arivazhagan 2nd Edition,Pg.No.426

15.(i)Use PLA with 3-inputs 4 AND terms and two outputs to implement the following Boolean functions. F1(A,B,C)= ∑m(3,5,6,7) , F2(A,B,C)= ∑m(1,2,3,4)

Refer"Digital Cicuits and Design " by S.Salivahanan &S.Arivazhagan 2nd Edition,Pg.No434

(ii)Compare and contrast PLA and PAL. (Nov/Dec 2014).

Refer"Digital Cicuits and Design " by S.Salivahanan &S.Arivazhagan 2nd Edition,Pg.No.432&440

16.(i)Explain the read cycle and write cycle timing parameters of a RAM with the help of timing diagram.

(ii) Draw the dynamic RAM cell and explain its operation. (May/June 2014).

Refer"Digital Cicuits and Design " by S.Salivahanan &S.Arivazhagan 2nd Edition,Pg.No.418

17.Design a BCD to Excess 3 code convertor using a PLA (May/June 2014).

18. (i) Implement the functions using PAL W=Σm(2,12,13), X=Σm(7,8,9,10,11,12,13,14,15), Y= Σm(0,2,3,4,5,6,7,8,10,11,15), Z= Σm(1,2,8,12,13) (May/June 2013)

Refer"Digital Cicuits and Design " by S.Salivahanan &S.Arivazhagan 2nd Edition,Pg.No.432&443

(ii) Implement Full adder and full subtractor using ROM

Refer"Digital Cicuits and Design " by S.Salivahanan &S.Arivazhagan 2nd Edition,Pg.No.399

19.Design and explain a 32x8 ROM (May/June 2013)

Refer"Digital Cicuits and Design " by S.Salivahanan &S.Arivazhagan 2nd Edition,Pg.No.393

20.(i) Implement using ROM a combinational logic circuit which can find 2 ´ s complement of 3bit binary number. (ii) Using ROM, implement a combinational circuit which accepts a 3 bit number and generates an output binary number equal to square of input number.

Refer"Digital Cicuits and Design " by S.Salivahanan &S.Arivazhagan 2nd Edition,Pg.No.399

21. Draw and explain Tri-state TTL inverter circuit diagram and explain its operation.

Refer"Digital Cicuits and Design " by S.Salivahanan &S.Arivazhagan 2nd Edition,Pg.No.133

B.E./B.Tech .DEGREE EXAMINATION, APRIL/MAY 2019

Third /Fourth Semester
Electronics and Communication Engineering

EC8392- DIGITAL ELECTRONICS

(Common to Medical Electronics/Biomedical Engineering/Computer and communication Engineering /Mechatronics Automation Engineering)/ Robotics and Automation Engineering)

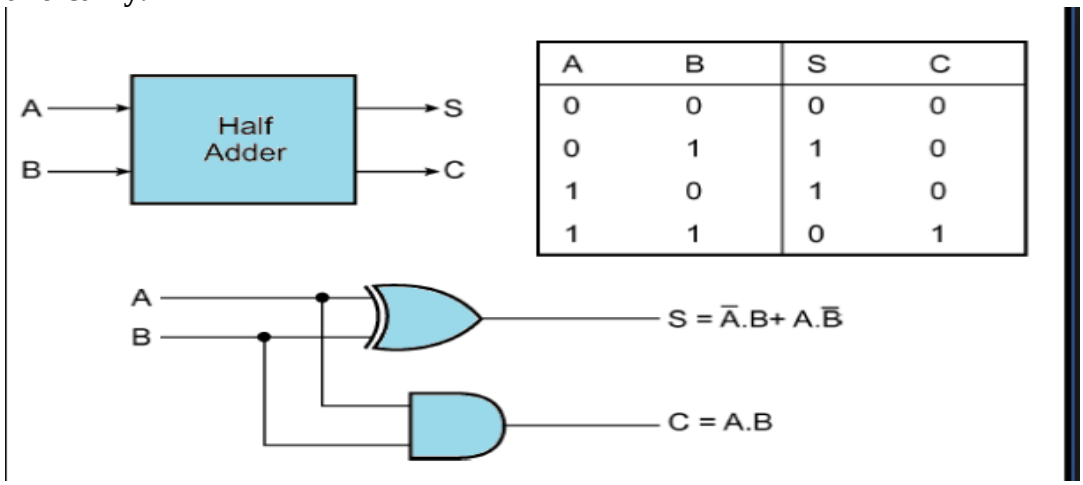
(Regulations 2017)

Time:Three hours **Maximum:100 marks**

Answer ALL Questions

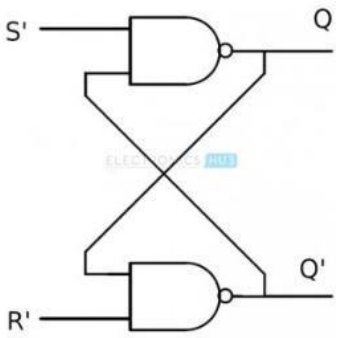
PART-A (10*2=20 marks)

1. **What is the largest binary number that can be expressed with 14 bits? Determine the equivalent decimal and hexadecimal numbers.**
   The largest binary number that can be expressed with 14 bits 11111111111111
   Decimal Equivalent=2^{14}-1=$(16.383)_{10}$
   Hexadecimal Equivalent=$(3FFF)_{16}$
2. **Find the complement of F =wx + yz and then show that FF' = 0.**
   Solution:
   (wx+yz)'=(wx)'.(yz)'=(w'+x')(y'+z')
   FF'=wx(w'+x')(y'+z')+yz(w'+x')(y'+z')=0
3. **Draw the truth table for a half adder circuit and write the Boolean expressions for sum and carry.**



A	B	S	C
0	0	0	0
0	1	1	0
1	0	1	0
1	1	0	1

4. **What is meant by a decoder circuit?**
   A binary decoder is a combinational logic circuit that converts binary information from the n coded inputs to a maximum of 2^n unique outputs
5. **Draw the logic diagram and function table of a SR latch implemented using NAND gates.**



$\bar{S}$	$\bar{R}$	Q	State
1	1	Previous State	No change
1	0	0	Reset
0	1	1	Set
0	0	?	Forbidden

6. **How many flip flops will be complemented in a 10- bit ripple counter to reach the next count after this count of '1001100111'?**
   4 flipflops need to be complemented.

   To calculate the number of flip-flops that will be complemented in a 10-bit binary counter to reach the next count after the given one is:

   • Add 1 to the given binary number.

   • And see how many bits have toggled to generate the next sequence.

   • The number of bits that has changed is the number of flip-flops required to reach the next counter.

   Add 1 to the binary number 1001100111.

   ```
   1001100111
   +          1
   ----------
   1001101000
   ----------
   ```

   • Four bits have toggled to generate the next sequence.

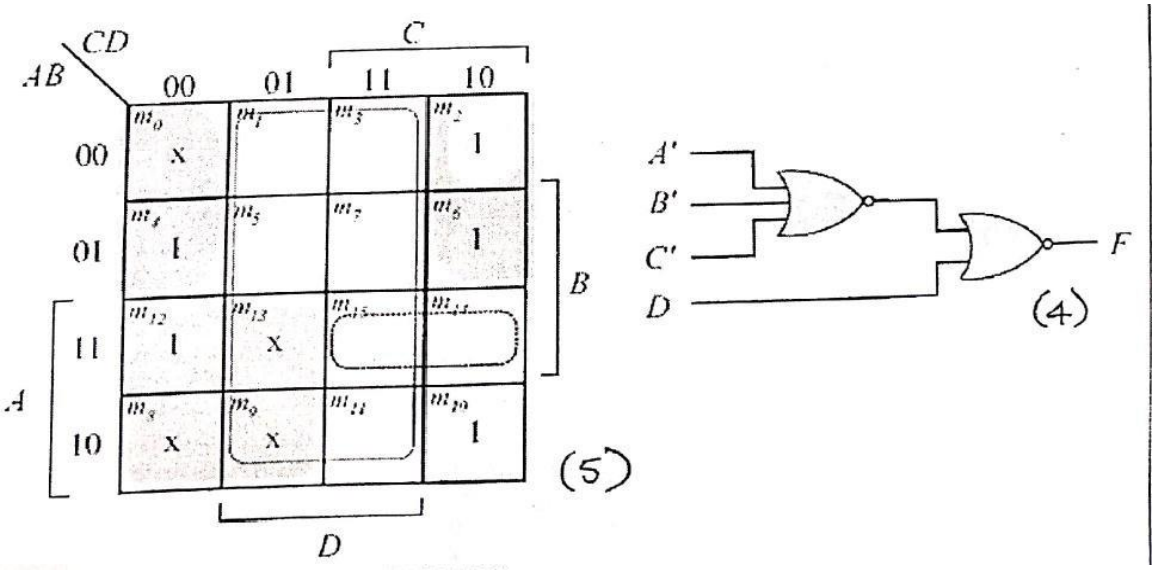
   • Therefore **four** flip-flops must be complemented to reach the next sequence.

7. **Define a 'flow table".**
   In the design of asynchronous sequential circuits,it is more convenient to name the states by letter symbols without making specific reference to their binary values.Such a table is called flowtable.
8. **Distinguish between non-critical race and critical race.**
   A **non-critical race** condition occurs when the sequence in which internal variables' changes do not have any impact on the final state of the machine. **Race** conditions are notorious for being difficult to troubleshoot, as reproduction depends on the relative timing **between the different** elements.
9. **A DRAM ship uses two dimensional address multiplexing. It has 13 common address pins with the row address having one bit more than the column address. What is the capacity of the memory?**
   Solution:
   13+12 = 25 Address lines, => Memory Capacity = 225 words
10. **A standard TTL gate has the following current specifications I_{OH}=400 µA,I_{IH}=40µA,I_{OL}=16 mA,I_{IL}=1.6mA.Calculate fanout.**
    Solution:
    a)Fanout(HIGH)= I_{OH}/ I_{IH}=400µA/40 µA
    Fanout(HIGH)=10 µA
    b)Fanout(LOW)= I_{OL}/ I_{IL}=**16 mA /1.6mA**
    Fanout(LOW)=10 mA

PART B(5*13=65 marks)

11. Use Karnaugh map method to simplify the following Boolean function F(A,B,C,D)= ∑m(2,4,6,10,12)+ ∑d(0,8,9,13).Implement the booloean function ,F using not more than two NOR gates.

Solution:



$$F = AC' + A'D' + B'CD'$$

$$F' = D + ABC$$

$$F = [D + ABC]' = [D + (A' + B' + C')']' \quad (4)$$

Or

(b) Implement the following function using Quine McCluskey method F= ∑m(6 7 8 9) +∑d (10,11,12,13,14,15)

Solution:

Column 1		Column 2	Column 3	Column 4
Index	Minterm	Pairs	Quads	Octets
Index 1	8 ✓	8, 9 (1) ✓	8, 9, 10, 11 (1, 2) ✓	8, 9, 10, 11, 12, 13, 14, 15 (1, 2, 4)
	6 ✓	8, 10 (2) ✓	8, 9, 12, 13 (1, 4) ✓	
	9 ✓	8, 12 (4) ✓	8, 10, 12, 14 (2, 4) ✓	
Index 2	10 ✓	6, 7 (1) ✓	6, 7, 14, 15 (1, 8) Q	
	12 ✓	6, 14 (8) ✓	9, 11, 13, 15, (2, 4) ✓	
	7 ✓	9, 11 (2) ✓	10, 11, 14, 15 (1, 4) ✓	
	11 ✓	9, 13 (4) ✓	12, 13, 14, 15 (1, 2) ✓	
Index 3	13 ✓	10, 11 (1) ✓		
	14 ✓	10, 14 (4) ✓		
Index 4	15 ✓	12, 13 (1) ✓		
		12, 14 (2) ✓		
		7, 15 (8) ✓		
		11, 15 (4) ✓		
		13, 15 (2) ✓		
		14, 15 (1) ✓		

From this table, we see that the prime implicants are P -> 8, 9, 10, 11, 12, 13, 14, 15(1, 2, 4) and Q-> 6, 7, 14, 15(1, 8). The term 6, 7, 14, 15b(1, 8) means that literals with weights 1 and 8. i.e., D and A re deleted. The term 8, 9, 10, 11, 12, 13, 14, 15(1, 2, 4) means that literals with weights 1, 2 and 4., D, C and B are deleted.

In the prime implicant chart of ∑(6, 7, 8, 9) + d(10, 11, 12, 13, 14, 15) is shown in the following table.

	✓	✓	✓	✓
PI\Minterms	6	7	8	9
*P → 6, 9, 10, 11, 12, 13, 14, 15 (1, 2, 4)			x	x
*Q → 6, 7, 14, 15 (1, 8)	x	x		

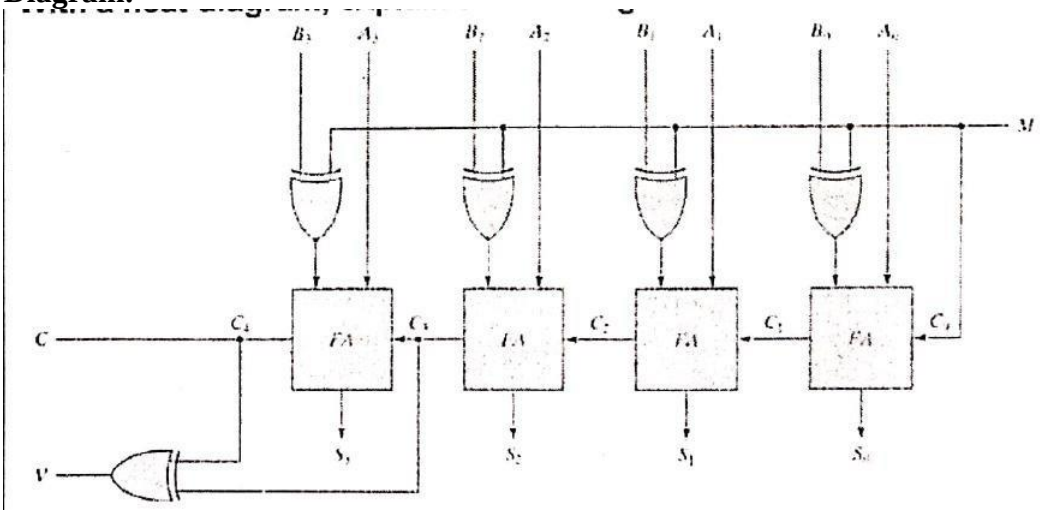
Fig 11.b: Prime Implicant Chart

Here, both P and Q are essential prime implicants. So the minimal expression is A + BC.

12 (a) With a neat diagram explain the working of a four bit adder – subtractor circuit .

Solution:

Diagram:



Operation:

The addition and subtraction operations can be combined into one circuit with one common binary adder by including an exclusive-OR gate with each full adder. The mode input M controls the operation. When *M* = 0, the circuit is an adder and when M=1, the circuit becomes a subtractor. Each exclusive-OR gate receives input *M* and one of the inputs of *B*. When M =0, we have B⊕0 =B. The full adders receive the value of B, the input carry is 0 and the circuit performs A plus B. when M =1, we have B⊕1 =B' and carry =1. The B inputs are all complemented and a 1 is added through the inpurt carry.. The circuit performs the operation A plus the 2's complement of B. The Ex-OR with output V is for detecting the overflow. (6)

Or

(b) With a truth table and logic diagram explain the operation of a four input priority encoder.

Solution:

D_0	D_1	D_2	D_3	x	y	V
0	0	0	0	X	X	0
1	0	0	0	0	0	1
X	1	0	0	0	1	1
X	X	1	0	1	0	1
X	X	X	1	1	1	1

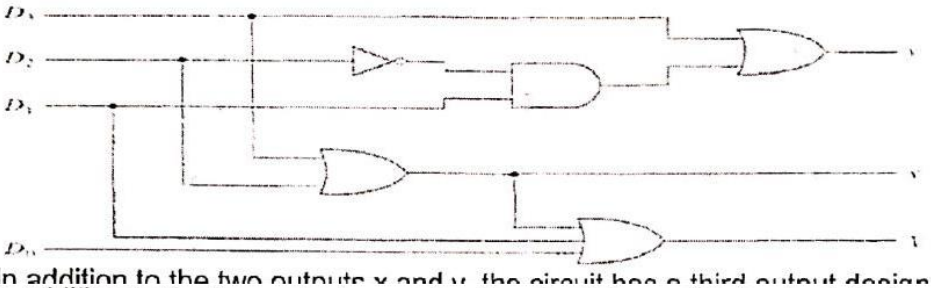
(5)

$x = D_2 + D_3$

$y = D_3 + D_1 D_2'$

(2)

$V = D_0 + D_1 + D_2 + D_3$



(3)

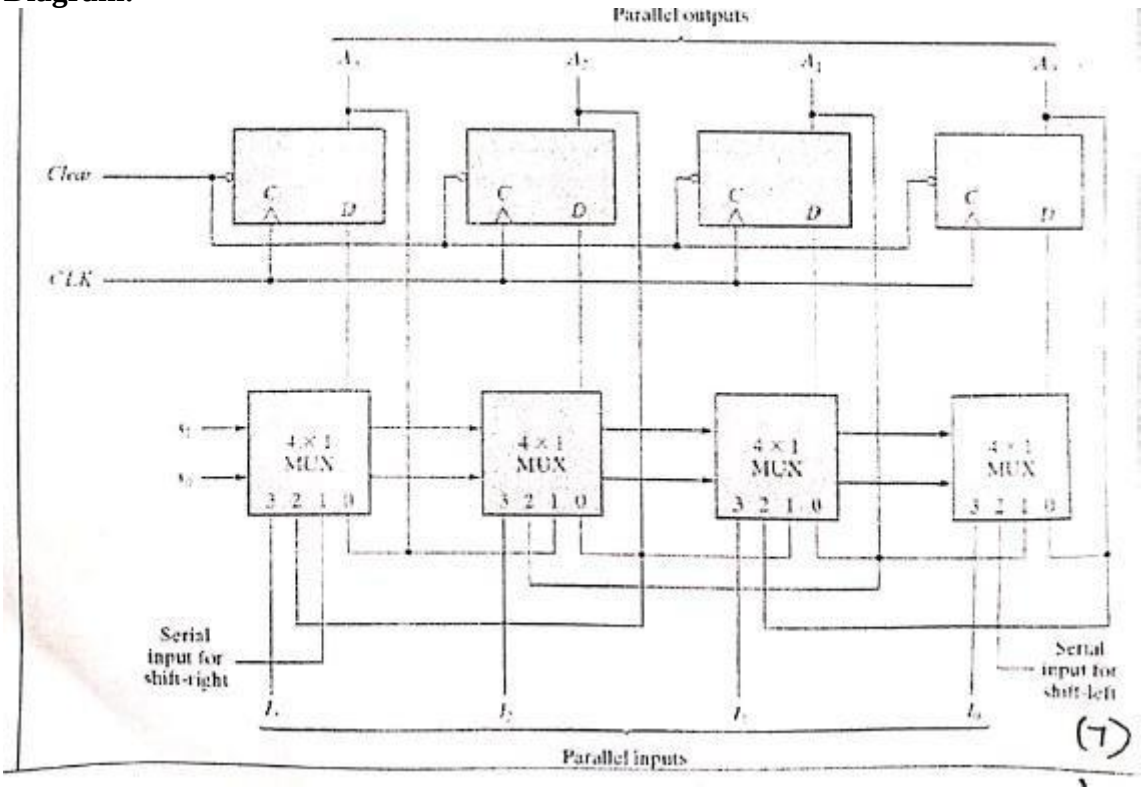
In addition to the two outputs x and y. the circuit has a third output designated by V: this is a valid bit indicator that is set to 1 when one or more inputs are equal to 1. If all inputs are 0, there is no valid input and V is equal to 0. The other two outputs are not inspected when V equals 0 and are specified as don't -care conditions.

(3)

13. (a) Draw the neat diagram of a 4 – bit universal shift register and explain it's Operation.

Solution:

Diagram:



(7)

Operation:

Some shift registers provide the necessary input and output terminals for parallel transfer. They may also have both shift-right and shift- left capabilities. The most general shift register has the following capabilities:

1. A *clear* control to clear the register to 0.
2. A *clock* input to synchronize the operations.
3. A *shift-right* control to enable the shift-right operation and the *serial input* and output lines associated with the shift right.
4. A *shift-left* control to enable the shift left operation and the *serials input* and *output lines* associated with the shift left.
5. A *parallel-load* control to enable a parallel transfer and the *n* input lines associated with the parallel transfer.
6. n parallel output lines.
7. A control state that leaves the information in the register unchanged in response to the clock. Other shift registers may have only some of the preceding functions. with atleast one shift operation.

Explanation pertaining to the operation (6)

Or

(b) A sequential circuit has two JK flip – flops A and B , two inputs x and y and one Output equation are:

$J_A = Bx + B'y'$ $\quad J_B = A'x$

$K_A = B'xy'$ $\quad K_B = A + xy'$

Draw the logic diagram and state table of the circuit .Also derive the state Equations for A and B.

Solution:

A and B:

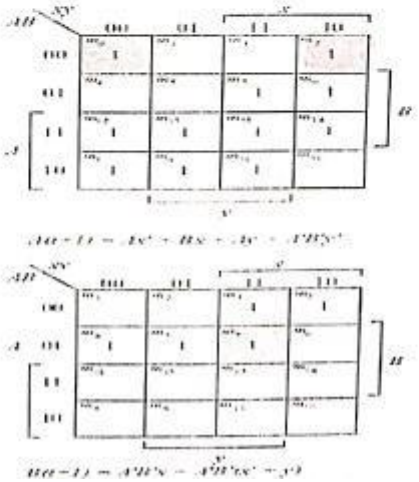
Logic Diagram (3)

State Table:

Present State A	Present State B	Inputs x	Inputs y	Next State A	Next State B	Output z	FF Outputs J_A	FF Outputs K_A	FF Outputs J_B	FF Outputs K_B
0	0	0	0	1	0	0	1	0	0	0
0	0	0	1	0	0	0	0	0	0	0
0	0	1	0	1	1	0	1	1	1	1
0	0	1	1	0	1	0	0	0	1	0
0	1	0	0	0	1	1	0	0	0	0
0	1	0	1	0	1	0	0	0	0	0
0	1	1	0	1	0	0	1	0	1	0
0	1	1	1	1	1	0	1	0	1	0
1	0	0	0	1	0	0	1	0	0	1
1	0	0	1	1	0	0	0	0	0	1
1	0	1	0	0	0	0	1	1	0	1
1	0	1	1	1	0	0	0	0	0	1
1	1	0	0	1	0	1	0	0	0	1
1	1	0	1	1	0	0	0	0	0	1
1	1	1	0	1	0	0	1	0	0	1
1	1	1	1	1	0	1	1	0	0	1

(5)

State Equation Derivation:



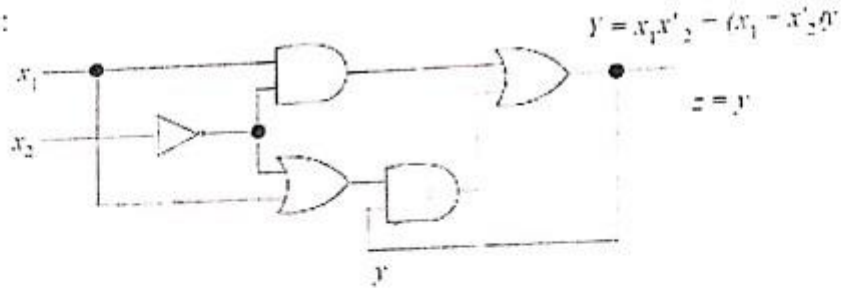
(5)

14. (a) An asynchronous sequential circuit is described by the excitation function, $Y=x_1x_2'+(x_1+x2')y$ and the output function z= y .Draw the logic diagram of the circuit .

Derive the transition table and output map. Also discuss about the behavior of the circuit.

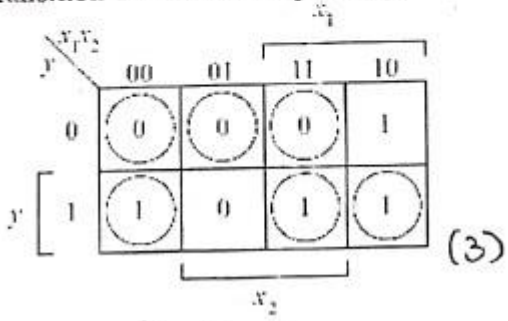
Solution:

Logic Diagram:

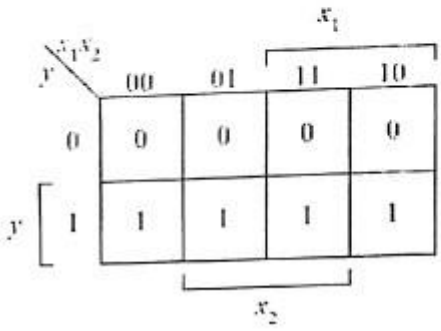


(4)

Transition Table and Output Map:



(3)



(2)

(4)

Behaviour of the Circuit:

Or

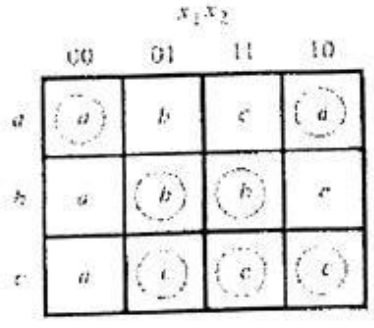
(b) Briefly explain about race –free state assignment with relevant examples.

Solution:

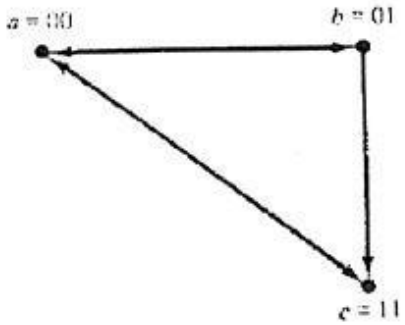
The procedure of binary state assignments by going through examples with only 3 and 4 rows in the flow table. These examples will demonstrate the general procedure that must be followed to ensure a race free assignment.

Three Row Flow Table:

It requires an assignment of two binary variables.



(a) Flow table



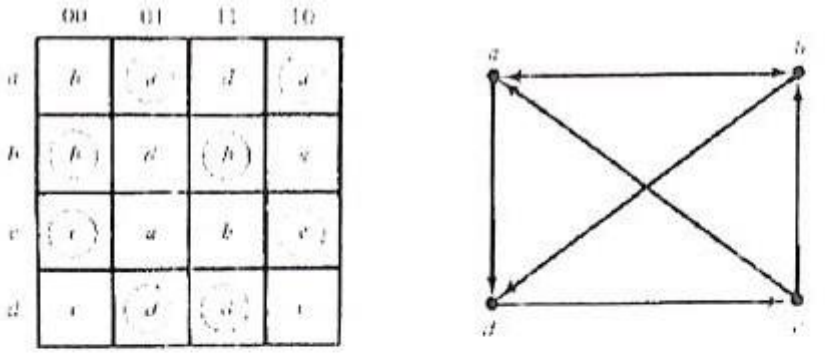
(b) Transition diagram

Three-row flow-table example

A race free assignment can be obtained if we add an extra row to the flow table. (5)

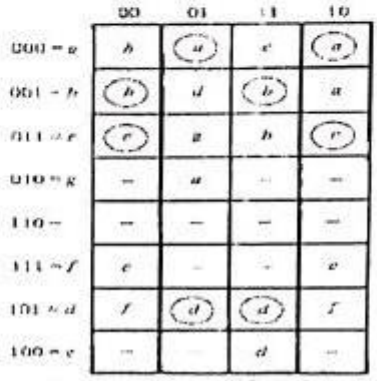
Four-Row Flow table example:

It requires a minimum of two state variables.



(a) Flow table (b) Transition diagram

Four-row flow table example

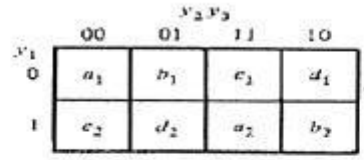


State assignment to modified flow table

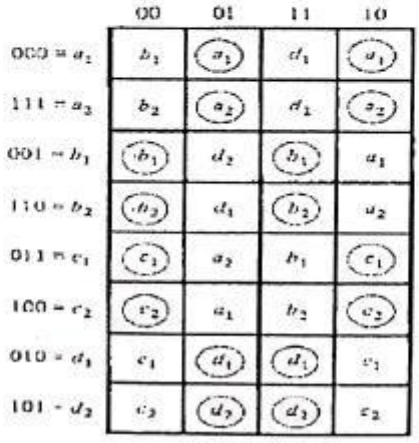
(5)

Multiple Row method :

Each state in the original flow table is replaced by two or more combinations of state variables.



(a) Binary assignment



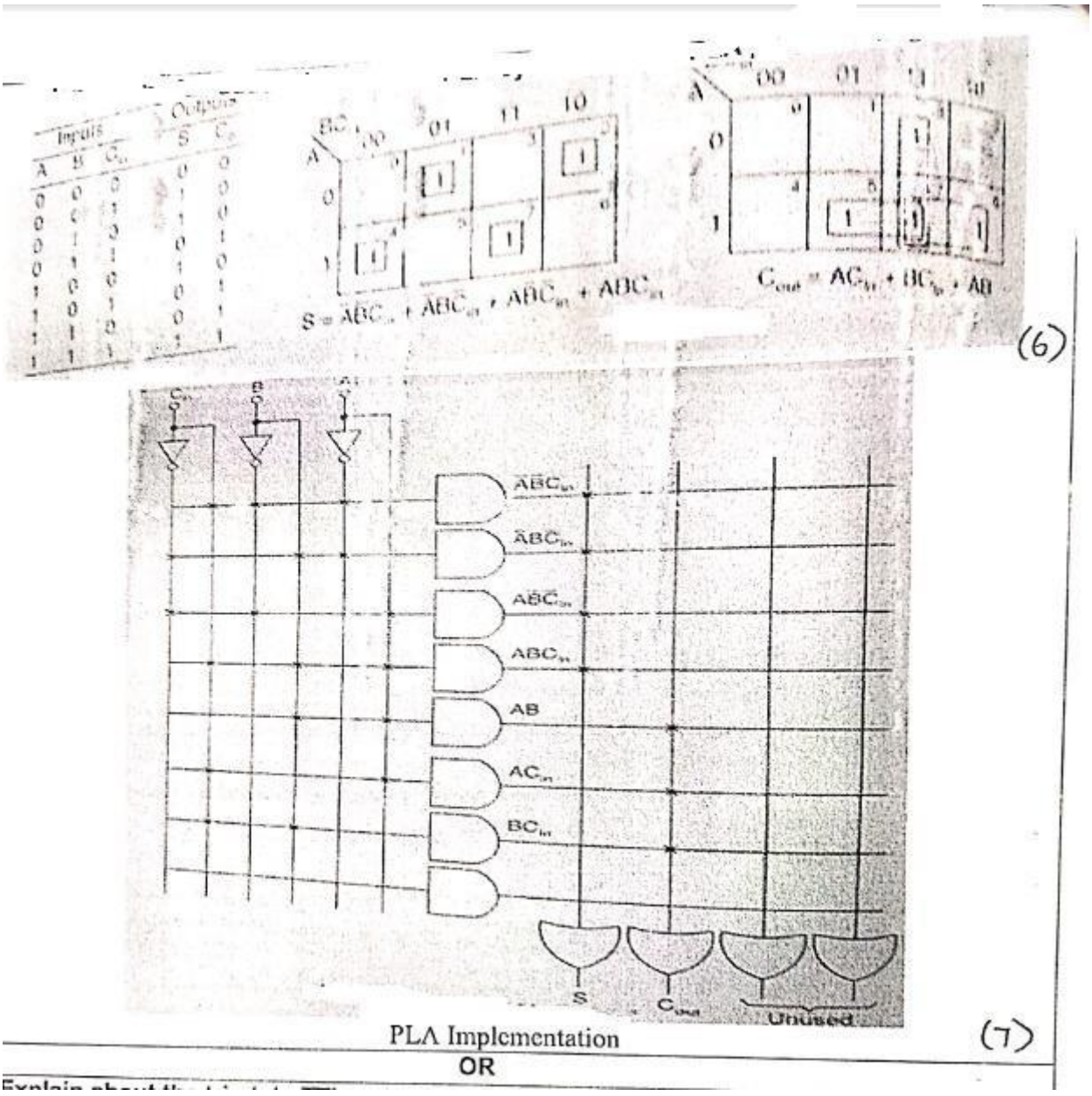
(b) Flow table

Multiple row assignment

(3)

15. (a) Implement the full adder circuit using PLA by deriving the PLA programming table.

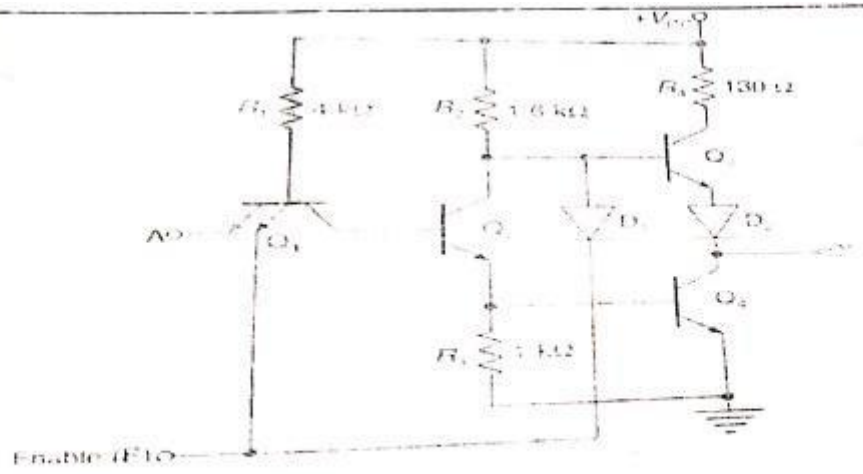
Solution:



Or

(b) Explain about the tri- state TTL output configuration with a neat diagram.
Solution:

Circuit Diagram:



(5)

Tri-state TTL inverter circuit diagram

Operation:

In this circuit, there are 2 inputs A is the normal logic input and E is an enable input that can produce the Hi-Z. With E=1, the circuit operates as a normal inverter because the high voltage at E has no effect on Q_1 or Q_2. In this condition, the output is simply the inversion of logic input A. When E=0, the circuit goes into its Hi-Z state regardless of the state of logic input A. The LOW at E forward biases the emitter base junction of Q1 and shunts the current in R1 away from Q2, so that Q2 turns off, which in turn Q4 off. The LOW at E also forward biases diode D1 to shunt current away from the base of Q3, therefore Q3 turns off. (6

PART C-(1*15=15 marks)

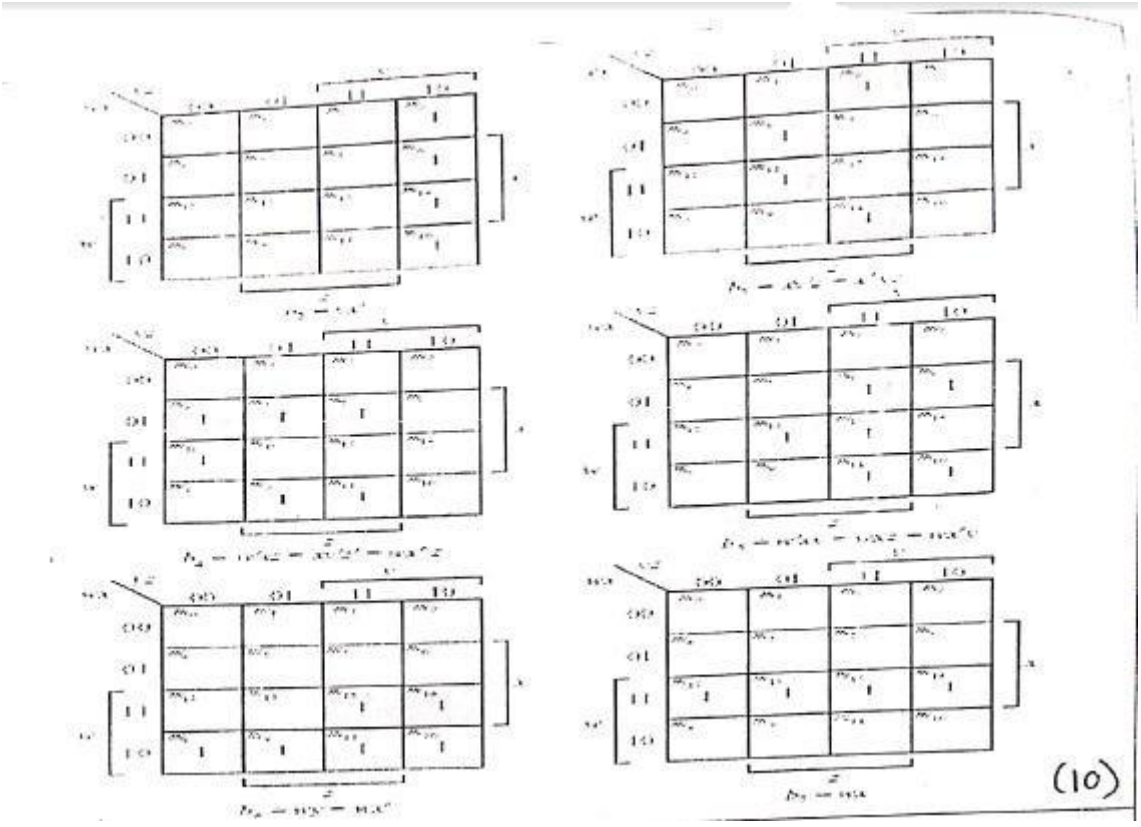
16. (a) Derive the Rom programming table for the combinational circuit that squares a 4 – bit number. Minimize the number of product terms.

Solution:

Decimal		w	x	y	z	b_7	b_6	b_5	b_4	b_3	b_2	b_1	b_0
0	0	0	0	0	0	0	0	0	0	0	0	0	0
1	1	0	0	0	1	0	0	0	0	0	0	0	1
2	4	0	0	1	0	0	0	0	0	0	1	0	0
3	9	0	0	1	1	0	0	0	0	1	0	0	1
4	16	0	1	0	0	0	0	0	1	0	0	0	0
5	25	0	1	0	1	0	0	0	1	1	0	0	1
6	36	0	1	1	0	0	0	1	0	0	1	0	0
7	49	0	1	1	1	0	0	1	1	0	0	0	1
8	64	1	0	0	0	0	1	0	0	0	0	0	0
9	81	1	0	0	1	0	1	0	1	0	0	0	1
10	100	1	0	1	0	0	1	1	0	0	1	0	0
11	121	1	0	1	1	0	1	1	1	1	0	0	1
12	144	1	1	0	0	1	0	0	1	0	0	0	0
13	169	1	1	0	1	1	0	1	0	1	0	0	1
14	196	1	1	1	0	1	1	0	0	0	1	0	0
15	225	1	1	1	1	1	1	1	0	0	0	0	1

Note: $b_0 = z$, and $b_1 = 0$. ROM would have 4 inputs and 6 outputs. A 4 x 8 ROM would waste two outputs.

(5)



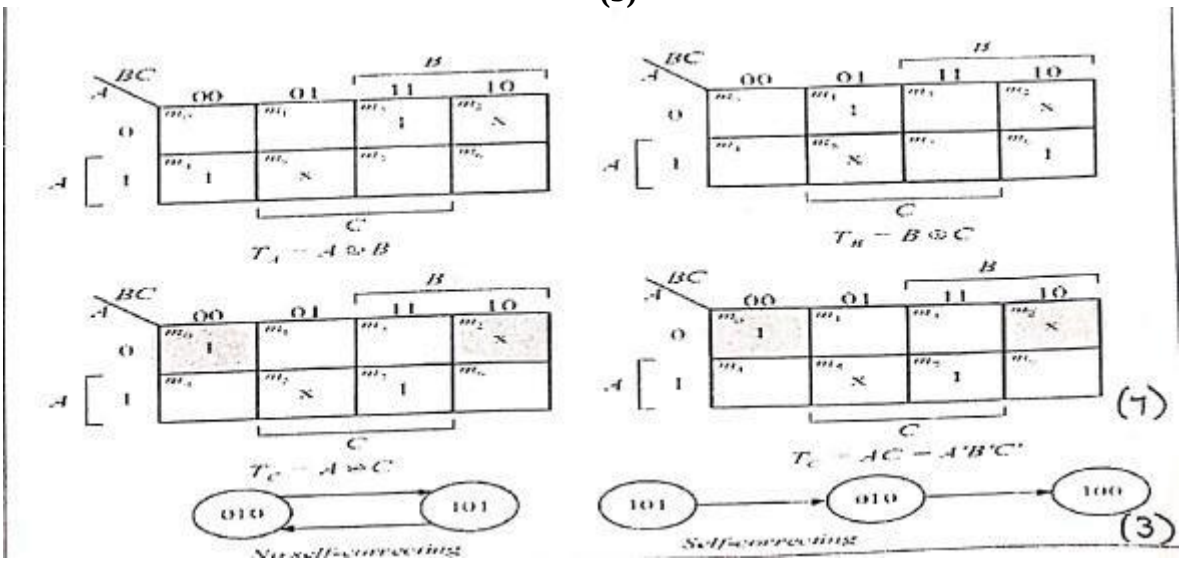
Or

(b) Design a counter with T flip –flops that goes through the following binary repeated sequence 0,1,3,7,6,4. Show that when binary states 010 and 101 are taken to be don't care conditions , the counter may not operate properly . Find a way to correct the design. (Apr/May'19)

Solution:

Present state ABC	Next state ABC	Flip-flop inputs T_A	T_B	T_C
000	001	0	0	1
001	011	0	1	0
010	XXX	X	X	X
011	111	1	1	0
100	000	1	0	0
101	XXX	X	X	X
110	100	0	1	0
111	110	0	0	1

(5)



B.E./DEGREE EXAMINATION, NOVEMBER/DECEMBER 2018

Third Semester
Electronics and Communication Engineering

EC8392- DIGITAL ELECTRONICS
(Common to B.E Medical Electronics/B.E Computer and Communication Engineering/B.E Mechatronics Engineering /B.E Robotics and Automation Engineering)
(Regulations 2017)

Time:Three hours **Maximum:100 marks**

Answer ALL Questions

PART-A (10*2=20 marks)

1. Subtract $(1010)_2$ from $(1000)_2$ using 2´s complement method. Subtract by direct method also and compare.

2 ´ s complement method:

2 ´ s complement of $(1010)_2$ = 0110

Add $(1000)_2$ with $(0110)_2$

```
  1000
 -----
  1110
 -----
```

Direct method:

```
  1000
  1010
 -------
 11110
 -------
```

2. Interpret the function Y=A+B´ C in canonical POS.

In the above three-variable expression, the function is given as sum of product form. First, the function needs to be changed to product of sum form by applying distributive law as shown below.

Y = A + B′C = (A + B′) (A + C)

Now, in the above expression, C is missing from the first term and B is missing from the second term. Hence CC′ is to be added with the first term and BB′ is to be added with the second term as shown below.

Y = (A + B′) (A + C) = (A + B′ + CC′) (A + C + BB′)

Y = (A + B′ + C) (A + B′ + C′) (A + B + C) (A + B′ + C)

3. Draw the full adder using two half Adders.

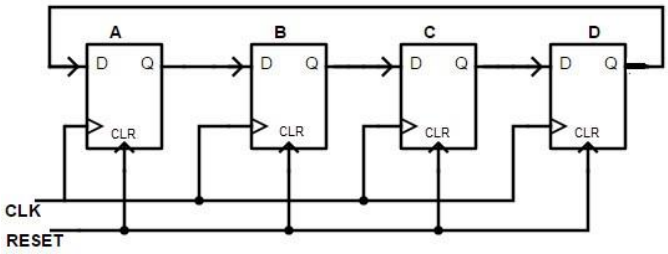
An adder is a digital circuit that performs addition of numbers. The half adder adds two binary digits called as augend and addend and produces two outputs as sum and carry; XOR is applied to both inputs to produce sum and AND gate is applied to both inputs to produce carry.

4.What do you mean by parity checker?

The parity checker is a combinational circuit that determines if the received data is correct or not. It is good for detecting a single bit error only. The parity checker can be built using Exclusive-OR gate.

5. Draw the circuit diagram of 4-bit ring counter using D ´ -flip flop.

A ring counter is a digital circuit which consists of a series of flip flops connected together in a feedback manner. The circuit is special type of shift register where the output of the last flip-flop is fed back to the input of first flip-flop. When the circuit is reset, except one of the flip-flop output, all others are made zero. For n-flip-flop ring counter we have a **MOD-n counter**. That means the counter has n different states. The circuit diagram for a 4 bit ring counter is shown below:



6. Define shift register.

Shift register: A register capable of shifting its binary information either from right to left or left to right is known as shift register. It consists of flip-flops connected in cascade. All flip-flops receive a common clock pulse which causes the shift from one stage to the next stage. It is of four basic types: 1. Serial in serial out register, 2. Serial in parallel out register 3. Parallel in serial out register and 4. Parallel in parallel out register. Bi- directional shift register and Universal shift registers are also used for different applications

7. Draw the general model of ASM.

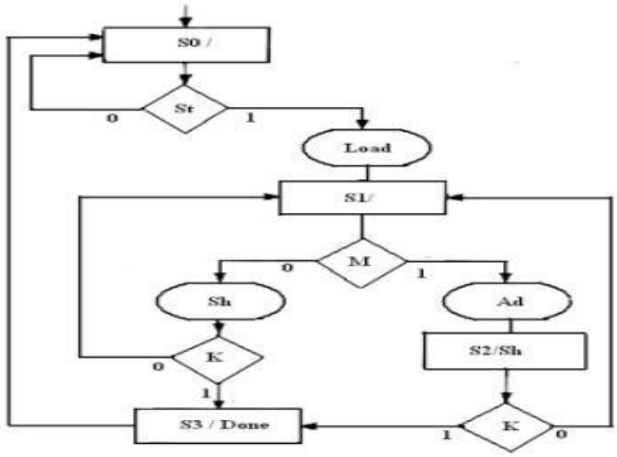


Figure: ASM chart

8. Outline critical race .

Critical race in asynchronous circuits occur between two signals that are required to change at the same time when the next stable state is dependent on the delay paths in the circuit. If it is possible to end up in two or more different stable states, depending on the order in which the state variable change, then it is called a critical race.

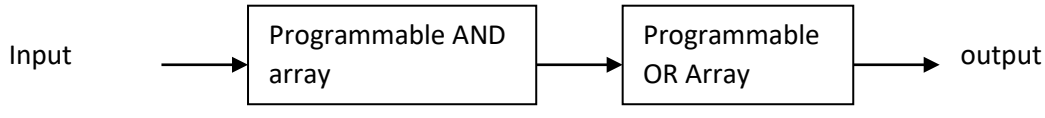
9. Interpret Read and Write operation. (Nov/Dec 2018)

Write operation: puts data into a specified address in the memory. **Read operation:** takes data out of a specified address in the memory

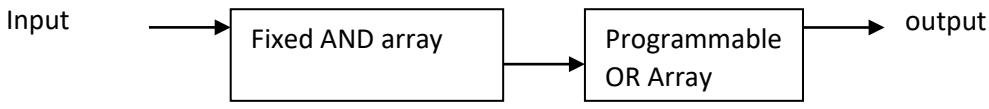
10. What is programmable logic array? How it differs from ROM?

The programmable logic array (PLA) is a programmable logic device with a programmable OR array and a programmable AND array. The Programmable Read Only Memory (PROM) is a programmable logic device with a fixed AND array and a programmable OR array.

Architecture: PAL

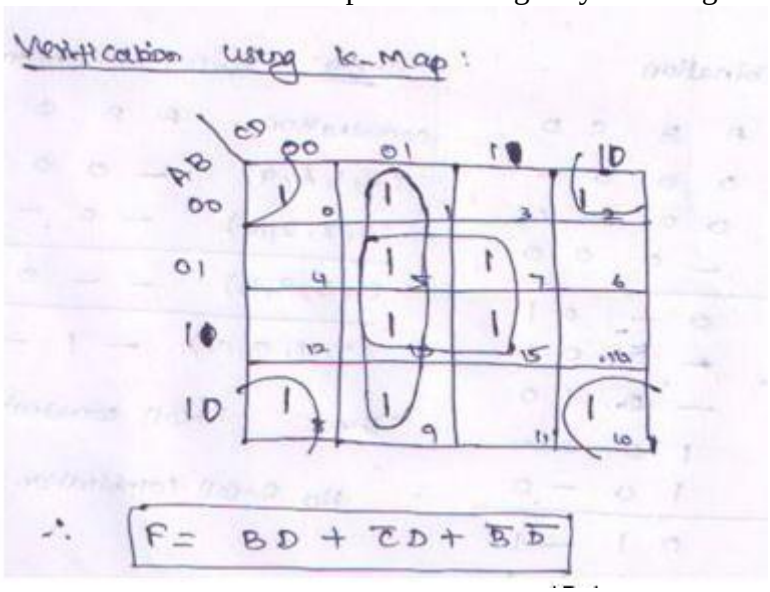


Architecture: PROM



11) a) . (i) Find the MSOP representation for

F(A,B,C,D,E) = ∑m(1,4,6,10,20,22,24,26)+ ∑d(0,11,16,27) using K-Map. Draw the circuit of minimal expression using only NAND gates.



(ii) Implement Y=(AB)´ + A + (B+C)´ using NAND gates only.

Any logical expression can be implemented as either using NAND only circuit or NOR only circuit. This is because one can make the basic gates (AND, OR and NOT) using only NAND and only NOR gates. So using this fact, we can draw the NAND only circuit for any logical expression following the steps given below:

Draw the circuit using basic gates. (Use 2-input AND and OR gates, as you have only 2-input NAND gates)

Replace these basic gates using their NAND equivalent.

NOT is NAND with shorted inputs

AND is NAND followed by NOT

OR is NAND with inverted inputs

Simplify the circuit if possible (two NOT gates can come in series, one after the other, and can be replaced with a short).

Or

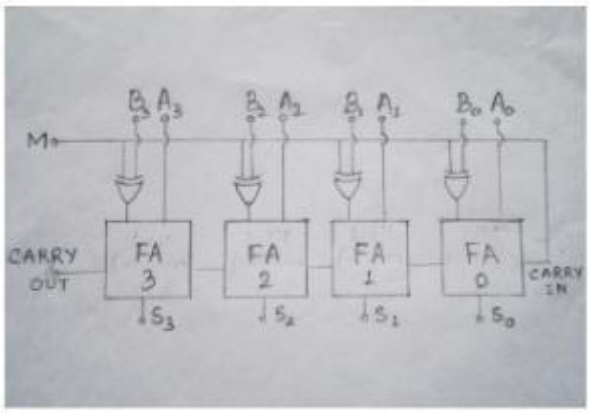
11. (b) What are the advantages of using Quine McCluskey method? Determine the minimal sum of products for the Boolean expression F(A,B,C,D) = ∑m(1,2,3,9,12,13,14)+ ∑d(0,7,10,15) using Quine McCluskey Tabular method. **(13))**

Solution:

Advantages of using Quine McCluskey method: QM Method is applicable for simplification of Boolean expression with more than 5 variables.

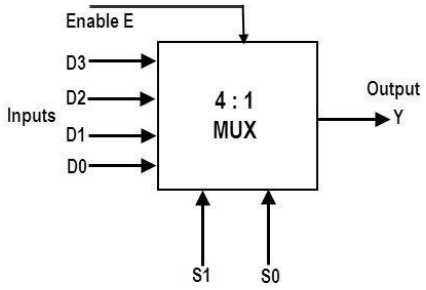
- Binary representation of Minterms------1 mark
- Minterms according to number of 1"s -------- 1mark
- 2-cell combinations ---------- 2 marks
- 4-cell combinations ---------- 2 marks
- Prime Implicants Table---------- 2 marks
- Final Boolean Expression----------5 marks

12 (a)(i) With neat circuit diagram, explain the working principle of 4-bit parallel Adder/Subtractor? (8)



(ii) Illustrate the concept of basic 4-input Multiplexer. (5)

A 4-to-1 multiplexer consists four data input lines as D0 to D3, two select lines as S0 and S1 and a single output line Y. The select lines S1 and S2 select one of the four input lines to connect the output line. The particular input combination on select lines selects one of input (D0 through D3) to the output.---1 mark

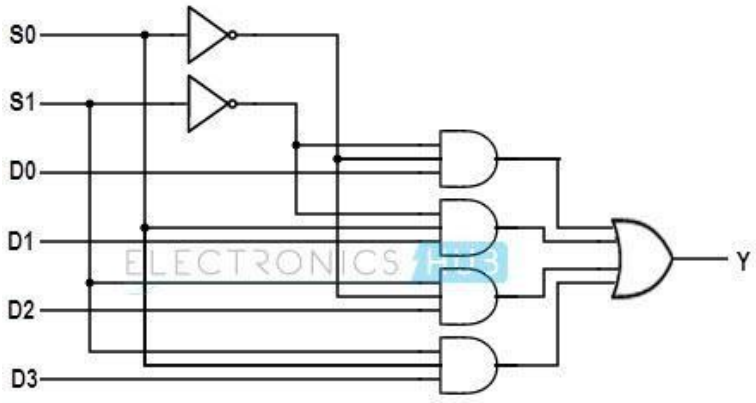


Select Data Inputs		Output
S_1	S_0	Y
0	0	D_0
0	1	D_1
1	0	D_2
1	1	D_3

-----**1mark**

If S1=0 and S0=0 then Y = D0, Therefore, Y = D0 $(S1)^{-}$ $(S0)^{-}$
If S1= 0 and S0=1, the Y = D1, Therefore, Y = D1 $(S1)^{-}$ S0
If S1=1 and S0=0, then Y = D2, Therefore, Y = D2 S1 $(S0)^{-}$
If S1=1 and S0=1 the Y = D3, Therefore, Y = D3 S1 S0------**1 mark**

$$\mathbf{Y = D0\,\overline{S1}\,\overline{S0} + D1\,\overline{S1}\,S0 + D2\,S1\,\overline{S0} + D3\,S1\,S0}$$



---2 marks

Or

(b) Design and describe the operation of 3- bit magnitude comparator. (13)

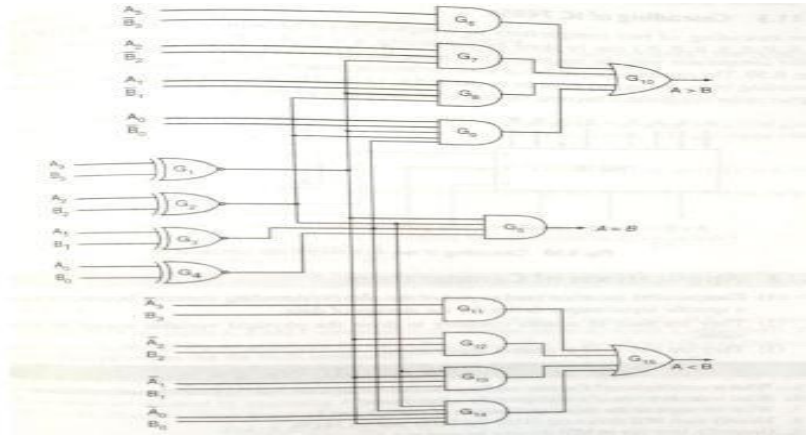
Definition:A magnitude digital Comparator is a combinational circuit that **compares two digital or binary numbers** in order to find out whether one binary number is equal, less than or greater than the other binary number. We logically design a circuit for which we will have two inputs one for A and other

for B and have three output terminals, one for A > B condition, one for A = B condition and one for A < B condition----------**2 marks**

Truth Table:3 marks

Comparing inputs				Cascading inputs			Outputs		
A_3, B_3	A_2, B_2	A_1, B_1	A_0, B_0	$A > B$	$A < B$	$A = B$	$A > B$	$A < B$	$A = B$
$A_3 > B_3$	X	X	X	X	X	X	1	0	0
$A_3 < B_3$	X	X	X	X	X	X	0	1	0
$A_3 = B_3$	$A_2 > B_2$	X	X	X	X	X	1	0	0
$A_3 = B_3$	$A_2 < B_2$	X	X	X	X	X	0	1	0
$A_3 = B_3$	$A_2 = B_2$	$A_1 > B_1$	X	X	X	X	1	0	0
$A_3 = B_3$	$A_2 = B_2$	$A_1 < B_1$	X	X	X	X	0	1	0
$A_3 = B_3$	$A_2 = B_2$	$A_1 = B_1$	$A_0 > B_0$	X	X	X	1	0	0
$A_3 = B_3$	$A_2 = B_2$	$A_1 = B_1$	$A_0 < B_0$	X	X	X	0	1	0
$A_3 = B_3$	$A_2 = B_2$	$A_1 = B_1$	$A_0 = B_0$	1	0	0	1	0	0
$A_3 = B_3$	$A_2 = B_2$	$A_1 = B_1$	$A_0 = B_0$	0	1	0	0	1	0
$A_3 = B_3$	$A_2 = B_2$	$A_1 = B_1$	$A_0 = B_0$	0	0	1	0	0	1

Logical Diagram:5 marks



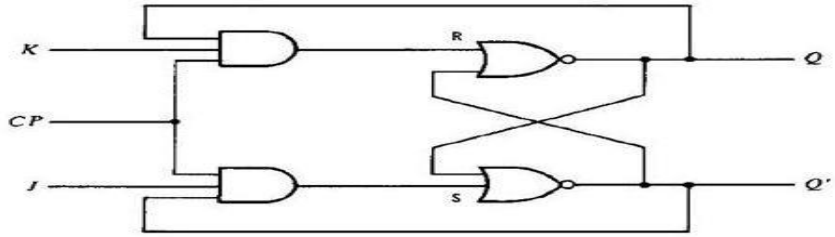
Explanation: 3 marks

13(a)(i)Explain the operation of JK flip-flop with neat diagram. (7)

Definition: 1 mark

JK flip-flop is a controlled Bi-stable latch where the clock signal is the control signal

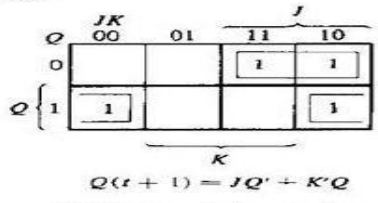
Logical diagram:2 marks



(a) Logic diagram

Q	J	K	Q(t + 1)
0	0	0	0
0	0	1	0
0	1	0	1
0	1	1	1
1	0	0	1
1	0	1	0
1	1	0	1
1	1	1	0

(b) Characteristic table



$Q(t+1) = JQ' + K'Q$

(c) Characteristic equation

OPERATION: 4 Marks

When J=0, K=1

When J=0, the output of the AND gate corresponding to J becomes 0 (i.e.) S=0 and R=1. Therefore Q‟ becomes 0. This condition will reset the flip-flop. This represents the RESET state of Flip-flop.

When J=1, K=0

In this case, the AND gate corresponding to K becomes 0(i.e.) S=1 and R=0. Therefore Q becomes 0. This condition will set the Flip-flop. This represents the SET state of Flip-flop.

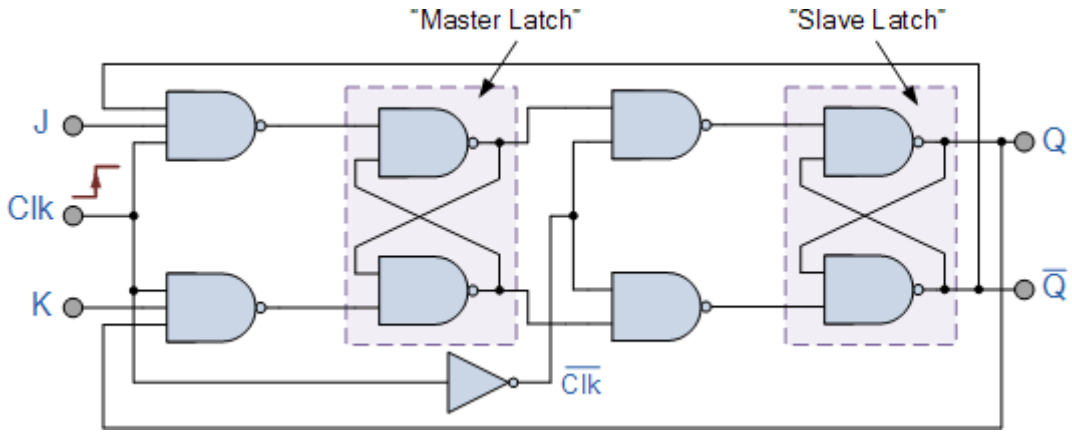
When J=K=1

Consider the condition of CP=1 and J=K=1. This will cause the output to complement again and again. This complement operation continues until the Clock pulse goes back to 0. Since this condition is undesirable, we have to find a way to eliminate this condition. This undesirable behavior can be eliminated by Edge triggering of JK flip-flop or by using master slave JK Flip-flops.

(ii) Explain the operation of master slave flip flop and show ,how the Race around condition is eliminated. (6)

The **Master-Slave Flip-Flop** is basically two gated SR flip-flops connected together in a series configuration with the slave having an inverted clock pulse. The outputs from Q and Q from the “Slave” flip-flop are fed back to the inputs of the “Master” with the outputs of the “Master” flip flop being connected to the two inputs of the “Slave” flip flop **1mark**

Logical diagram---- 2 marks



Operation: 3 marks

The input signals J and K are connected to the gated "master" SR flip flop which "locks" the input condition while the clock (Clk) input is "HIGH" at logic level "1". As the clock input of the "slave" flip flop is the inverse (complement) of the "master" clock input, the "slave" SR flip flop does not toggle. The outputs from the "master" flip flop are only "seen" by the gated "slave" flip flop when the clock input goes "LOW" to logic level "0".

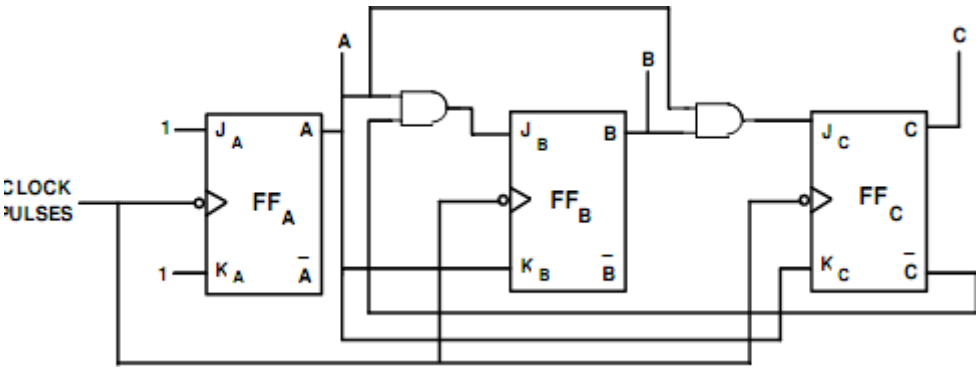
When the clock is "LOW", the outputs from the "master" flip flop are latched and any additional changes to its inputs are ignored. The gated "slave" flip flop now responds to the state of its inputs passed over by the "master" section.

Then on the "Low-to-High" transition of the clock pulse the inputs of the "master" flip flop are fed through to the gated inputs of the "slave" flip flop and on the "High-to-Low" transition the same inputs are reflected on the output of the "slave" making this type of flip flop edge or pulse-triggered.

Then, the circuit accepts input data when the clock signal is "HIGH", and passes the data to the output on the falling-edge of the clock signal. In other words, the Master-Slave JK Flip flop is a "Synchronous" device as it only passes data with the timing of the clock signal.

Or

(b)Explain the operation of synchronous MOD-6 counter. (13)



	$\bar{B}\bar{C}$	$\bar{B}C$	BC	$B\bar{C}$
$\bar{A}$	1	1	X	1
A	X	X	X	X

Map for J_A
$J_A = 1$
Fig.(i)

	$\bar{B}\bar{C}$	$\bar{B}C$	BC	$B\bar{C}$
$\bar{A}$	X	X	X	X
A	1	1	X	1

Map for K_A
$K_A = 1$
Fig.(ii)

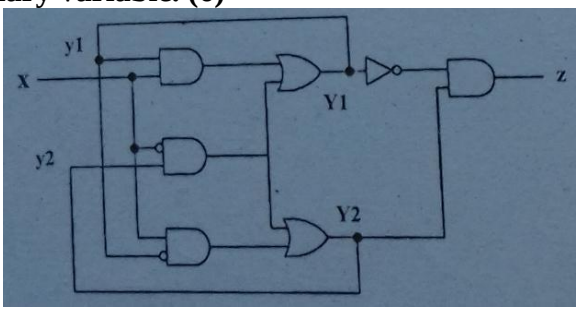
	$\bar{B}\bar{C}$	$\bar{B}C$	BC	$B\bar{C}$
$\bar{A}$	0	0	X	X
A	1	0	X	X

Map for J_B
$J_B = A\bar{C}$
Fig.(iii)

	$\bar{B}\bar{C}$	$\bar{B}C$	BC	$B\bar{C}$
$\bar{A}$	X	X	X	0
A	X	X	X	1

Map for K_B
$K_B = A$
Fig.(iv)

14 (a) (i) Write logical equations and construct transition table for the circuit output in terms of the circuit inputs and secondary variable. (6)



(ii) Explain Race-Free state Assignment in detail, with an example. (7)

Once a reduced flow table has been derived for an asynchronous sequential circuit, the next step in the design is to assign binary variables to each stable state. This assignment results in the transformation of the flow table into its equivalent transition table. The primary objective in choosing a proper binary state assignment is the prevention of critical races. Critical races can be avoided by making a binary state

assignment in such a way that only one variable changes at any given time when a state transition occurs in the flow table **2 marks**

✓ **Three-Row Flow-Table Example**

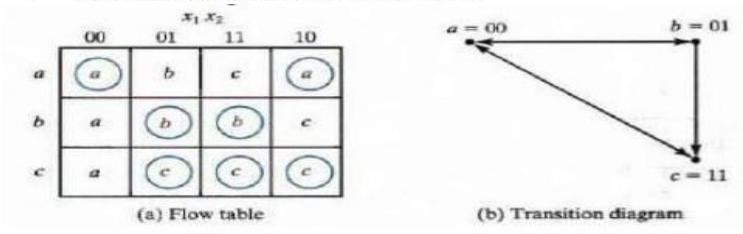


Fig: Three row flow table example **---------2 marks**

To avoid critical races, we must find a binary state assignment such that only one binary variable changes during each state transition. An attempt to find such an assignment is shown in the transition diagram. State a is assigned binary 00, and state c is assigned binary 11. This assignment will ca use a critical race during the transition from a to c because there are two changes in the binary state variables and the transition from a to c may occur directly or pass through b. Note that the transition from c to a also ca uses a race condition, but it is noncritical because the transition does not pass through other states.

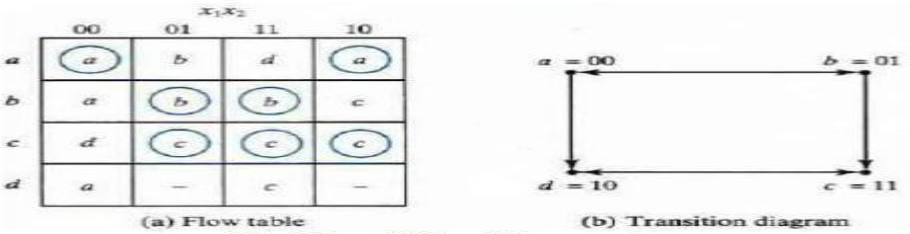


Fig: Flow table with an extra row

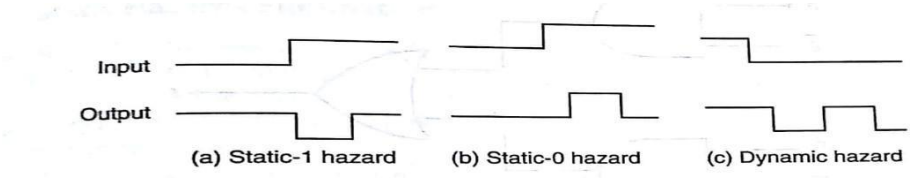
A race-free assignment is possible if we add an extra row to the flow table, as shown in Fig. The use of a fourth row does not increase the number of binary state variables, but it allows the formation of cycles between two stable states

Or

(b)(i) Draw timing diagram and explain the types of hazard in detail. (7)

- **Static 1-hazard:** The output may momentarily go to 0 when it should remain 1. ---(**1 mark)**
- **Static 0-hazard:** The output may momentarily go to 1 when it should remain 0 -----(**1 mark**)
- **Dynamic hazard** causes the output to change three or more times when it should change from 1 to 0 or from 0 to 1.....(**2 marks)**
- **Essential Hazard:**An essential Hazard is caused by unequal delays along two or more paths that originate from the same input. An excessive delay through an inverter circuit in comparison to the adding redundant gates as in static hazards. To avoid essential hazard, each feedback loop must be handled with individual care to ensure that the delay in the feedback path is long enough compared to delays of other signals that originate from the input terminals.----- (**2 marks)**

➢ **Diagram 1 mark**

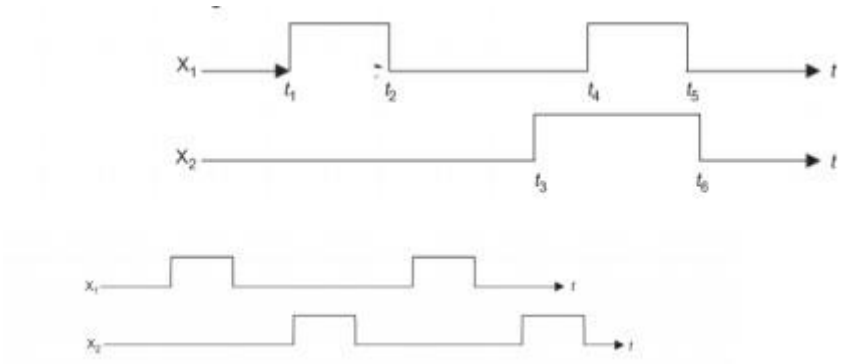


(ii) Explain pulse mode sequential circuit in detail. (6)

In pulse mode, the inputs and outputs are represented by pulses. In this mode of operation the width of the input pulses is critical to the circuit operation. The input pulse must be long enough for the circuit to respond to the input but it must not be so long as to be present even after new state is reached. In such a situation the state of

the circuit may make another transition. The minimum pulse width requirement is based on the propagation delay through the next state logic .

The maximum pulse width is determined by the total propagation delay through the next state logic and the memory elements .In pulse-mode operation, only one input is allowed to have pulse present at any time. This means that when pulse occurs on any one input, while the circuit is in stable state, pulse must not arrive at any other input. X1 and X2 are the two inputs to a pulse mode circuit. In the diagram at time t3 pulse at input X2 arrives. While this pulse is still present, another pulse at X1 input arrives at t4. Therefore, this kind of the presence of pulse inputs is not allowed. Both fundamental and pulse mode asynchronous sequential circuits use unclocked S-R flip-flops or latches. In the design of both types of circuits, it is assumed that a change occurs in only one inputs and no changes occurs in any other inputs until the circuit enters a stable state.



15. (a) . Differentiate static and dynamic RAM. Draw the circuits of one cell of each and explain its working. (13)

SRAM (**static RAM**) is random access memory (**RAM**) that retains data bits in its memory as long as power is being supplied. Unlike **dynamic RAM** (DRAM), which stores bits in cells consisting of a capacitor and a transistor, **SRAM** does not have to be periodically refreshed. ---- ---------- **3 Marks**

SRAM CELL Diagram with explanation ---------- 5 Marks

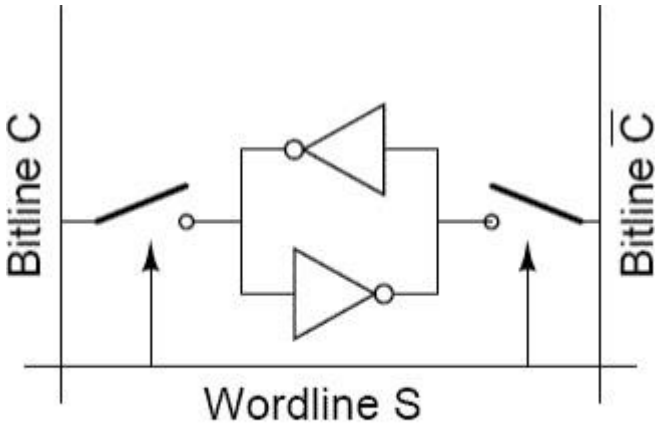
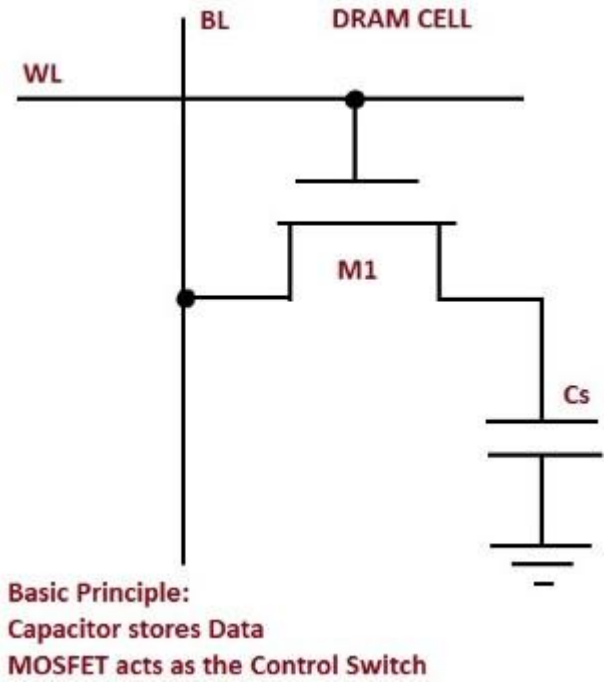


Fig 28.11: SRAM Cell

DRAM CELL Diagram with explanation ---------- 5 Marks



Or

(b) Illustrate the circuit operation and characteristics of TTL NAND logic gate in detail(13)

Definition:TTL inputs are the emitters of bipolar transistors. In the case of NAND inputs, the inputs are the emitters of multiple-emitter transistors, functionally equivalent to multiple transistors where the bases and collectors are tied together.[12] The output is buffered by a common emitter amplifier.

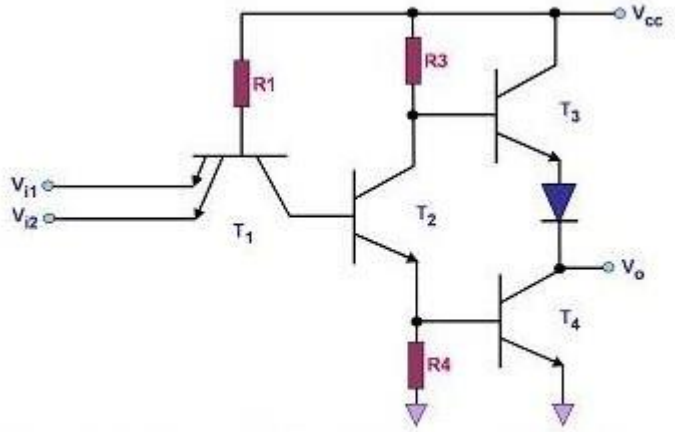


Figure 1. A 2-input TTL NAND Gate with a Totem Pole Output Stage

CASE 1:In the TTL NAND gate of Figure 1, applying a logic '1' input voltage to both emitter inputs of T1 reverse-biases both base-emitter junctions, causing current to flow through R1 into the base of T2, which isdriven into saturation. When T2 starts conducting, the stored base charge of T3 dissipates through the T2collector, driving T3 into cut-off. On the other hand, current flows into the base of T4, causing it to saturate and pull down the output voltage Vo to logic '0', or near ground. Also, since T3 is in cut-off, no current will flow from Vcc to the output, keeping it at logic '0'. Note that T2 always provides complementary inputs to the bases ofT3 and T4, such that T3 and T4 always operate in opposite regions, except during momentary transition between regions.

CASE2: On the other hand, applying a logic '0' input voltage to at least one emitter input of T1 will forward-bias the corresponding base-emitter junction, causing current to flow out of that emitter. This causes the stored base charge of T2 to discharge through T1, driving T2 into-cut-off. Now that T2 is in cut-off, current from Vcc will be diverted to the base of T3 through R3, causing T3 to saturate. On the other hand, the base of T4 will be deprived

of current, causing T to go into cut-off. With T4 in cut-off and T3 in saturation, the output Vo is pulled up to logic '1', or closer to Vcc.

PART C –

16. (a)Design a synchronous sequence detector that produces an output 1,Whenever non overlapping sequence 1011 is detected. (15)

Solution: Step 1 – Derive the State Diagram and State Table for the Problem

Step 1 – Derive the State Diagram and State Table for the Problem

Step 1a – Determine the Number of States

We are designing a sequence detector for a 5-bit sequence, so we need 5 states. We label these states A, B, C, D, and E. State A is the initial state.

Step 1b – Characterize Each State by What has been Input and What is Expected

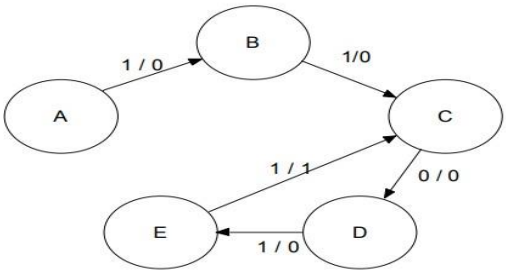
State	Has	Awaiting
A	--	11011
B	1	1011
C	11	011
D	110	11
E	1101	1

Step 1b – Characterize Each State by What has been Input and What is Expected State Has Awaiting A -- 11011 B 1 1011 C 11 011 D 110 11 E 1101 1

Step 1c –

Step 1c – Do the Transitions for the Expected Sequence

Here is a partial drawing of the state diagram. It has only the sequence expected. Note that the diagram returns to state C after a successful detection; the final 11 are used again.



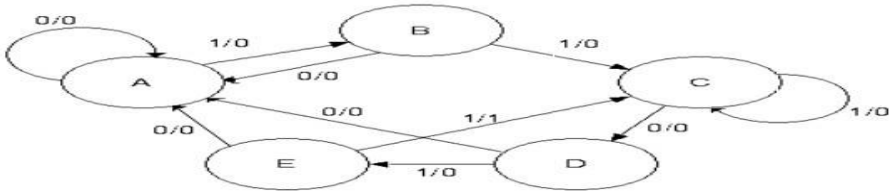
Note the labeling of the transitions: X / Z. Thus the expected transition from A to B has an input of 1 and an output of 0.

The transition from E to C has an output of 1 denoting that the desired sequence has been detected.

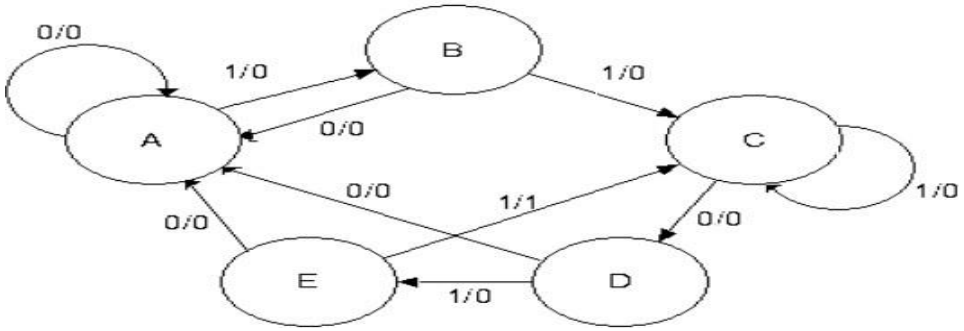
The sequence is 1 1 0 1 1.

Step 1d – Insert the Inputs That Break the Sequence

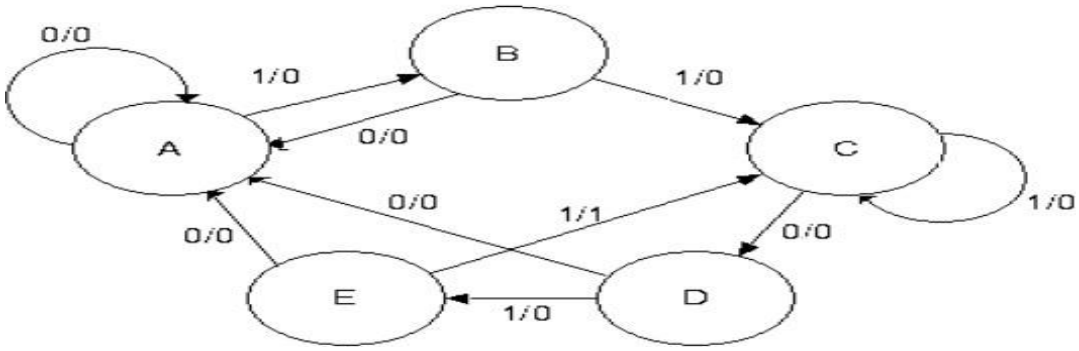
The sequence is 1 1 0 1 1.



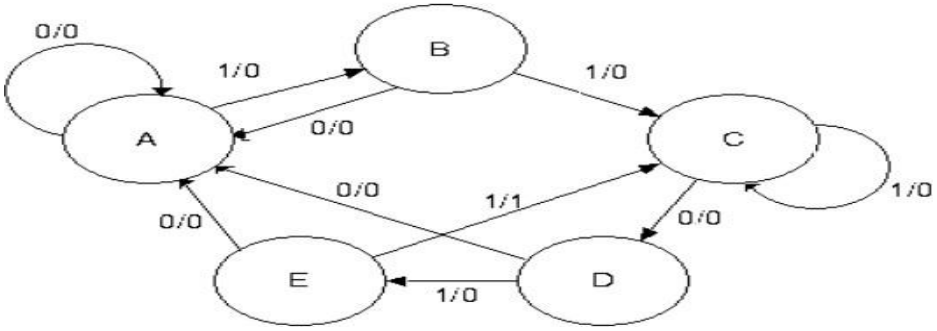
State A in the 11011 Sequence Detector



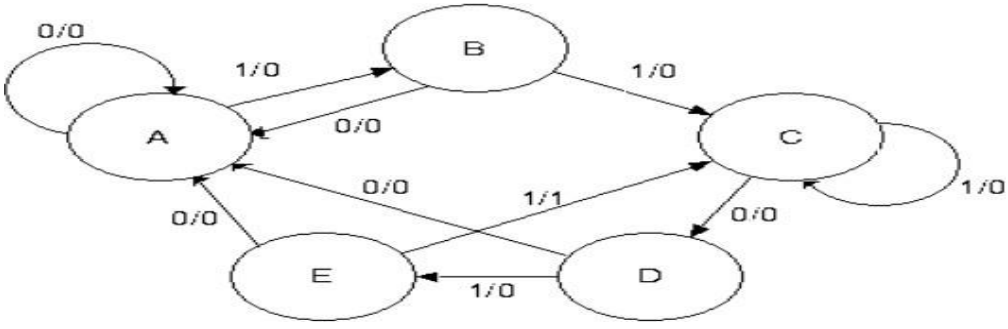
State B in the 11011 Sequence Detector



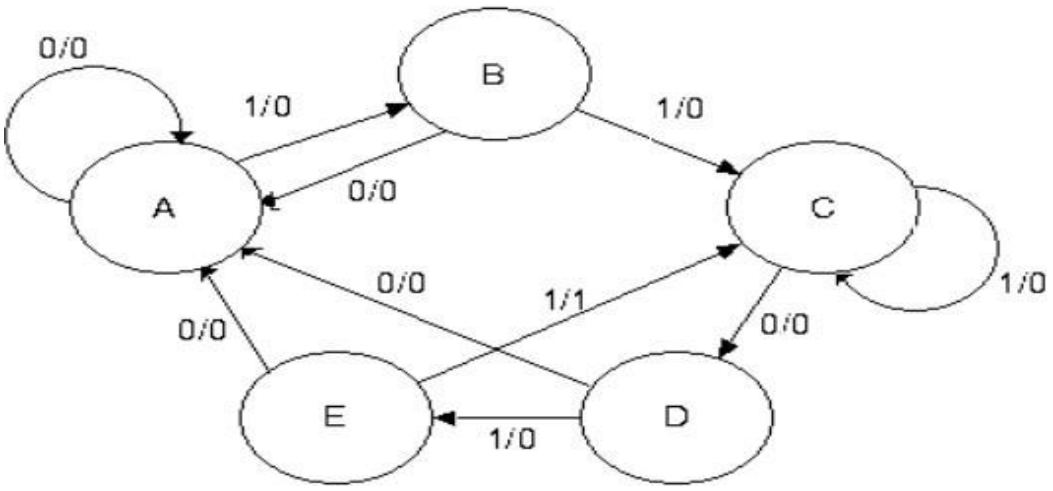
State C in the 11011 Sequence Detector

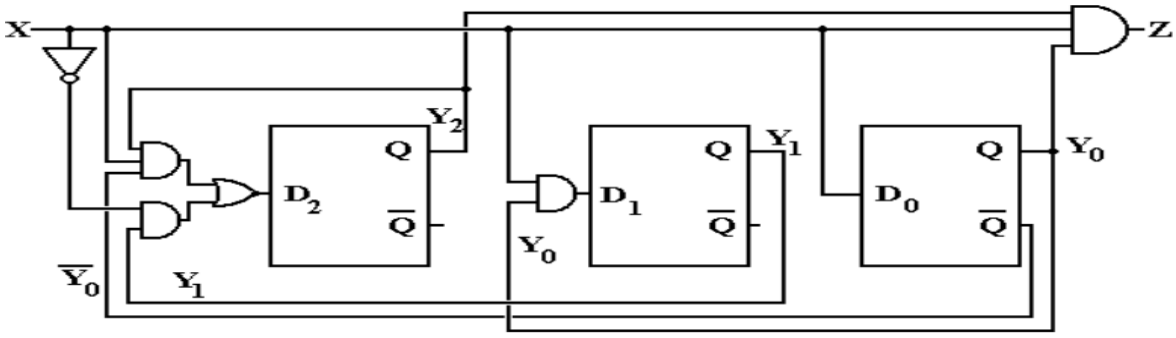


State D in the 11011 Sequence Detector



State E in the 11011 Sequence Detector





(b)Design an even parity generator, that generates an even parity bit for every input string of 3- bits. (15)

An even parity bit generator generates an output of 0 if the number of 1's in the input sequence is even and 1 if the number of 1's in the input sequence is odd. The checker circuit gives an output of 0 if there is no error in the parity bit generated. Thus it basically checks to see if the parity bit generator is error free or not.

Truth table:

	Message	Even parity bit	Checker bit
X Y Z		P	C
0 0 0	0	0	
0 0 1	1	0	
0 1 0	1	0	
0 1 1	0	0	
1 0 0	1	0	
1 0 1	0	0	
1 1 0	0	0	

1 1 1 1 0

X,Y \ Z	0	1
00		1
01	1	
11		1
10	1	

$$P = \overline{X}\overline{Y}Z + \overline{X}Y\overline{Z} + XYZ + X\overline{Y}\overline{Z} = X \oplus Y \oplus Z$$

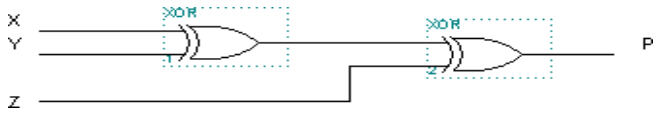


Figure 1: Parity bit generator

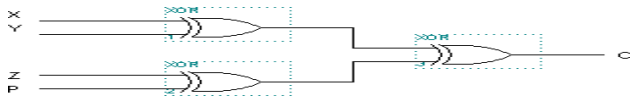


Figure 2: Checker circuit

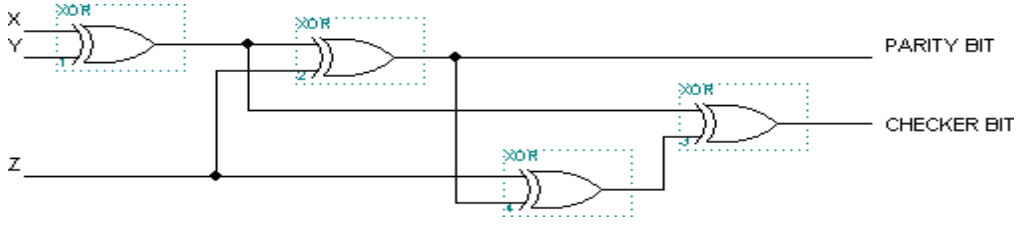


Figure 3: Combined schematic of both parity bit generator and checker circuit