JEPPIAAR
ENGINEERING COLLEGE

DEPARTMENT OF ELECTRONICS AND COMMUNICATION ENGINEERING

CEC370 – LOW POWER IC DESIGN

(Regulation 2021)

QUESTION BANK

Batch: (2022 – 2026)

Year/ Semester: III/VI

JEPPIAAR ENGINEERING COLLEGE		
Vision of the Institute	To build Jeppiaar Engineering College as an institution of academic excellence in technological and management education to become a world class University	
Mission of the Institute	**M1**	To excel in teaching and learning, research and innovation by promoting the principles of scientific analysis and creative thinking
	M2	To participate in the production, development and dissemination of knowledge and interact with national and international communities.
	M3	To equip students with values, ethics and life skills needed to enrich their lives and enable them to meaningfully contribute to the progress of society
	M4	To prepare students for higher studies and lifelong learning, enrich them with the practical and entrepreneurial skills necessary to excel as future professionals and contribute to Nation's economy
DEPARTMENT: ELECTRONICS AND COMMUNICATION ENGINEERING		
Vision of the Department	To become a centre of excellence to provide quality education and produce creative engineers in the field of Electronics and Communication Engineering to excel at international level.	
Mission of the Department	**M1**	Inculcate creative thinking and zeal for research to excel in teaching-learning process
	M2	Create and disseminate technical knowledge in collaboration with industries
	M3	Provide ethical and value based education by promoting activities for the betterment of the society
	M4	Encourage higher studies, employability skills, entrepreneurship and research to produce efficient professionals thereby adding value to the nation's economy

PROGRAM OUTCOMES (PO)	**PO 1**	**Engineering knowledge**: **Apply** the knowledge of mathematics, science, engineering fundamentals, and an engineering specialization to the solution of complex engineering problems.
	PO 2	**Problem analysis**: **Identify, formulate, review** research literature, and **analyze** complex engineering problems reaching substantiated conclusions using first principles of mathematics, natural sciences, and engineering sciences.
	PO 3	**Design/development of solutions**: **Design solutions** for complex engineering problems and **design** system components or processes that meet the specified needs with appropriate consideration for the public health and safety, and the cultural, societal, and environmental considerations
	PO 4	**Conduct investigations of complex problems**: **Use** research-based knowledge and research methods including **design** of experiments, **analysis** and **interpretation** of data, and **synthesis** of the information to provide valid conclusions.
	PO 5	**Modern tool usage**: **Create**, **select**, and **apply** appropriate techniques, resources, and modern engineering and IT tools including prediction and modeling to complex engineering activities with an understanding of the limitations.
	PO 6	**The engineer and society**: **Apply** reasoning informed by the contextual knowledge to assess societal, health, safety, legal and cultural issues and the consequent responsibilities relevant to the professional engineering practice.
	PO 7	**Environment and sustainability**: **Understand** the impact of the professional engineering solutions in societal and environmental contexts, and **demonstrate** the knowledge of, and need for sustainable development.
	PO 8	**Ethics**: **Apply** ethical principles and commit to professional ethics and responsibilities and norms of the engineering practice.
	PO 9	**Individual and team work**: **Function effectively** as an individual, and as a member or leader in diverse teams, and in multidisciplinary settings.
	PO 10	**Communication**: **Communicate effectively** on complex engineering activities with the engineering community and with society at large, such as, being able **to comprehend** and **write** effective reports and **design** documentation, **make** effective presentations, and **give** and **receive** clear instructions.

	PO 11	**Project management and finance**: **Demonstrate** knowledge and understanding of the engineering and management principles and **apply** these to one's own work, as a member and leader in a team, to **manage** projects and in multidisciplinary environments.
	PO 12	**Life-long learning**: **Recognize** the need for, and have the preparation and ability to **engage** in independent and life-long learning in the broadest context of technological change.
PROGRAM EDUCATIONAL OBJECTIVES (PEOS)	**PEO I**	Produce technically competent graduates with a solid foundation in the field of Electronics and Communication Engineering with the ability to analyze, design, develop, and implement electronic systems.
	PEO II	Motivate the students for choosing the successful career choices in both public and private sectors by imparting professional development activities.
	PEO III	Inculcate the ethical values, effective communication skills and develop the ability to integrate engineering skills to broader social needs to the students.
	PEO IV	Impart professional competence, desire for lifelong learning and leadership skills in the field of Electronics and Communication Engineering.
PROGRAM SPECIFIC OUTCOMES (PSOs)	**PSO 1**	Design, develop and analyze electronic systems through application of relevant electronics, mathematics and engineering principles.
	PSO 2	Design, develop and analyze communication systems through application of fundamentals from communication principles, signal processing, and RF System Design & Electromagnetics.
	PSO 3	Adapt to emerging electronics and communication technologies and develop innovative solutions for existing and newer problems.

PROGRAM EDUCATIONAL OBJECTIVES (PEOS)	PEO I	To provide the students with a strong foundation in the required sciences in order to pursue studies in Electronics and Communication Engineering.
	PEO II	To gain adequate knowledge to become good professional in electronic and communication engineering associated industries, higher education and research.
	PEO III	To develop attitude in lifelong learning, applying and adapting new ideas and technologies as their field evolves.
	PEO IV	To prepare students to critically analyze existing literature in an area of specialization and ethically develop innovative and research oriented methodologies to solve the problems identified.
	PEO V	To inculcate in the students a professional and ethical attitude and an ability to visualize the engineering issues in a broader social context.
PROGRAM SPECIFIC OUTCOMES (PSOs)	PSO 1	Design, develop and analyze electronic systems through application of relevant electronics, mathematics and engineering principles.
	PSO 2	Design, develop and analyze communication systems through application of fundamentals from communication principles, signal processing, and RF System Design & Electromagnetics.
	PSO 3	Adapt to emerging electronics and communication technologies and develop innovative solutions for existing and newer problems.

CEC370	LOW POWER IC DESIGN	L T P C 2 0 2 3

COURSE OBJECTIVES:

- To learn the fundamentals of low power low voltage VLSI design.
- To understand the impact of power on system performances.
- To understand the different design approaches.
- To develop the low power low voltage memories

UNIT I FUNDAMENTALS OF LOW POWER CIRCUITS 6

Need for Low Power Circuit Design, Sources of Power Dissipation – Switching Power Dissipation, Short Circuit Power Dissipation, Leakage Power Dissipation, Glitching Power Dissipation, Short Channel Effects –Drain Induced Barrier Lowering and Punch Through, Surface Scattering, Velocity Saturation, Impact Ionization, Hot Electron Effect.

UNIT II LOW-POWER DESIGN APPROACHES 6

Low-Power Design through Voltage Scaling: VTCMOS circuits, MTCMOS circuits, Architectural Level Approach –Pipelining and Parallel Processing Approaches. Switched Capacitance Minimization Approaches: System Level Measures, Circuit Level Measures, Mask level Measures.

UNIT III LOW-VOLTAGE LOW-POWER ADDERS 6

Introduction, Standard Adder Cells, CMOS Adder's Architectures – Ripple Carry Adders, Carry Look-Ahead Adders, Carry Select Adders, Carry Save Adders, LowVoltage Low Power Design Techniques –Trends of Technology and Power Supply Voltage, LowVoltage Low-Power Logic Styles.

UNIT IV LOW-VOLTAGE LOW-POWER MULTIPLIERS 6

Introduction, Overview of Multiplication, Types of Multiplier Architectures, Braun Multiplier, Baugh-Wooley Multiplier, Booth Multiplier, Introduction to Wallace Tree Multiplier

UNIT V LOW-VOLTAGE LOW-POWER MEMORIES 6

Basics of ROM, Low-Power ROM Technology, Future Trend and Development of ROMs, Basics of SRAM, Memory Cell, Precharge and Equalization Circuit, LowPower SRAM Technologies, Basics of DRAM, Self-Refres Circuit, Future Trend and Development of DRAM.

30 PERIODS

PRACTICAL EXERCISES: 30 PERIODS

1. Modeling and sources of power consumption
2. Power estimation at different design levels (mainly circuit, transistor, and gate)
3. Power optimization for combinational circuits
4. Power optimization for sequential circuits
5. Power optimization for RT and algorithmic levels.

TOTAL:60 PERIODS

COURSE OUTCOMES:

Upon successful completion of the course the student will be able to

CO1: Understand the fundamentals of Low power circuit design.

CO2: Attain the knowledge of architectural approaches.

CO3: Analyze and design Low-Voltage Low-Power combinational circuits.

CO4: Learn the design of Low-Voltage Low-Power Memories

CO5: Design and develop Low Power, Low Voltage Circuits

UNIT-1 Fundamentals of Low Power VLSI Design

Need for Low Power Circuit Design, Sources of Power Dissipation – Switching Power Dissipation, Short Circuit Power Dissipation, Leakage Power Dissipation, Glitching Power Dissipation, Short Channel Effects –Drain Induced Barrier Lowering and Punch Through, Surface Scattering, Velocity Saturation, Impact Ionization, Hot Electron Effect.

1. What is the importance of low power circuit design? (BTL-1: Remembering, PO1) CO312.1

Answer:
Low power circuit design is essential to minimize power consumption in electronic devices, extend battery life in portable applications, reduce heat dissipation, and enhance device reliability. It is particularly critical for mobile and embedded systems.

2. **Define switching power dissipation. (BTL-1: Remembering, PO1)** CO312.1

Answer:
Switching power dissipation occurs due to the charging and discharging of load capacitances in CMOS circuits. It is given by:

Pswitching=αCLVdd2fP_{switching} = α C_L V_{dd}^2 fPswitching=αCLVdd2f

where α is the activity factor, C_L is the load capacitance, V_{dd} is the supply voltage, and f is the frequency.

3. **Explain the effect of short-circuit power dissipation. (BTL-2: Understanding, PO2) CO312.1**

Answer:
Short-circuit power dissipation occurs when both NMOS and PMOS transistors are momentarily ON during switching, creating a direct path between supply and ground. This leads to unnecessary power loss and affects circuit efficiency.

4. **List the sources of leakage power dissipation. (BTL-1: Remembering, PO1) CO312.1**

Answer:
The major sources of leakage power dissipation include:

- Subthreshold Leakage – Due to weak inversion in MOS transistors.
- Gate Leakage – Due to tunneling current through thin gate oxide.
- Reverse Bias Junction Leakage – Due to leakage at drain-bulk and source-bulk junctions.

5. **Describe glitching power dissipation. (BTL-2: Understanding, PO2, PO3) CO312.1**

Answer:
Glitching power dissipation arises due to unnecessary transitions in logic circuits caused by different path delays. These unwanted transitions consume extra power and reduce efficiency.

6. **What are the major short-channel effects in MOSFETs? (BTL-1: Remembering, PO1) CO312.1**

Answer:

- Drain-Induced Barrier Lowering (DIBL)
- Punch Through
- Velocity Saturation
- Surface Scattering
- Impact Ionization
- Hot Electron Effect

7. **Explain Drain Induced Barrier Lowering (DIBL). (BTL-2: Understanding, PO1, PO2) CO312.1**

Answer:
DIBL occurs when a high drain voltage lowers the threshold voltage of a MOSFET, causing increased leakage currents and degraded performance.

8. **How does Punch Through affect MOSFET performance? (BTL-2: Understanding, PO2) CO312.1**

Answer:
Punch Through occurs when the depletion regions of source and drain extend into the channel, reducing gate control and increasing leakage current.

9. **Discuss the significance of velocity saturation in short-channel devices. (BTL-3: Applying, PO2, PO4) CO312.1**

Answer:
Velocity saturation limits carrier speed at high electric fields, reducing current drive and affecting MOSFET performance in deep submicron technologies.

10. **How does surface scattering influence carrier mobility? (BTL-2: Understanding, PO2) CO312.1**

Answer:
Surface scattering occurs when carriers interact with surface roughness at the silicon-oxide interface, leading to reduced carrier mobility and degraded performance.

11. **Compare different types of power dissipation in CMOS circuits. (BTL-4: Analyzing, PO2, PO3) CO312.1**

Answer:

Type	Cause	Mitigation Techniques
Switching Power	Charging and discharging of capacitance	Reduce voltage, optimize switching activity
Short-Circuit Power	Both transistors conducting simultaneously	Reduce transition time
Leakage Power	Subthreshold conduction, gate leakage	Use high-threshold transistors

Type	Cause	Mitigation Techniques
Glitching Power	Unnecessary transitions	Reduce delay mismatches

12. **How does leakage power dissipation impact energy efficiency? (BTL-4: Analyzing, PO2, PO7) CO312.1**

Answer:
Leakage power is a major concern in deep submicron technology. It causes continuous power loss even in standby mode, significantly reducing energy efficiency in battery-powered devices.

13. **Analyze the role of impact ionization in device degradation. (BTL-4: Analyzing, PO2, PO6) CO312.1**

Answer:
Impact ionization occurs when high-energy carriers generate additional electron-hole pairs, leading to device degradation through increased leakage currents and reliability issues.

14. **Evaluate the effects of hot electron injection on long-term device reliability. (BTL-5: Evaluating, PO2, PO7) CO312.1**

Answer:
Hot electron injection degrades MOSFETs by trapping charge in the gate oxide, leading to threshold voltage shifts and long-term reliability concerns.

1**5. Propose techniques to minimize switching power dissipation in digital circuits. (BTL-6: Creating, PO3, PO7) CO312.1**

Answer:

- Reduce supply voltage (V_dd)
- Use clock gating to disable inactive sections
- Optimize circuit design to reduce switching activity
- Use low-power logic families

16. Suggest methods to reduce short-circuit power dissipation in VLSI circuits. (BTL-6: Creating, PO3, PO6) CO312.1

Answer:

- Reduce transition time
- Use pass-transistor logic
- Implement differential signaling

17. Develop a low-power design strategy for mobile devices. (BTL-6: Creating, PO3, PO7, PO12) CO312.1

Answer:

- Optimize voltage scaling
- Use energy-efficient memory architectures
- Implement dynamic power management

18. Justify the importance of leakage power reduction techniques in modern VLSI design. (BTL-5: Evaluating, PO7) CO312.1

Answer:
Leakage power accounts for a significant portion of power dissipation in nanometer-scale CMOS circuits. Techniques such as high-k dielectrics and multi-threshold transistors help mitigate leakage, improving energy efficiency.

19. Design a power-efficient logic gate circuit considering all power dissipation factors. (BTL-6: Creating, PO3, PO4) CO312.1

Answer:

- Use logic styles like adiabatic logic
- Optimize transistor sizing
- Implement sleep transistors for power gating

20. Assess the impact of short-channel effects on transistor scaling. (BTL-5: Evaluating, PO2, PO6) CO312.1

Answer:
As transistor dimensions shrink, short-channel effects degrade performance by increasing leakage, reducing drive current, and impacting threshold voltage stability.

PART-B

1.Explain the need for low power circuit design. Discuss various techniques to achieve low power consumption BTL 2 . PO1, PO3, PO7 CO312.1

2. Describe the different types of power dissipation in CMOS circuits. Explain their impact on circuit performance.? BTL 4 ,PO1, PO2, PO3 CO312.1

3. Explain switching power dissipation in detail and suggest methods to minimize it in VLSI circuits. ?BTL PO1, PO3, PO7 CO312.1

4. Discuss short-circuit power dissipation and explain how it affects the overall power consumption of a digital circuit. ?BTL 3 (Applying) PO2, PO3 CO312.1

5. Analyze leakage power dissipation and describe techniques to control it in modern semiconductor devices. BTL Level: 5 (Evaluating)Program Outcome PO1, PO2, PO7 CO312.1

6. What is glitching power dissipation? Explain how it occurs and propose strategies to reduce it. BTL 4 (Analyzing) Program Outcome PO1, PO2, PO3 CO312.1

7. Explain in detail the short-channel effects in MOSFETs, including DIBL, Punch Through, and Surface Scattering. BTL Level: 2 (Understanding) PO1, PO2 CO312.1

8. Discuss the impact of velocity saturation, impact ionization, and hot electron effect on MOSFETs. BTL Level: 4 (Analyzing) Program Outcome Level: PO2, PO4 CO312.1

9. Evaluate the challenges and solutions for power-efficient circuit design in deep submicron technology.?BTL Level: 5 (Evaluating) PO3, PO7, PO12 CO312.

10. Design a low-power VLSI system considering all aspects of power dissipation and transistor behavior. ?BTL Level: 6 (Creating) Program Outcome Level: PO3, PO6, PO7 CO312.1

UNIT II LOW-POWER DESIGN APPROACHES

SYLLABUS:

Low-Power Design through Voltage Scaling: VTCMOS circuits, MTCMOS circuits, Architectural Level Approach –Pipelining and Parallel Processing Approaches. Switched Capacitance Minimization Approaches: System Level Measures, Circuit Level Measures, Mask level Measures.

1. **What is low-power design in VLSI?** BTL 1 (Remembering) PO2 PO3 CO 312.2
   Low-power design in VLSI refers to techniques that reduce power consumption in digital circuits. This is critical for battery-operated devices, energy efficiency, and heat management.
2. **What is the primary goal of voltage scaling?** BTL2 PO2 PO3 CO 312.2
   Voltage scaling reduces power consumption by lowering supply voltage, which significantly decreases dynamic and leakage power in circuits.
3. **How does VTCMOS reduce power consumption?** BTL2 PO2 PO3 CO 312.2
   VTCMOS dynamically adjusts the threshold voltage of transistors, allowing low-voltage operation during active states while reducing leakage current in standby mode.
4. **What is the advantage of MTCMOS circuits?** BTL2 PO2 PO3 CO 312.2
   MTCMOS circuits use high-threshold transistors to cut off power to idle blocks, reducing leakage power while maintaining high-speed operation with low-threshold transistors.
5. **How does pipelining help in low-power design?** BTL2 PO2 PO3 CO 312.2
   Pipelining divides a task into multiple stages, allowing lower clock speeds while maintaining throughput, reducing overall power consumption.
6. **Explain parallel processing in low-power design.** BTL2 PO2 PO3 CO 312.2
   Parallel processing distributes tasks across multiple units, enabling reduced operating frequency and voltage, which minimizes power usage.
7. **What is switched capacitance in CMOS circuits**? BTL2 PO2 PO3 CO 312.2
   Switched capacitance refers to the charge and discharge of capacitance in a circuit during switching, which contributes to dynamic power consumption.

8. **How does clock gating reduce power?** BTL2 PO2 PO3 CO 312.2
   Clock gating disables the clock signal to inactive circuit sections, preventing unnecessary switching and reducing dynamic power consumption.
9. **What is operand isolation?** BTL2 PO2 PO3 CO 312.2
   Operand isolation prevents unnecessary signal transitions by ensuring computations occur only when required, reducing switching activity.
10. **How does data encoding help in power reduction?** BTL2 PO2 PO3 CO 312.2
    Data encoding techniques like bus-invert encoding reduce the number of bit transitions, thereby lowering dynamic power consumption.
11. **What is dynamic voltage scaling** (DVS)? BTL2 PO2 PO3 CO 312.2
    DVS dynamically adjusts the supply voltage based on workload demands to optimize power efficiency without compromising performance.
12. **What is the main drawback of aggressive voltage scaling**? BTL2 PO2 PO3 CO 312.2
    Aggressive voltage scaling can degrade circuit performance and increase delay, impacting timing constraints.
13. **What is transistor sizing in low-power design**? BTL2 PO2 PO3 CO 312.2
    Transistor sizing optimizes the width of transistors to balance speed and power consumption efficiently.
14. **Why is interconnect optimization important for low-power VLSI**? BTL2 PO2 PO3 CO 312.2
    Optimizing interconnects reduces capacitance and resistance, minimizing signal delay and power dissipation.
15. **What is leakage power?** BTL2 PO2 PO3 CO 312.2
    Leakage power is the power lost due to subthreshold conduction and gate leakage, which is significant in deep submicron technologies.
16. W**hat are the types of power dissipation in CMOS circuits?** BTL2 PO2 PO3 CO 312.2
    CMOS circuits experience dynamic power dissipation (due to switching) and static power dissipation (due to leakage currents).
17. **How does adaptive body biasing help in low-power design?** BTL2 PO2 PO3 CO 312.2
    Adaptive body biasing dynamically adjusts transistor body voltage to optimize leakage and performance trade-offs.
18. **What is the role of supply voltage in power dissipation?** BTL2 PO2 PO3 CO 312.2
    Power dissipation is proportional to the square of the supply voltage, making voltage scaling a powerful technique for power reduction.
19. **How does reducing threshold voltage affect power?** BTL2 PO2 PO3 CO 312.2
    Lowering the threshold voltage increases leakage current but improves switching speed, requiring a balance for optimal power efficiency.
20. **What is the difference between active and leakage power?** BTL2 PO2 PO3 CO 312.2
    Active power occurs during circuit operation, while leakage power is consumed even when the circuit is idle.
21. **Why is layout optimization important in power-efficient design?** BTL2 PO2 PO3 CO 312.2
    Proper layout reduces interconnect capacitance, wire length, and parasitics, improving power efficiency.
22. **What is the benefit of using multi-Vt design in VLSI?** BTL2 PO2 PO3 CO 312.2
    Multi-Vt design strategically places transistors with different threshold voltages to balance power and performance.

23. **What is power gating?** BTL2 PO2 PO3 CO 312.2
    Power gating turns off power to inactive circuit sections using high-threshold transistors, reducing leakage power.
24. **How does energy-delay product (EDP) relate to low-power design?** BTL2 PO2 PO3 CO 312.2
    EDP considers both power consumption and performance, helping designers optimize circuits for energy efficiency.
25. **What is a sleep transistor?** BTL2 PO2 PO3 CO 312.2

    A sleep transistor is a high-threshold transistor used in power gating to cut off power supply during idle states.

26. **How do mask-level techniques reduce power?** BTL2 PO2 PO3 CO 312.2
    Mask-level techniques optimize layout design to minimize capacitance and resistance, reducing power loss.
27. **What is the difference between static and dynamic power reduction techniques?** BTL2 PO2 PO3 CO 312.2
    Static techniques reduce leakage power, while dynamic techniques minimize switching activity to lower power consumption.
28. **How does frequency scaling impact power?** BTL2 PO2 PO3 CO 312.2
    Lowering clock frequency reduces dynamic power but may affect performance, requiring workload-based optimization.
29. **What is the role of clock distribution in low-power VLSI?** BTL2 PO2 PO3 CO 312.2
    Efficient clock distribution reduces power wasted in unnecessary toggling, minimizing dynamic power consumption.
30. **What is the significance of the Bloom's Taxonomy Level in learning outcomes?** BTL2 PO2 PO3 CO 312.2
    Bloom's Taxonomy classifies learning objectives from basic recall to advanced analysis and synthesis, ensuring structured learning.

PART-B

1. **Explain the various low-power design methodologies used in VLSI circuits. BTL2 PO2 PO3 CO 312.2**
2. **Discuss the importance of power dissipation in VLSI design and explain different sources of power dissipation. BTL4 PO2 PO3 CO 312.2**
3. **Describe the circuit-level techniques used for low-power design in digital circuits. Provide examples. BTL4 PO2 PO3 CO 312.2**
4. **Explain the architectural-level power optimization techniques and their impact on power consumption. BTL4 PO2 PO5 CO 312.2**
5. **Compare and contrast static and dynamic power dissipation in CMOS circuits. Provide mathematical models. BTL 4PO2 PO4 CO 312.2**
6. **Discuss the impact of supply voltage scaling on power consumption and performance in VLSI circuits. BTL5 PO2 PO3 CO 312.2**
7. **Explain the concept of clock gating and its role in power reduction. How is it implemented in modern processors? BTL4 PO2 PO5 CO 312.2**

8. **Describe the significance of multi-threshold CMOS (MTCMOS) technology in low-power design. BTL2 PO2 PO3 CO 312.2**
9. **Analyze the power gating technique and compare it with clock gating for power optimization. BTL4 PO4 PO5 CO 312.2.**
10. **Explain the role of adaptive voltage scaling (AVS) and dynamic voltage and frequency scaling (DVFS) in energy-efficient design. BTL3 PO4 PO5 CO 312.2**
11. **Explain the concept of voltage scaling and its impact on power consumption in VLSI circuits. Discuss VTCMOS and MTCMOS techniques. BTL 5 (Evaluating) PO 2, PO 4**
12. **Describe** pipelining and parallel processing techniques **for low-power design. How do they improve performance and reduce power? BTL3 PO4 PO5 CO 312.**

Unit III

Introduction, Standard Adder Cells, CMOS Adder's Architectures – Ripple Carry Adders, Carry Look-Ahead Adders, Carry Select Adders, Carry Save Adders, LowVoltage Low Power Design Techniques –Trends of Technology and Power Supply Voltage, LowVoltage Low-Power Logic Styles.

PART- A

1. **Define low-power design.** PO1 Remember (BTL 1) CO 312.3

Low-power design refers to techniques and methodologies used in electronic circuits, especially in VLSI (Very Large Scale Integration), to minimize power consumption while maintaining performance, reliability, and efficiency.

2. **What are the key challenges in low-power VLSI design?** PO1 Remember (BTL 1) CO 312.3
Power dissipation (static & dynamic)

- Performance vs. power trade-off
- Process variations in manufacturing
- Technology scaling limitations
- Leakage currents in deep submicron technologies

3**. List the different sources of power dissipation in VLSI circuits.** PO1 Remember (BTL 1) CO 312.3

- Dynamic power dissipation (due to switching activity)
- Short-circuit power dissipation (during transitions)
- Static power dissipation (leakage currents)

4. **What is dynamic power dissipation?** PO1 Remember (BTL 1) CO 312.3

Dynamic power dissipation occurs when transistors switch between logic states (0 and 1). It is given by:

Pdynamic=αCV2fP_{dynamic} = α C V^2 fPdynamic=αCV2f

where α = switching activity, C = capacitance, V = supply voltage, and f = frequency.

5.What is leakage power? How does it impact circuit performance? **PO1 Remember (BTL 1) CO 312.3**

Leakage power is the unwanted power dissipation due to subthreshold leakage current when the transistor is OFF. It leads to higher standby power consumption and reduced battery life.

6. **Differentiate between static and dynamic power dissipation.** PO1 Remember (BTL 1**CO 312.3**

Static Power Dissipation	Dynamic Power Dissipation
Occurs even when the circuit is idle	Happens due to switching activity
Due to leakage currents	Due to charging/discharging of capacitance
Dominates in deep submicron technologies	Dominant in high-speed circuits

7. **What is an adder cell?** PO1 Remember (BTL 1) CO 312.3

An adder cell is a basic digital circuit used to perform binary addition in arithmetic units, such as ALUs and DSPs.

8. **What are the different types of adders?** PO1 Remember (BTL 1) CO 312.3
Ripple Carry Adder (RCA)

- Carry Look-Ahead Adder (CLA)
- Carry Select Adder (CSA)
- Carry Save Adder (CSA)

9**. Compare ripple carry adder and carry look-ahead adder.** PO1 Remember (BTL 1) CO 312.3

Ripple Carry Adder (RCA)	Carry Look-Ahead Adder (CLA)
Slow due to carry propagation	Faster using parallel carry computation
Simple design	More complex hardware
Power-efficient	Consumes more power

10. Define carry select adder. PO1 Remember (BTL 1) CO 312.3

A carry select adder (CSA) speeds up addition by precomputing results for both carry-in = 0 and carry-in = 1, then selecting the correct result.

11. What is the principle of a carry save adder? PO1 Remember (BTL 1) CO 312.3

A carry save adder (CSA) is used to add multiple binary numbers without immediately propagating the carry, improving speed in multiplication circuits.

12. Why is the ripple carry adder slow? PO1 Remember (BTL 1) CO 312.3

The carry output of each full adder depends on the previous carry, creating a sequential delay known as carry propagation delay.

13. Explain the advantage of a carry look-ahead adder. PO1 Remember (BTL 1) CO 312.3

A carry look-ahead adder (CLA) reduces propagation delay by computing carries in parallel, making it faster than a ripple carry adder.

14. What are the advantages of low-power design? PO1 Remember (BTL 1) CO 312.3

- Longer battery life (for portable devices)
- Less heat dissipation (reducing cooling costs)
- Lower energy consumption (environmental benefits)

15. What is clock gating? How does it help in power reduction? PO1 Remember (BTL 1) CO 312.3

Clock gating is a technique where clock signals are disabled for inactive circuits, reducing dynamic power consumption.

16. Define dynamic voltage scaling. PO1 Remember (BTL 1) CO 312.3

Dynamic Voltage Scaling (DVS) is a technique that adjusts the supply voltage based on the required performance, reducing power consumption.

17. What is power gating? PO1 Remember (BTL 1) CO 312.3

Power gating turns off entire blocks of a circuit when not in use, reducing static power dissipation.

18. What is the effect of reducing supply voltage on power consumption? PO1 Remember (BTL 1) CO 312.3

Reducing supply voltage reduces dynamic power as power is proportional to V^2, but it also increases delay, affecting performance.

19. What are the different low-voltage low-power design techniques? PO1 Remember (BTL 1) CO 312.3

- Voltage scaling
- Clock gating
- Power gating
- Multi-threshold CMOS (MTCMOS)

2**0. Define multi-threshold CMOS (MTCMOS).** PO1 Remember (BTL 1) CO 312.3

MTCMOS uses transistors with different threshold voltages to optimize speed and power efficiency.

21. What is body biasing in low-power design? PO1 Remember (BTL 1) CO 312.3

Body biasing alters the threshold voltage (Vt) dynamically to reduce leakage current.

22. Explain dual-threshold voltage design. PO1 Remember (BTL 1) CO 312.3

This technique assigns low Vt transistors to critical paths for speed and high Vt transistors to non-critical paths for power savings.

23. What are the limitations of low-power design techniques? PO1 Remember (BTL 1) CO 312.3

- Increased design complexity
- Higher manufacturing costs
- Performance trade-offs

24. What is adaptive voltage scaling (AVS)? PO1 Remember (BTL 1) CO 312.3

Adaptive Voltage Scaling (AVS) dynamically adjusts both voltage and frequency based on workload demands to minimize power.

25. What is the significance of low-power logic styles? PO1 Remember (BTL 1) CO 312.3

Low-power logic styles, such as Pass Transistor Logic (PTL) and Dynamic Logic, help reduce switching power and leakage power.

26. Define subthreshold leakage current. PO1 Remember (BTL 1) CO 312.3

Subthreshold leakage current is the tiny current that flows through a transistor even when it is OFF, leading to static power loss.

27. What is the effect of process variation on low-power design? PO1 Remember (BTL 1) CO 312.3

Process variation can cause threshold voltage mismatches, leading to higher leakage and timing failures in circuits.

28. Define energy-delay product (EDP). PO1 Remember (BTL 1) CO 312.3

EDP is a performance metric that evaluates the trade-off between energy consumption and delay:

EDP=Energy×DelayEDP = Energy \times DelayEDP=Energy×Delay

29. What is the impact of technology scaling on power consumption? PO1 Remember (BTL 1) CO 312.3

Technology scaling reduces transistor size, leading to:

- Lower dynamic power (due to lower capacitance)
- Higher leakage current (due to reduced threshold voltage)

30. Explain the concept of low-power energy-efficient circuits. PO1 Remember (BTL 1) CO 312.3

Low-power energy-efficient circuits use techniques like voltage scaling, clock gating, power gating, and multi-threshold design to minimize power consumption without sacrificing performance.

PART-B

1.Explain the different types of adder circuits in detail. Compare their advantages and disadvantages. PO1, PO3 Analyze (BTL 4), Evaluate (BTL 5)

2 Discuss the design and working principle of a ripple carry adder. Analyze its delay and power consumption. PO1, PO2 Apply (BTL 3), Analyze (BTL 4)

3 Explain the concept of a carry look-ahead adder and its significance in reducing propagation delay. PO1, PO3 Apply (BTL 3), Analyze (BTL 4)

4 Compare the carry select adder and carry save adder in terms of performance and power consumption. PO1, PO3 Analyze (BTL 4), Evaluate (BTL 5)

5 Discuss various low-voltage low-power logic styles and their impact on power consumption. PO1, PO2 Understand (BTL 2), Analyze (BTL 4)

6 Explain different low-power design techniques at circuit and system levels. Provide suitable examples. PO1, PO3 Apply (BTL 3), Analyze (BTL 4)

7 How does technology scaling affect power dissipation? Discuss its impact on VLSI circuits. PO1, PO2 Analyze (BTL 4), Evaluate (BTL 5)

8 Explain the role of power supply voltage scaling in low-power VLSI design. Compare different scaling techniques. PO1, PO4 Analyze (BTL 4), Evaluate (BTL 5)

9 Discuss power optimization techniques such as clock gating, power gating, and adaptive voltage scaling. PO1, PO3 Apply (BTL 3), Analyze (BTL 4)

10 Describe the design considerations for energy-efficient adders in low-power VLSI systems. PO1, PO3 Analyze (BTL 4), Evaluate (BTL 5)

UNIT IV LOW-VOLTAGE LOW-POWER MULTIPLIERS

Introduction, Overview of Multiplication, Types of Multiplier Architectures, Braun Multiplier, Baugh-Wooley Multiplier, Booth Multiplier, Introduction to Wallace Tree Multiplier

1. **Define multiplication in digital circuits. BTL 1 (Remember), PO1, CO312.4**

Multiplication in digital circuits refers to the repeated addition of a binary number, implemented using shift-and-add or specialized multipliers.

2. **What are the key challenges in designing multipliers? BTL 2 (Understand), PO1, PO2, CO312.4**

- Speed vs. area trade-offs
- Power consumption
- Complexity of partial product generation and reduction

3. **List different types of multiplier architectures. BTL 1 (Remember), PO1, CO312.4**

- Array Multiplier
- Booth Multiplier
- Wallace Tree Multiplier
- Baugh-Wooley Multiplier
-

4. **What is an array multiplier? BTL 1 (Remember), PO1, CO312.4**

An array multiplier is a combinational circuit that performs bitwise multiplication using a structured array of adders.

5. **What is a Braun multiplier? BTL 1 (Remember), PO1, CO312.4**

A Braun multiplier is a parallel array multiplier using carry-save adders, suitable for unsigned binary multiplication.

6. What are the limitations of a Braun multiplier? BTL 2 (Understand), PO1, PO2, CO312.4

- Only for unsigned multiplication
- Requires many adders
- Slow due to carry propagation

7**. What is a Booth multiplier? BTL 2 (Understand), PO1, CO312.4**

A Booth multiplier uses Booth's algorithm to reduce the number of partial products, improving efficiency in signed multiplication.

8. What is Booth's algorithm? BTL 2 (Understand), PO1, CO312.4

Booth's algorithm is an efficient multiplication technique that recodes operands to reduce the number of shifts and adds.

9. What are the advantages of Booth multiplication? BTL 2 (Understand), PO1, PO2, CO312.4

- Handles signed numbers efficiently
- Fewer additions compared to array multipliers
- Better performance for large numbers

10. Define a Baugh-Wooley multiplier. BTL 1 (Remember), PO1, CO312.4

A Baugh-Wooley multiplier is an optimized signed multiplication technique that simplifies two's complement operations.

11. What are the advantages of Baugh-Wooley multiplication? BTL 2 (Understand), PO1, PO2, CO312.4

- Simplifies signed multiplication
- Optimized for hardware implementation
- Reduces additional bit extension overhead

12. Compare Booth and Baugh-Wooley multipliers. BTL 2 (Understand), PO1, PO2, CO312.4

Booth Multiplier	Baugh-Wooley Multiplier
Uses recoding technique	Uses direct partial product summation
Good for variable-length operands	Optimized for fixed-width multiplication
Efficient for signed numbers	Simplifies two's complement multiplication

Booth Multiplier Baugh-Wooley Multiplier

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13. What is the Wallace Tree multiplier? BTL 1 (Remember), PO1, CO312.4

A Wallace Tree multiplier uses a fast parallel reduction method to sum partial products with minimal delay.

14. What are the benefits of a Wallace Tree multiplier? BTL 2 (Understand), PO1, PO2, CO312.4

- Fast computation due to parallel reduction
- Fewer carry propagation delays
- Efficient hardware implementation

15. How does a Wallace Tree multiplier differ from an array multiplier? BTL 2 (Understand), PO1, CO312.4

A Wallace Tree multiplier reduces partial products in parallel, while an array multiplier propagates carries sequentially, making Wallace Tree faster.

16. What are the three stages of Wallace Tree multiplication? BTL 2 (Understand), PO1, PO2, CO312.4

1. Partial product generation
2. Reduction using carry-save adders
3. Final addition using a fast adder

17. Wat is partial product reduction in multipliers? BTL 2 (Understand), PO1, CO312.4

A process that combines multiple intermediate sums into a final product using adders.

18. What is the importance of carry-save adders in multipliers? BTL 2 (Understand), PO1, PO3, CO312.4

They allow multiple partial sums to be added without waiting for carry propagation, speeding up computation.

19. Define radix-4 Booth encoding.

A technique that reduces the number of partial products by encoding two bits at a time instead of one.
BTL 1 (Remember), PO1, CO312.4

20. How does Booth encoding improve multiplication speed? BTL 2 (Understand), PO1, PO2, CO312.4

Reduces the number of operations

- Handles negative numbers efficiently
- Optimized for large multiplier

21. What is signed multiplication? BTL 1 (Remember), PO1, CO312.4

A multiplication technique that correctly processes negative numbers using two's complement representation.

22. What is unsigned multiplication? BTL 1 (Remember), PO1, CO312.4

Multiplication where both operands are treated as positive binary numbers.

23. What is a combinational multiplier? BTL 1 (Remember), PO1, CO312.4

A multiplier that uses only logic gates (no sequential elements) to compute the result in a single clock cycle.

24. What is a sequential multiplier? BTL 2 (Understand), PO1, CO312.4

A multiplier that generates the product over multiple clock cycles, reducing hardware complexity

25. What is power-delay product (PDP) in multipliers? BTL 2 (Understand), PO1, PO3, CO312.4

A metric that evaluates energy efficiency, given by:

PDP=Power×DelayPDP = Power \times DelayPDP=Power×Delay

26. How does low-power design impact multiplier performance? BTL 2 (Understand), PO1, PO3, CO312.4

- Reduces heat dissipation
- Extends battery life in embedded systems
- Improves circuit reliability

27. What is the impact of technology scaling on multipliers? BTL 2 (Understand), PO1, PO3, CO312.4

- Increases speed due to smaller transistors
- Higher leakage power due to lower threshold voltages
- More efficient parallelism

28. What is a high-speed multiplier? BTL 1 (Remember), PO1, CO312.4

A low-latency multiplier that uses techniques like Wallace Trees or Booth encoding to improve performance.

29. What is a pipelined multiplier? BTL 2 (Understand), PO1, PO3, CO312.4

A multiplier that stages operations across multiple clock cycles to increase throughput.

30. Why are multipliers critical in digital systems? BTL 2 (Understand), PO1, PO2, CO312.4

- Used in DSPs, image processing, and cryptography
- Speed-critical component in CPUs
- Optimized designs improve power efficiency

PART-B

1**. Explain different types of multipliers and compare their performance.**
BTL 4 (Analyze), PO1, PO2, CO312.4

2. Describe the working of a Braun multiplier with a neat diagram.
BTL 3 (Apply), PO1, PO3, CO312.4

3. Explain Booth's multiplication algorithm with an example.
BTL 4 (Analyze), PO1, PO2, CO312.4

4.Discuss the working of Baugh-Wooley multiplier and compare it with Booth multiplier.
BTL 4 (Analyze), PO1, PO2, CO312.4

5. Explain Wallace Tree multiplier with a neat diagram. How does it improve performance?
BTL 5 (Evaluate), PO1, PO3, CO312.4

6. Compare Array, Booth, Wallace Tree, and Baugh-Wooley multipliers in terms of delay, power, and area.
BTL 5 (Evaluate), PO1, PO2, CO312.4

7. What are the challenges in designing low-power multipliers? Explain power reduction techniques in multipliers..
BTL 6 (Create), PO1, PO3, CO312.4

8. Explain the importance of signed and unsigned multiplication in digital circuits. Illustrate with examples.BTL 3 (Apply), PO1, PO2, CO312.4

9. Explain the role of pipelining in high-speed multipliers. How does it improve efficiency?.
BTL 5 (Evaluate), PO1, PO3, CO312.4

10. Discuss the impact of technology scaling on multipliers. How do advanced CMOS techniques help in optimization? BTL 6 (Create), PO1, PO2, CO312.4

UNIT V LOW-VOLTAGE LOW-POWER MEMORIES

Basics of ROM, Low-Power ROM Technology, Future Trend and Development of ROMs, Basics of SRAM, Memory Cell, Precharge and Equalization Circuit, LowPower SRAM Technologies, Basics of DRAM, Self-Refresh Circuit, Future Trend and Development of DRAM.

PART-A

1. **Define Read-Only Memory (ROM). BTL 1 (Remember), PO1, CO312.5**

   ROM is a type of non-volatile memory that stores data permanently and does not require power to retain its contents.

2. **What are the different types of ROM? BTL 1 (Remember), PO1, CO312.5**
   a. The different types of ROM are:
   b. Mask ROM
   c. Programmable ROM (PROM)
   d. Erasable Programmable ROM (EPROM)
   e. Electrically Erasable Programmable ROM (EEPROM)
   f. Flash Memory
3. **What are the advantages of ROM over RAM? BTL 2 (Understand), PO1, PO2, CO312.5**

   ROM is non-volatile, meaning it retains data even when power is turned off. It is more reliable for storing firmware and system boot instructions.

4. **What is mask-programmed ROM? BTL 1 (Remember), PO1, CO312.5**
   a. Mask ROM is a type of ROM where data is permanently written during the manufacturing process and cannot be altered.
5. **Define EEPROM. BTL 1 (Remember), PO1, CO312.5**
   i. EEPROM (Electrically Erasable Programmable Read-Only Memory) is a ROM type that allows data to be erased and reprogrammed electronically.
6. **What is Flash memory?BTL 2 (Understand), PO1, PO2, CO312.5**

a. Flash memory is a non-volatile storage technology that allows data to be erased and rewritten in blocks rather than bytes, making it faster than EEPROM.

7. Explain low-power ROM techniques. BTL 2 (Understand), PO1, PO2, CO312.5

Techniques include:

a. Using low-leakage transistors
b. Optimized circuit design
c. Efficient memory organization to minimize power dissipation

8. How is power consumption reduced in ROM? BTL 2 (Understand), PO1, PO3, CO312.5

Techniques such as clock gating, voltage scaling, and optimizing read operations help reduce ROM power consumption.

9. What are the future trends in ROM technology? BTL 2 (Understand), PO1, PO2, CO312.5

Future trends include resistive RAM (ReRAM), phase-change memory (PCM), and MRAM for faster and low-power applications.

10. Define Static RAM (SRAM)? BTL 1 (Remember), PO1, CO312.5

.SRAM is a type of volatile memory that retains data as long as power is supplied and does not require periodic refreshing.

11. What is the difference between SRAM and DRAM? BTL 2 (Understand), PO1, PO2, CO312.5

SRAM: Faster, no need for refreshing, used in cache memory.

DRAM: Slower, requires periodic refresh, used for main memory.

12. What are the key components of an SRAM cell? BTL 1 (Remember), PO1, CO312.5

An SRAM cell consists of six transistors (6T) arranged as two cross-coupled inverters and two access transistors.

13. What is the function of a precharge circuit in SRAM? BTL 2 (Understand), PO1, PO2, CO312.5

It ensures that the bit-lines are precharged before the read operation to improve speed and stability.

14.**Define equalization in SRAM. BTL 1 (Remember), PO1, CO312.5**

Equalization ensures that both bit-lines of an SRAM cell start at the same voltage before reading to reduce read errors.

15.**What are the low-power design techniques for SRAM? BTL 2 (Understand), PO1, CO 312.5**

Techniques include reducing supply voltage, power gating, and using multi-threshold transistors.

16.**Define Dynamic RAM (DRAM). BTL 1 (Remember), PO1, CO312.**

DRAM is a volatile memory where data is stored in capacitors and requires periodic refreshing to retain information.

17. What are the advantages of DRAM over SRAM? BTL 2 (Understand), PO1, PO2, CO312.5

DRAM is cheaper, has higher density, and consumes less area per bit compared to SRAM.

18. What is the role of the refresh circuit in DRAM? BTL 2 (Understand), PO1, PO2, CO312.5

The refresh circuit periodically reads and rewrites the stored data to prevent data loss due to charge leakage.

19.**Explain the concept of self-refresh in DRAM. BTL 2 (Understand), PO1, PO3, CO312.5**

Self-refresh allows DRAM to refresh itself in low-power mode without CPU intervention, improving power efficiency.

20.**What are the main sources of power consumption in DRAM? BTL 2 (Understand), PO1, PO2, CO312.5**

Major sources include capacitor leakage, refresh operations, and read/write switching power.

PART-B

1. **Explain the different types of ROM and their applications in modern VLSI design. BTL: 4 PO: 1, 2 CO 312.5**
2. **Describe the architecture and working of Flash memory. How does it compare to EEPROM?BTL: 4 (Analyze)PO: 1, 2 CO 312.5**
3. **Discuss the various low-power design techniques used in ROM. BTL: 5 (Evaluate) PO: 1, 3 CO 312.5**
4. **Explain the structure, working, and advantages of a 6T SRAM cell. ?BTL: 4 (Analyze) PO: 1, 2 CO 312.5**
5. **Compare and contrast SRAM and DRAM in terms of speed, power consumption, and design complexity. BTL: 5 (Evaluate) PO: 1, 2 CO 312.5**
6. **Describe the self-refresh mechanism in DRAM. How does it contribute to power reduction? BTL: 4 (Analyze) PO: 1, 3 CO 312.5**
7. **Discuss the impact of technology scaling on SRAM and DRAM performance and power consumption. BTL: 5 (Evaluate) PO: 1, 2 CO 312.5**
8. **Explain the role of precharge and equalization circuits in SRAM. Why are they important for memory performance? BTL: 4 (Analyze) PO: 1, 2 CO 312.5**
9. **What are the future trends in memory technology, including MRAM, ReRAM, and PCM? BTL: 6 (Create) PO: 1, 3 CO 312.5**
10. **Describe the concept of 3D-stacked DRAM and its advantages over traditional memory architectures. BTL: 4 (Analyze) PO: 1, 2 CO 312.**