

JEPPIAAR ENGINEERING COLLEGE
DEPARTMENT OF ELECTRICAL AND ELECTRONICS ENGINEERING

VISION OF INSTITUTION

To build Jeppiaar Engineering College as an institution of academic excellence in technology and management education, leading to become a world class University.

MISSION OF INSTITUTION

- To excel in teaching and **learning, research and innovation** by promoting the principles of scientific analysis and creative thinking.
- To participate in the production, **development, dissemination of knowledge** and interact with **national and international communities**.
- To equip students with ethical **values, and life skills** that would enrich their lives and enable them to meaningfully contribute to the **progress of the society**.
- To prepare students for **higher studies and lifelong learning**, enrich them with the **practical and entrepreneurial skills** necessary to excel as future professionals and contribute to **Nation's economy**.

PROGRAM OUTCOMES (POs)

- 1 Engineering knowledge:** Apply the knowledge of mathematics, science, engineering fundamentals, and an engineering specialization to the solution of complex engineering problems.
- 2 Problem analysis:** Identify, formulate, review research literature, and analyze complex engineering problems reaching substantiated conclusions using first principles of mathematics, natural sciences, and engineering sciences.
- 3 Design/development of solutions:** Design solutions for complex engineering problems and design system components or processes that meet the specified needs with appropriate consideration for the public health and safety, and the cultural, societal, and environmental considerations
- 4 Conduct investigations of complex problems:** Use research-based knowledge and research methods including design of experiments, analysis and interpretation of data, and synthesis of the information to provide valid conclusions.
- 5 Modern tool usage:** Create, select, and apply appropriate techniques, resources, and modern engineering and IT tools including prediction and modeling to complex engineering activities with an understanding of the limitations.
- 6 The engineer and society:** Apply reasoning informed by the contextual knowledge to assess societal, health, safety, legal and cultural issues and the consequent responsibilities relevant to the professional engineering practice.
- 7 Environment and sustainability:** Understand the impact of the professional engineering solutions in societal and environmental contexts, and demonstrate the knowledge of, and need for sustainable development.
- 8 Ethics:** Apply ethical principles and commit to professional ethics and responsibilities and norms of the engineering practice.
- 9 Individual and team work:** Function effectively as an individual, and as a member or leader in diverse teams, and in multidisciplinary settings.
- 10 Communication:** Communicate effectively on complex engineering activities with the engineering community and with society at large, such as, being able to comprehend and write effective reports and design documentation, make effective presentations, and give and receive clear instructions.
- 11 Project management and finance:** Demonstrate knowledge and understanding of the engineering and management principles and apply these to one's own work, as a member and leader in a team, to manage projects and in multidisciplinary environments.

- 12 Life-long learning:** Recognize the need for, and have the preparation and ability to engage in independent and life-long learning in the broadest context of technological change.

VISION OF THE DEPARTMENT

The Department of Electrical and Electronics Engineering strives to be a Centre of Excellence in education and technical research, in the endeavour of which the Department will continually update the teaching methodologies, progress in the emerging technologies and continue to play a vital role in the development of the society.

MISSION OF THE DEPARTMENT

M1	To develop the ability to learn and work creatively that would enhance the ability of both students and faculty to do innovative research .
M2	To create and maintain state-of-the art facilities which provide students and faculty with opportunities to analyse, apply and disseminate knowledge globally .
M3	To impart the knowledge in essential interdisciplinary fields which will enhance the interpersonal skills , team work, professional ethics and make them work effectively for their own benefit and the betterment of the society .
M4	Prepare students for lifelong learning of theoretical and practical concepts to face intellectual, economical and career challenges.

PROGRAM EDUCATIONAL OBJECTIVES (PEOs)

PEO 01	Strengthen the knowledge in Electrical and Electronics Engineering to enable them work for modern industries by promoting energy conservation and sustainability.
PEO 02	Enrich analytical, creative and critical logical reasoning skills to solve problems faced by emerging domains of electrical and electronics engineering industries worldwide.
PEO 03	Develop effective communication and inter-personal skills to work with enhanced team spirit in multidisciplinary projects with a broader ethical , professional, economical and social perspective.
PEO 04	Prepare the students either to establish start ups or to pursue higher education at reputed institutions.

PROGRAM SPECIFIC OUTCOME (PSOs)

PSO 1	Professional Skills: Apply the knowledge of Mathematics, Science and Engineering to solve real time problems in the field of Power Electronics, Electrical Drives, Power Systems, Control Systems and Instrumentation .
PSO 2	Research and Innovation: Analyze and synthesize circuits by solving complex engineering problems to obtain the optimal solution using effective software tools and hardware prototypes in the field of robotics and renewable energy systems.
PSO 3	Product development: Develop concepts and products by applying ideas of electrical domain into other diversified engineering domains.

EE8351 DIGITAL LOGIC CIRCUITS

OBJECTIVES:

- To study various number systems and simplify the logical expressions using Boolean functions
- To study combinational circuits
- To design various synchronous and asynchronous circuits.
- To introduce asynchronous sequential circuits and PLDs
- To introduce digital simulation for development of application oriented logic circuits.

UNIT I NUMBER SYSTEMS AND DIGITAL LOGIC FAMILIES 6+6

Review of number systems, binary codes, error detection and correction codes (Parity and Hamming code) - Digital Logic Families -comparison of RTL, DTL, TTL, ECL and MOS families -operation, characteristics of digital logic family.

UNIT II COMBINATIONAL CIRCUITS 6+6

Combinational logic - representation of logic functions-SOP and POS forms, K-map representations - minimization using K maps - simplification and implementation of combinational logic – multiplexers and de multiplexers - code converters, adders, subtractors, Encoders and Decoders.

UNIT III SYNCHRONOUS SEQUENTIAL CIRCUITS 6+6

Sequential logic- SR, JK, D and T flip flops - level triggering and edge triggering - counters - asynchronous and synchronous type - Modulo counters - Shift registers - design of synchronous sequential circuits – Moore and Melay models- Counters, state diagram; state reduction; state assignment.

UNIT IV ASYNCHRONOUS SEQUENTIAL CIRCUITS AND PROGRAMMABILITY LOGIC DEVICES 6+6

Asynchronous sequential logic circuits-Transition tability, flow tability-race conditions, hazards & errors in digital circuits; analysis of asynchronous sequential logic circuits introduction to Programmability Logic Devices: PROM – PLA –PAL, CPLD-FPGA.

UNIT V VHDL 6+6

RTL Design – combinational logic – Sequential circuit – Operators – Introduction to Packages – Subprograms – Test bench. (Simulation /Tutorial Examples: adders, counters, flip flops, Multiplexers & De multiplexers).

TOTAL : 60 PERIODS

TEXT BOOKS:

1. James W. Bignel, Digital Electronics, Cengage learning, 5th Edition, 2007.
2. M. Morris Mano, 'Digital Design with an introduction to the VHDL', Pearson Education, 2013.
3. Comer "Digital Logic & State Machine Design, Oxford, 2012.

REFERENCES

1. Mandal, "Digital Electronics Principles & Application, McGraw Hill Edu, 2013.
2. William Keitz, Digital Electronics-A Practical Approach with VHDL, Pearson, 2013.
3. Thomas L.Floyd, 'Digital Fundamentals', 11th edition, Pearson Education, 2015.
4. Charles H.Roth, Jr, Lizy Lizy Kurian John, 'Digital System Design using VHD, Cengage, 2013.
5. D.P.Kothari,J.S.Dhillon, 'Digital circuits and Design', Pearson Education, 2016.

Course code& Name: **EE8351 & Digital Logic Circuits**

Degree/Programme: **B.E/EEE** Semester: **III**

Section: **A, B**

Duration: **DEC – APRIL 2018**

Regulation: **2017/AUC**

Name of the Staff:

AIM

- To understand and analyse the digital electronic circuits.

OBJECTIVES

- To study various number systems , simplify the logical expressions using Boolean functions
- To study implementation of combinational circuits
- To design various synchronous and asynchronous circuits.
- To introduce asynchronous sequential circuits and PLCs
- To introduce digital simulation for development of application oriented logic circuits

C2 2.1	Recollecting the various number systems and simplifications using mathematical expression and understand the concepts of digital logic families
C2 2.2	Ability to design and implementation of combinational logic circuits
C2 2.3	Ability to design and implementation of combinational logic circuits
C2 2.4	Design of asynchronous sequential circuits and describe the operation of Programmable Logic Devices
C2 2.5	Ability to understand the digital simulation techniques for application oriented logic circuits using VHDL coding.

EE8351	PO1	PO2	PO3	PO4	PO5	PO6	PO7	PO8	PO9	PO10	PO11	PO 12	PSO1	PSO2	PSO3
C2 2.1	3	3	1	1	-	-	-	-	-	2	-	3	3	1	3
C2 2.2	3	3	3	2	-	-	-	-	-	2	-	3	3	1	3
C2 2.3	3	3	3	2	-	-	-	-	-	2	-	3	3	1	3
C2 2.4	3	3	3	1	-	-	-	-	-	2	-	3	3	1	3
C2 2.5	3	2	1	1	3	-	-	-	-	2	-	3	3	1	3

UNIT-I NUMBER SYSTEMS AND DIGITAL LOGIC FAMILIES			Target Period :9			
SI No	Contents	CO Statement	Book Reference & Page No	Delivery method	Delivery Period	Knowledge Level
1	Review of number systems	C2 2.1	T1[11]	Chalk & board / PPT	1	R & U
2	Binary codes, Error detection codes	C2 2.1	R4[62,75]	Chalk & board / PPT	1	R & U
3	Error correction codes (Parity and Hamming code)	C2 2.1	R4[79]	Chalk & board / PPT	1	R, U, A
4	Digital Logic Families: RTL-operation	C2 2.1	T1[131] R9[7.2]	Chalk & board / PPT	1	R, U
5	DTL, ECL -operation	C2 2.1	T1[134] R9[7.28]	Chalk & board / PPT	1	R, U
6	TTL -operation	C2 2.1	T1[136] R9[7.6]	Chalk & board / PPT	1	R,U
7	MOS families -operation	C2 2.1	T1[147] R9[7.19]	Chalk & board / PPT	1	R,U
8	Comparison of RTL, DTL, TTL, ECL and MOS families, characteristics of digital logic family	C2 2.1	T1[151] R9[7.31] R9[7.2]	Chalk & board / PPT	2	R,U
UNIT II COMBINATIONAL CIRCUITS			Target Periods:9			
SI No	Contents	CO Statement	Book Reference & Page No	Delivery method	Delivery Hrs	Knowledge Level
1	Combinational logic circuits	C2 2.2	T1[53] R9[1.2]	Chalk & board / PPT	1	R, U,A
2	Representation of logic functions	C2 2.2	T1[57] R9[1.4]	Chalk & board / PPT	1	R, U, A, An
3	SOP and POS forms	C2 2.2	T1[60,64] R9[1.8]	Chalk & board / PPT	1	R, U, A, An
4	K-map representations	C2 2.2	T1[76] R9[1.18]	Chalk & board / PPT	1	R, U, A, An
5	Minimization using K maps	C2 2.2	T1[78] R9[1.56]	Chalk & board / PPT	1	R, U, A, An
6	Simplification and implementation of combinational logic	C2 2.2	T1[89] R9[1.69]	Chalk & board / PPT	1	R, A, An
7	Multiplexers and demultiplexers	C2 2.2	T1[227] R9[2.40]	Chalk & board / PPT	1	R, U,A,An
8	Code converters	C2 2.2	T1[249] R9[2.19]	Chalk & board / PPT	1	R, U,A,An
9	Adders, subtractors, Encoders, Decoders	C2 2.2	T1[214] R9[2.5]	Chalk & board / PPT	1	R, U,A,An
UNIT III SYNCHRONOUS SEQUENTIAL CIRCUITS			Target Periods: 9			
SI No	Contents	CO Statement	Book Reference & Page No	Delivery method	Delivery Hrs	Knowledge Level
1	Sequential logic- SR, JK flip flops	C2 2.3	T1[312] R9[3.2]	Chalk & board / PPT	1	R, U, A,An

2	D and T flip flops –working Principles, Truth table, Excitation Table	C2 2.3	T1[326] R9[3.9]	Chalk & board / PPT	1	R, U, A, An
3	Level triggering and edge triggering of flip flops	C2 2.3	T1[335] R9[3.3]	Chalk & board / PPT	1	R, U, A
4	Counters - asynchronous type	C2 2.3	T1[390] R9[4.59]	Chalk & board / PPT	1	R, U, A, An
5	Counters - synchronous type	C2 2.3	T1[400] R9[4.44]	Chalk & board / PPT	1	R, U, A, An
6	Modulo counters	C2 2.3	T1[395] R9[4.62]	Chalk & board / PPT	1	R, U, A, An
7	Shift registers	C2 2.3	T1[385]	Chalk & board / PPT	1	R, U, A, An
8	Design of synchronous sequential circuits – Moore and Melay models	C2 2.3	T1[353] R9[4.2]	Chalk & board / PPT	1	R, U, A, An
9	Counters, state diagram; state reduction; state assignment.	C2 2.3	T1[355] R9[4.5]	Chalk & board / PPT	1	R, U, A
UNIT IV Asynchronous Sequential Circuits and Programmable Logic Devices Target Periods:9						
SI No	Contents	CO Statement	Book Reference & Page No	Delivery method	Delivery Hrs	Knowledge Level
1	Asynchronous sequential logic circuits	C2 2.4	T1[442] R9[5.2]	Chalk & board / PPT	1	R, U, A, An
2	Transition table, flow table	C2 2.4	T1[459] R9[5.24]	Chalk & board / PPT	1	R, U, A, An
3	Race conditions	C2 2.4	T1[456] R9[5.30]	Chalk & board / PPT	1	R, U, A, An
4	Hazards in digital circuits	C2 2.4	T1[467] R9[B.2]	Chalk & board / PPT	1	R, U, A, An
5	Errors in digital circuits	C2 2.4	T1[467]	Chalk & board / PPT	1	R, U, A, An
6	Analysis of asynchronous sequential logic circuits	C2 2.4	T1[448] R9[5.4]	Chalk & board / PPT	1	R, U, A, An
7	Introduction to Programmable Logic Devices: PROM	C2 2.4	R4[582] R9[6.5]	Chalk & board / PPT	1	R, U
8	PLA, PAL	C2 2.4	R4[608] R9[6.19]	Chalk & board / PPT	1	R, U
9	CPLD, FPGA	C2 2.4	T1[509] R9[6.33]	Chalk & board / PPT	1	R, U
UNIT V VHDL Target Periods: 9						
SI No	Contents	CO Statement	Book Reference & Page No	Delivery method	Delivery Hrs	Knowledge Level
1	RTL Design	C2 2.5	R5[44] R9[8.106]	Chalk & board / PPT	1	R, U,
2	Combinational logic circuit	C2 2.5	R5[17] R9[8.94]	Chalk & board / PPT	1	R, U
3	Sequential circuit	C2 2.5	R5[47] R9[8.77]	Chalk & board / PPT	1	R, U
4	Operators	C2 2.5	R5[76] R9[8.16]	Chalk & board / PPT	1	R, U

5	Introduction to Packages	C2 2.5	R5[76] R9[8.3]	Chalk & board / PPT	1	R, U
6	Subprograms	C2 2.5	R9[8.69]	Chalk & board / PPT	1	R, U
7	Test bench, Revision	C2 2.5	R9[8.115]	Chalk & board / PPT	1	R, U
8	Simulation /Tutorial Examples: adders	C2 2.5	R9[8.98]	Chalk & board / PPT	1	R, U, A,
9	Simulation /Tutorial Examples: counters	C2 2.5	R9[8.86]	Chalk & board / PPT	1	R, U, A,
10	Simulation /Tutorial Examples: flip-flops	C2 2.5	R5[44] R9[8.106]	Chalk & board / PPT	1	R, U, A,
11	Simulation /Tutorial Examples: FSM	C2 2.5	R9[8.94]	Chalk & board / PPT	1	R, U, A,
12	Simulation /Tutorial Examples: Multiplexers/Demultiplexers	C2 2.5	R5[54]	Chalk & board / PPT	1	R, U, A,

Books: Text (T) / Reference(R):

S.No	Book No	Title of the Book	Author	Publisher	Year
1	T1	Digital Systems – Principles and Design	Raj Kamal	Pearson Edison, 2nd edition	2007
2	T2	Digital Design with an introduction to the VHDL	M. Morris Mano	Pearson Education	2013
3	T3	Digital Logic & State Machine Design,	Comer	Oxford	2012
4	R1	Digital Electronics Principles & Application	Mandal	McGraw Hill Edu	2013
5	R2	Digital Electronics-A Practical Approach with VHDL	William Keitz	Pearson	2013
6	R3	Digital Fundamentals	Floyd and Jain	8th edition, Pearson Education	2003
7	R4	Fundamentals of Digital Circuits	Anand Kumar	PHI	2013
8	R5	Digital System Design using VHDL	Charles H.Roth,Jr,Lizy Lizy Kurian John	Cengage	2013
9	R6	Digital Logic, Application & Design	John M.Yarbrough	Thomson	2002
10	R7	VHDL Basics to Programming	Gaganpreet Kaur	Pearson	2013
11	R8	HDL Programming Fundamental, VHDL& Verilog	Botros	Cengage	2013
12	R9	<i>Digital Logic Circuits</i>	A.P.Godse & D.A.Godse	<i>Technical Publications</i>	2014
13	R10	<i>Digital Circuits and Design</i>	S.Salivahanan & S. Arivazhgan	<i>Vikas Publication 3rd Edition</i>	2008

Comments Given by the Scrutinizing Committee Members	
Signature of the Scrutinizing	
Signature of the HOD	

EE8351 DIGITAL LOGIC CIRCUITS

UNIT – I

NUMBER SYSTEMS AND DIGITAL LOGIC FAMILIES

PART-A

1. What is the different classification of binary codes?

- Weighted codes
- Non - weighted codes
- Reflective codes
- Sequential codes
- Alphanumeric codes
- Error Detecting and correcting codes.

2. What are the needs for binary codes?

- a. Code is used to represent letters, numbers and punctuation marks.
- b. Coding is required for maximum efficiency in single transmission.
- c. Binary codes are the major components in the synthesis (artificial generation) of speech and video signals.
- d. By using error detecting codes, errors generated in signal transmission can be detected.
- e. Codes are used for data compression by which large amounts of data are transmitted in very short duration of time.

3. What are weighed codes? Give examples (NOV/DEC 2012)

The weighed codes are the codes that have assigned weights or values for each bit position. A code in which each bit position has a certain numeric value assigned. Several such codes exist, such as 8-4-2-1, 7-4-2-1, 6-3-1 -1, Excess – 3 code.

4. What are cyclic codes? (APR/MAY 2013)

An (n, k) linear code C is called a cyclic code if any cyclic shift of a codeword is another codeword. That is,

$$\text{if } \bar{c} = (c_0, c_1, \dots, c_{n-1}) \in C$$
$$\text{then } \bar{c}^{(1)} = (c_{n-1}, c_0, c_1, \dots, c_{n-2}) \in C$$

5. What are self complementing codes?

These are the codes whose arithmetic and logic complements are the same.

Example: Excess – 3 code, 2421 code

6. What are BCD codes?

A special binary code used to directly represent the decimal characters. Each four bit value in BCD represents a single decimal character.

7. What are alphanumeric codes?

A binary code used to represent the alphabets, numbers and punctuation marks as well as control characters for controlling a printer or display. Eg – ASCII, EBCD

8. What is an Excess – 3 code?

A self complementing code used to represent BCD numbers. It is self complementing because the 1's complement is also the 9's complement of the BCD number. It is widely used in BCD arithmetic circuits.

Example: 1000 of 8421 = 1011 in Excess-3

9. What is a Gray code? (or) What is a unit distance code? Give an example (NOV/DEC 2015)

A reflective, unit distance code where only one bit position changes for each adjacent change in value.

10. Define radix or base.

The number of characters in the characters set of a positional number system. Decimal numbers have a base of 10, binary numbers have a base of 2. Base and radix are used interchangeably.

11. List the advantages and disadvantages of BCD code?

12. The advantages of BCD code are

- a. Any large decimal number can be easily converted into corresponding binary number
- b. A person needs to remember only the binary equivalents of decimal number from 0 to 9.
- c. Conversion from BCD into decimal is also very easy.

The disadvantages of BCD code are

- a. The code is least efficient. It requires several symbols to represent even small numbers.
- b. Binary addition and subtraction can lead to wrong answer.
- c. Special codes are required for arithmetic operations.
- d. This is not a self-complementing code.
- e. Conversion into other coding schemes requires special methods.

13. What is meant by self-complementing code?

A self-complementing code is the one in which the members of the number system complement on themselves. This requires the following two conditions to be satisfied.

- a. The complement of the number should be obtained from that number by replacing 1s with 0s and 0s with 1s.
- b. The sum of the number and its complement should be equal to decimal 9. Example of a self-complementing code is
 1. 2-4-2-1 code.
 2. Excess-3 code.
 3. BCD code

14. Mention the advantages of ASCII code?

The following are the advantages of ASCII code

- a. There are $2^7 = 128$ possible combinations. Hence, a large number of symbols, alphabets etc., can be easily represented.
- b. There is a definite order in which the alphabets, etc., are assigned to each code word.
- c. The parity bits can be added for error-detection and correction.

15. What are the disadvantages of ASCII code?

The disadvantages of ASCII code are

- a. The length of the code is larger and hence more bandwidth is required for transmission.
- b. With more characters and symbols to represent, this is not completely sufficient.

16. What is a reflective code?

A code is said to be reflective when code for 9 is complement for the code for 0, and so is for 8 and 1 codes, 7 and 2, 6 and 3, 5 and 4. Codes 2421, 5211, gray and excess-3 are reflective, whereas the 8421 code is not.

17. What is sequential code?

A code is said to be sequential when two subsequent codes, seen as numbers in binary representation, differ by one. This greatly aids mathematical manipulation of data. The 8421 and Excess-3 codes are sequential, whereas the 2421 and 5211 codes are not.

18. What is meant by parity bit?

Parity bit is an extra bit included with a binary message to make the number of 1's either odd or even. The message, including the parity bit is transmitted and then checked at the receiving end for errors.

19. What is even and odd parity?

(NOV/DEC 2011)

A parity bit is an extra bit included with a message to make the total number of 1's either even or odd. Consider the following two characters and their even and odd parity:

	With even parity	With odd parity
ASCII A = 1000001	01000001	11000001
ASCII T = 1010100	11010100	01010100

In each case we add an extra bit in the left most position of the code to produce an even number of 1's in the character for even parity or an odd number of 1's in the character for odd parity. The parity bit is helpful in detecting errors during the transmission of information from one location to another.

20. State the associative property of Boolean algebra.

The associative property of Boolean algebra states that the OR ing of several variables results in the same regardless of the grouping of the variables. The associative property is stated as follows: $A + (B + C) = (A + B) + C$

21. State the commutative property of Boolean algebra.

The commutative property states that the order in which the variables are OR ed makes no difference. The commutative property is: $A + B = B + A$

22. State and prove the distributive property of Boolean algebra. (NOV/DEC 2012)

The distributive property states that AND ing several variables and OR ing the result with a single variable is equivalent to OR ing the single variable with each of the several variables and then AND ing the sums. The distributive property is: $A + BC = (A + B)(A + C)$

x	y	z	$y + z$	$x \cdot (y + z)$	$x \cdot y$	$x \cdot z$	$(x \cdot y) + (x \cdot z)$
0	0	0	0	0	0	0	0
0	0	1	1	0	0	0	0
0	1	0	1	0	0	0	0
0	1	1	1	0	0	0	0
1	0	0	0	0	0	0	0
1	0	1	1	1	0	1	1
1	1	0	1	1	1	0	1
1	1	1	1	1	1	1	1

23. Define duality property

Duality property states that every algebraic expression deducible from the postulates of Boolean algebra remains valid if the operators and identity elements are interchanged. If the dual of an algebraic expression is desired, we simply interchange OR and AND operators and replace 1's by 0's and 0's by 1's.

24. State De Morgan's theorem. (NOV/DEC 2010), (APR/MAY 2010), (MAY/JUNE 2014)

De Morgan suggested two theorems that form important part of Boolean algebra.

1) The complement of a product is equal to the sum of the complements.

$$(AB)' = A' + B'$$

2) The complement of a sum term is equal to the product of the complements.

$$(A + B)' = A'B'$$

25. What are called don't care conditions?

In some logic circuits certain input conditions never occur, therefore the corresponding output never appears. In such cases the output level is not defined, it can be either high or low. These output levels are indicated by 'X' or 'd' in the truth tables and are called don't care conditions or incompletely specified functions.

26. Convert the given expression in canonical SOP form $Y = AC + AB + BC$ (NOV/DEC 2015, 2016), (APR/MAY 2016)

$$\begin{aligned}
 Y &= AC + AB + BC \\
 &= AC(B + B') + AB(C + C') + (A + A')BC \\
 &= ABC + ABC' + AB'C + AB'C' + ABC + ABC' + ABC + ABC' \\
 &= ABC + ABC' + AB'C + AB'C'
 \end{aligned}$$

27. Convert the given expression in canonical SOP form $Y = AC + AB + BC$ (NOV/DEC 16)

$$\begin{aligned} &= AC(B + B') + AB(C + C') + (A + A')BC \\ &= ABC + ABC' + AB'C + AB'C' + ABC + ABC' + ABC \\ &= ABC + ABC' + AB'C + AB'C' \end{aligned}$$

28. Simplify $F = ABC + AB'C + A'C + AB'$ (MAY/JUNE 2014)

$$\begin{aligned} F &= ABC + AB'C + A'C + AB' \\ &= AC(B+B') + A'C + AB' \\ &= AC + A'C + AB' \\ &= C + AB' \end{aligned}$$

29. Simplify the expression $Z = AB + AB'(A'C)'$ (MAY/JUNE 2016)

$$\begin{aligned} Z &= AB + AB'(A'C)' \\ &= AB + AB'(A+C) \\ &= AB + AB' + AB'C \\ &= A(B + B' + B'C) \\ &= A(1+B'C) = A \end{aligned}$$

30. Simplify the expression $Z = B' + AB' + A'C'$ (NOV/DCE 2014)

$$\begin{aligned} Z &= B' + AB' + A'C' \\ &= B' + A'C' \end{aligned}$$

31. What are the different classification of binary codes?

- Weighted codes
- Non - weighted codes
- Reflective codes
- Sequential codes
- Alphanumeric codes
- Error Detecting and correcting codes.

32. Define logic gates?

Logic gates are electronic circuits that operate on one or more input signals to produce an output signal. Electrical signals such as voltages or currents exist throughout a digital system in either of two recognizable values. Voltage- operated circuits respond to two separate voltage levels that represent a binary variable equal to logic 1 or logic 0.

33. Why are NAND and NOR gates known as universal gates?

The NAND and NOR gates are known as universal gates, since any logic function can be implemented using NAND or NOR gates.

34. What is a maxterm or POS?

n variables forming an OR term, with each variable being primed or unprimed, provide 2ⁿ possible combinations, called maxterms, or standard sums.

35. What is minterm or SOP?

n variables forming an AND term, with each variable being primed or unprimed, provide 2ⁿ possible combinations, called minterms, or standard products.

36. What is a prime implicant? (APR/MAY 2010), (NOV/DEC 2013)

A prime implicant is a product term obtained by combining the maximum possible number of adjacent squares in the map. If a minterm in a square is covered by only one prime implicant, that prime implicant is said to be essential.

37. What is the value of 'b' if $\sqrt{41_b} = 5$? (MAY/JUNE 2012)

The value of b = 6

38. Convert $(108.2)_{10}$ and $(10110.110)_2$ into hexadecimal numbers. (APR/MAY 2011)

$$\begin{array}{r} 16 \overline{) 108} \\ \underline{6 - 6} \\ 6 \\ \end{array} \quad \begin{array}{l} 0.2 \times 16 = 3.2 \\ 0.2 \times 16 = 3.2 \\ 0.2 \times 16 = 3.2 \end{array}$$

Hence, $(108.2)_{10} = (66.222)_{16}$

$$\frac{00010110.1100}{1 \quad 6 \quad C}$$

Hence, $(10110.110)_2 = (16.C)_{16}$

39. Determine $(377)_{10}$ in octal and hexa decimal equivalent (NOV/DEC 2014)

(i) $(377)_{10} = 571$

(ii) $(377)_{10} = 179$

40. Simplify $X\bar{Y} + ZX\bar{Y}$ (APR/MAY 2011)

$$= X\bar{Y} + ZX\bar{Y}$$

$$= X\bar{Y}[1 + Z] = X\bar{Y}$$

41. Simplify the expression $\overline{ABC} + BC + AC$ (NOV/DEC 2011)

$$= \overline{ABC} + BC + AC$$

$$= [\overline{AB} + B]C + AC$$

$$= [\overline{A} + B]C + AC$$

$$= \overline{A}C + BC + AC$$

$$= [\overline{A} + A]C + BC$$

$$= C + BC = C[1 + B] = C$$

42. What is the decimal equivalent of $(8963)_{16}$? (NOV/DEC 2010)

$$\begin{array}{r} 8 \quad 9 \quad 6 \quad 3 \\ \rightarrow 3 \times 16^0 = 3 \\ \rightarrow 6 \times 16^1 = 96 \\ \rightarrow 9 \times 16^2 = 2304 \\ \rightarrow 8 \times 16^3 = 32768 \\ \hline 35157 \end{array}$$

Hence, $(8963)_{16} = (35157)_{10}$

43. What is the abbreviation of ASCII and EBCDIC code?

- ASCII-American Standard Code for Information Interchange.
- EBCDIC-Extended Binary Coded Decimal Information Code.

44. What are the universal gates?

NAND and NOR

45. What are the different types of number complements?

- i) r's Complement
- ii) (r-1)'s Complement.

46. Express the function $f(x, y, z)=1$ in the sum of minterms and a product of maxterms?

Minterms= $\Sigma(0,1,2,3,4,5,6,7)$

Maxterms=No maxterms.

47. Explain or list out the advantages and disadvantages of K-map method? (MAY /JUNE 2012)

The *advantages* of the K-map method are

- i. It is a fast method for simplifying expression up to four variables.
- ii. It gives a visual method of logic simplification.
- iii. Prime implicants and essential prime implicants are identified fast.
- iv. Suitable for both SOP and POS forms of reduction.
- v. It is more suitable for class room teachings on logic simplification.

The *disadvantages* of the K-map method are

- i. It is not suitable for computer reduction.
- ii. K-maps are not suitable when the number of variables involved exceed four.
- iii. Care must be taken to fill in every cell with the relevant entry, such as a 0, 1 (or) don't care terms

48. What is Hamming code?

(NOV/DEC 2013)

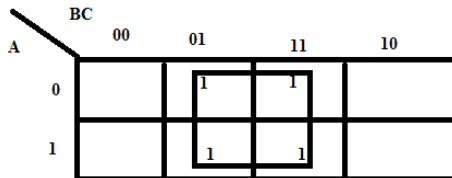
One of the most common error-correcting codes used in random-access memories was devised by R. W. Hamming. In the Hamming code, k parity bits are added to an n -bit data word, forming a new word of $n + k$ bits. The bit positions are numbered in sequence from 1 to $n + k$. Those positions numbered as a power of 2 are reserved for the parity bits. The remaining bits are the data bits. The code can be used with words of any length.

49. State absorption theorem in Boolean algebra.

(NOV/DEC 2010)

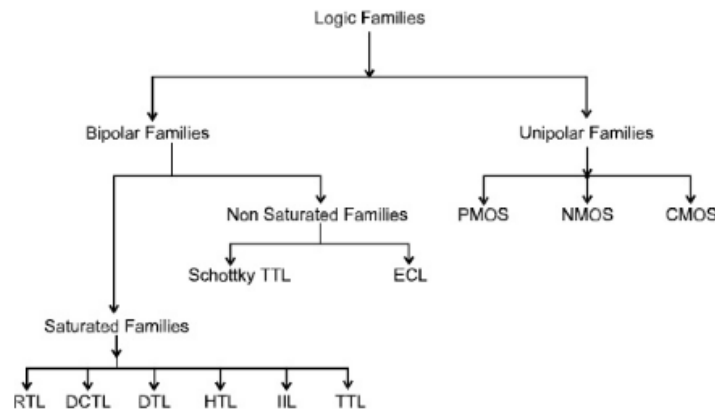
- i. $x + xy = x$
- ii. $x(x+y) = x$

50. Simplify the function $Y = \sum m(1,3,5,7)$ (MAY/JUNE 2013)



$Y = C$

51. What are the various digital logic families available?



52. List the characteristics of digital IC family.

- Fan in
- Fan out
- Power dissipation
- Propagation delay
- Noise margin
- Speed power product

53. What is totem pole configuration?

It is the output stage of a TTL gate. The name totem pole stems from the apparent stacking of one transistor on the top of another.

54. State the advantages and drawbacks of totem pole output. (NOV/DEC 2013)

Advantages:

- External pull up resistor is not required
- Operating speed is very high

Drawbacks:

- Output of two gates cannot be tied together

55. Describe the characteristics of TTL family.

S.No	CHARACTERISTICS	VALUES
1.	Supply voltage	For 74 series - (4.75 to 5.25) units For 54 series - (4.5 to 5.5) units
2.	Temperature range	For 74 series - (0°C to 70°C) For 54 series - (-55°C to 125°C)
3.	Voltage levels	$V_{OL(max)} - 0.4V$

		$V_{OH(min)} - 2.4V$ $V_{IL(max)} - 0.8V$ $V_{IH(min)} - 2.0V$
4.	Noise margin	0.4V
5.	Power dissipation	10 mW per gate
6.	Propagation delay	Typically 10 ns
7.	Fan out	10

56. List the sub families of TTL.

- Standard TTL
- High speed TTL
- Low power TTL
- Schottky TTL
- Low power Schottky TTL
- Advanced Schottky TTL
- Fast TTL
- Advanced Low power Schottky TTL

57. How is the high speed achieved in TTL?

All the resistance values are reduced due to which high switching speed is achieved. Also a Darlington pair is provided which generates a high current gain hence power consumption is reduced.

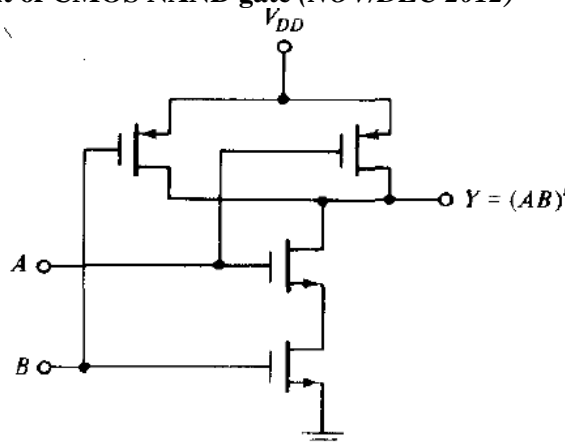
58. Give the comparison between TTL, CMOS and ECL families.

S.no	Parameter	TTL	CMOS	ECL
1.	Propagation delay	10ns	70ns	750ps
2.	Noise margin	0.4V	$0.45V_{DD}$	150mW
3.	Power dissipation	10mW	0.01mW	5mW
4.	Fan out	10	50	25
5.	Figure of merit	100pJ	0.7pJ	0.5pJ

59. Which IC family offers low propagation delay and Low power dissipation?

ECL and CMOS

60. Draw the logic circuit of CMOS NAND gate (NOV/DEC 2012)



61. Define fan out and fan in. (NOV/DEC 2011,2015), (MAY/JUNE 2016)

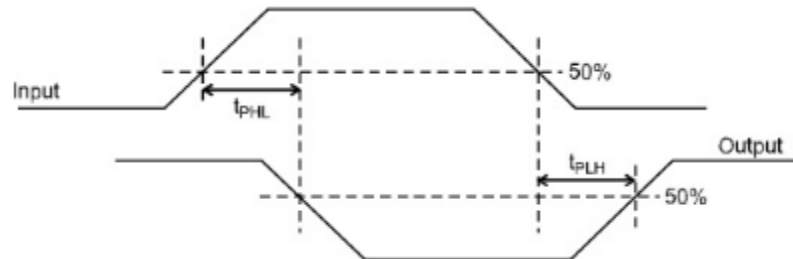
Fan in : Maximum number of inputs that can be connected to a logic gate without any impairment of its normal operation is called as fan – in

Fan – Out : Maximum number of standard loads that output of the gate can be drive without any impairment or degradation of its normal operation

62. Define propagation delay (MAY/JUNE 2014)(APRIL/MAY 2015)

Propagation delay is the average transition delay time for the signal to propagate from input to output when the signals change in value. It is expressed in ns. Propagation Delay is the maximum time taken by output to change its state in response to input. The

propagation delay determines the speed of operation of a gate. In general switching speed is measured when 50% duty cycle time square wave is applied at a input and a square wave is generated at output, The times are measured from 50% of voltage levels. The time t_{PHL} is delay when output goes LOW from HIGH and t_{PLH} is the time delay taken by output to go HIGH from LOW state. The propagation delay t_p is average of the two times and measured in n sec.



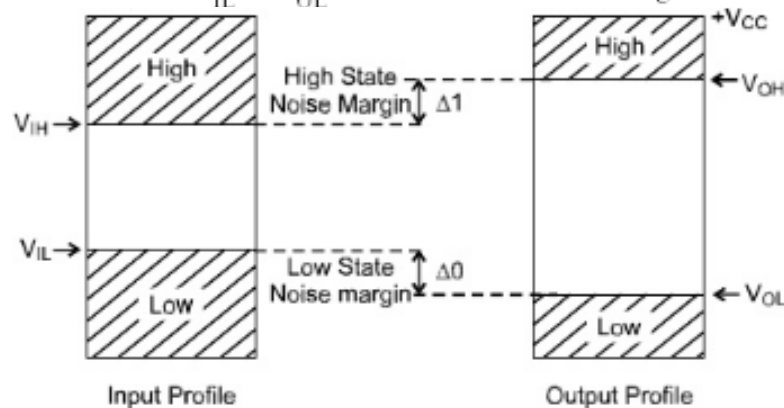
$$t_p = \frac{t_{PHL} + t_{PLH}}{2} = \text{Propagation Delay (n sec)}$$

63. Define noise margin. (MAY/JUNE 2014)

It is the maximum noise voltage added to an input signal of a digital circuit that does not cause an undesirable change in the circuit output. It is expressed in volts. Unwanted electric signals, called noise, can appear when connecting the logic devices. These noise signals can cause the voltage levels to rise or reduce from intended value. This may cause circuit malfunction. For example if noise causes an input voltage to reduce below the V_{IH} , then input is not recognized as logic 1 and thus the circuit malfunctions. The ability of a circuit to tolerate the effect of noise is called as noise immunity. The amount by which a circuit can tolerate the effect of noise is called noise margin.

$$\Delta I = V_{OH} - V_{IH} = \text{High state noise margin}$$

$$\Delta O = V_{IL} - V_{OL} = \text{Low state noise margin}$$



64. What is power dissipation?

Power dissipation is measure of power consumed by the gate when fully driven by all its inputs.

65. What is power dissipation factor?

Power Dissipation (P_D) is defined as the power dissipated in an IC and measured in mW. It is desired to have low power dissipation to reduce cooling, but it may increase the propagation delays.

66. What is speed power product?

Speed power product is defined as the as the product of propagation delay (in nano seconds) and power dissipation (in mW) and is measured in pico joules. It is also referred as the figure of merit of a digital IC

67. Explain the various Input and output Currents

For a high – state gate driving a second gate,

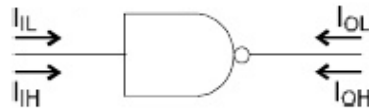
I_{OH} – high level output current, current that flows from an output in the logic – 1 state under specified load conditions

I_{IH} – high level input current, current that flows into an input when a logic – 1 voltage is applied to that input.

For a low state gate driving a second gate,

I_{OL} – Low level output current, current that flows from an output in the logic-0 state under specified load conditions.

I_{IL} – Low level input current, current that flows into an input when a logic – 0 voltage is applied to that input.



68. List the advantages and drawbacks of ECL. (APR/MAY 2010)

Advantages:

1. Current drawn from the supply is steady
2. Switching time is less.

Disadvantages:

1. It is difficult to achieve good noise immunity
2. Power consumption is increased as the transistors are saturated.

88. What factors limit CMOS fan –out?

The CMOS fan out depends on the permissible maximum propagation delay. For low frequencies the fan out is 50Hz, and for high frequencies it will be less.

89. What can happen if TTL output is connected to more unit loads that its output rating specifications? (MAY/JUNE 2012)

If more gate inputs are specified by the fan out are connected to the output of the gate, the gate may not function correctly. Indeed even when the fan out is not exceeded, each additional load at the gate tends to increase the switching time of the gate. For high speed operations manufacturers usually recommend a maximum loading factor which is less than the dc loading capability of the gate. The limits on the fan out of the gate are caused by the currents which flow when the input has to be held at one level usually 0.

90. Give the fan – in, fan – out and noise margin range of a TTL family NAND gate. (APR/MAY 2011)

- Noise margin = 0.4V
- Fan in = 8
- Fan out = 10

91. Compare TTL, ECL, CMOS families for switching speed. (NOV/DEC 2010)

- TTL – Faster than CMOS
- ECL – Fastest of all
- CMOS – Less than TTL

92. What are the uses of a buffer? (MAY/JUNE 2013)

Buffer is used to transfer the output of the input circuit to that of the output circuit

93. State advantages and disadvantages of TTL

Advantages:

- Easily compatible with other ICs
- Low output impedance

Disadvantages:

- Wired output capability is possible only with tristate and open collector types. Special circuits in Circuit layout and system design are required.

94. When does the noise margin allow digital circuits to function properly?

When noise voltages are within the limits of VNA(High State Noise Margin) and VNK for a particular logic family.

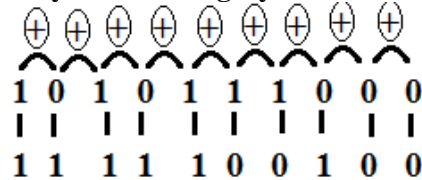
95. What happens to output when a tristate circuit is selected for high impedance.

Output is disconnected from rest of the circuits by internal circuitry.

96. What is 14000 series?

It is the oldest and standard CMOS family. The devices are not pin compatible or electrically compatible with any TTL Series.

97. Convert the following binary code into a gray code 1010111000_2 (MAY/JUNE 2015)



98. Convert (APR/MAY 2016)

a. $(475.25)_8$ to its decimal equivalent – 317.328_{10}

b. $(549.B4)_{16}$ to its binary equivalent – $0101\ 0100\ 1001.\ 1011\ 0100_2$

99. Compare the totempole output and open collector output (NOV/DEC 2014)

S.No	TOTEM POLE	OPEN COLLECTOR
1. 1	Output state consist of pull up transistor, diode resistor and pull down transistor	Output stage consists of only pull down transistor.
2.	External pull-up resistor is not required	External pull-up resistor is required for proper operation of gate.
3.	Output of two gates cannot be tied together.	Output of two gates can be tied together using wired AND technique
4.	Operating speed is high	Operating speed is low.

100. Convert the following Excess – 3 number into decimal numbers (NOV/DEC 2016)

1. 1011 - 8

2. 1001 0011 0111- 604

PART – B

- Convert the following numbers to their decimal equivalents $BC2_{16}$ and $(11011.011)_2$ (APR/MAY 2010), (NOV/DEC 2011), (NOV/DEC 2012), (MAY/JUNE 2013)(NOV/DEC 2013) (MAY/JUNE 2016) (NOV/DEC 2016) (T2– 5-9)
- Binary, BCD, Octal, Hexa decimal, Excess -3 Arithmetic (APR/MAY 2015)(NOV/DEC 2015)
- Prove that $\overline{AB} + \overline{A} + AB = 0$ (NOV/DEC 2010) (T2– 43-44)
- Express function $Y = AB + \overline{BC} + \overline{AC}$ in canonical sum of product form. (NOV/DEC 2011), (NOV/DEC 2012), (MAY/JUNE 2013) (NOV/DEC 2013 (T2– 44- 51)
- Encode the binary word 1011 into seven bit even parity Hamming code (APR/MAY 2010), (NOV/DEC 2012) (NOV/DEC 2013) (NOV/DEC 2014) (NOV/DEC 2015) (MAY/JUNE 2015) (MAY/JUNE 2016) (NOV/DEC 2016) (T 2- 268 - 269)
- Using the NOR outputs of two ECL gates, show that when connected together to an external resistor and negative supply voltage, the wired connection produces an ‘OR’ function (APR/MAY 2011) (MAY/JUNE 2012), (NOV/ DEC 2012), (MAY/JUNE 2013) (NOV/DEC 2013) (MAY/JUNE 2016) (T2– 420-421)
- Write detailed notes on CMOS technology (MAY/JUNE 2012), (NOV/ DEC 2010) (APR/MAY 2010), (NOV/ DEC 2012), (APR/MAY 2011), (NOV/DEC 2015), (NOV/DEC 2016) (NOV/DEC 2014) (T2– 423-427)

8. Explain the working of three input TTL Inverter, NAND totem pole output gate, NOR gates (*APR/MAY 2011*), (*NOV/ DEC 2011*), (*NOV/ DEC 2010*) (*NOV/DEC 2013*)(*NOV/DEC 2014*) (*MAY/JUNE 2015*) (*MAY/JUNE 2016*) (T2– 410 -419)

Unit – II
COMBINATIONAL CIRCUITS

PART – A

1. What are combinational circuits?

A combinational circuit consists of logic gates whose outputs at any time are determined from the present combination of inputs. A combinational circuit performs an operation that can be specified logically by a set of Boolean functions. It consists of input variables, logic gates, and output variables.

2. Give the design procedures for the designing of a combinational circuit.

The procedure involves the following steps,

- From the specification of the circuit, determine the required number of inputs and outputs and assign a symbol to each.
- Derive the truth table that defines the required relationships between inputs and outputs.
- Obtain the simplified Boolean functions for each output as a function of the input variables.
- Draw the logic diagram and verify the correctness of the design.

3. Define half adder.

A combinational circuit that performs the addition of two bits is called a half adder. A half adder needs two binary inputs and two binary outputs. The input variables designate the augend and addend bits; the output variables produce the sum and carry

4. Define full adder

A combinational circuit that performs the addition of three bits is a full adder. It consists of three inputs and two outputs.

5. Define magnitude comparator

A magnitude comparator is a combinational circuit that compares two numbers, A and B, and determines their relative magnitudes. The outcome of the comparison is specified by three binary variables that indicate whether $a > b$, $A = b$, or $A < B$.

6. What are decoders? Give an application. (NOV/DEC 2014)

A decoder is a combinational circuit that converts binary information from n input lines to a maximum of 2^n unique output lines. If the n bit coded information has unused combinations, the decoder may have fewer than 2^n outputs.

The decoders are used in code converters, implementation of combinational circuits, address decoding, BCD to 7-segment decoder.

7. What are encoders?

An encoder is a digital circuit that performs the inverse operation of a decoder. An encoder has 2^n and n output lines. The output lines generate the binary code corresponding to the input value.

8. Define priority encoder

A priority encoder is an encoder circuit that includes the priority function. The operation of priority encoder is such that if two or more inputs are equal to 1 at the same time, the input having the highest priority will take precedence.

9. Define multiplexer. Give an application. (NOV/DEC 2014)

A multiplexer is a combinational circuit that selects binary information from one of many input lines and directs it to a single output line. The selection of a particular input line is controlled by a set of selection lines. Normally there are 2^n input lines and n selection lines whose bit combinations determine which input is selected.

They can be used as a data selector to select one out of many data inputs, to implement combinational logic circuit, in time multiplexing systems, in frequency multiplexing systems, in data acquisition systems

10. What is the function of a multiplexers select inputs?(NOV/DEC 2012)The selection of a particular input line is controlled by a set of selection lines. Normally there are 2^n input lines and n selection lines whose bit combinations determine which input is selected

11. What do you mean by comparator?

A comparator is a special combinational circuit designed primarily to compare the relative magnitude of two binary numbers.

12. What is a look ahead carry adder?

The carry propagation time is a limiting factor on the speed with which two numbers are added in parallel. The most widely used technique employs the principle of *look-ahead* carry adder. Where in the final carry is expressed in terms of the initial carry and is designed such that it does not depend on the intermediate carry values.

13. What is positive logic system? Give an example. (APR/MAY 2011)

When high voltage or more positive voltage level is associated with binary '1' and while the low or less positive level is associated with binary '0' then the system adhering to this is called positive logic.

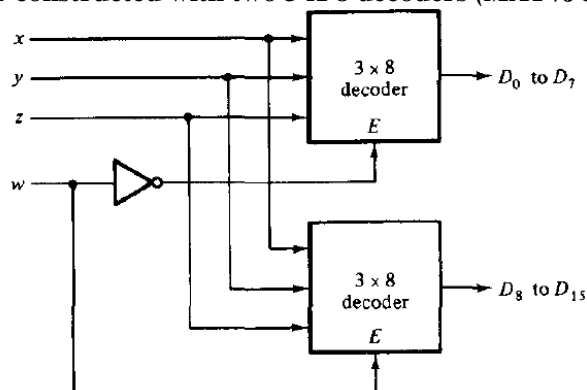
14. Define Negative Logic.

When high voltage level is associated with binary '0' and while the low level is associated with binary '1' then the system adhering to this is called negative logic

15. Give the differences between DMUX and MUX (MAY/JUNE 2012)

S.No	MULTIPLEXER	DEMULTIPLEXER
1.	It has 2^n inputs	it has 1 input
2.	It has 1 output	It has 2^n outputs
3.	It is also called as data selector	It is also called as data distributor
4.	It is used at the input side	It is used at the output side

16. Draw a 4X16 decoder constructed with two 3 X 8 decoders (MAY/JUNE 2012)



17. Give the truth table of EX-OR gate. Give an example for EX-OR gate. (APR/MAY 2011)

TRUTH TABLE :

A	B	$\overline{A}B + A\overline{B}$
0	0	0
0	1	1
1	0	1
1	1	0

18. Write the truth table of universal gates.(NOV/DEC 2011)

NAND GATE

NOR GATE

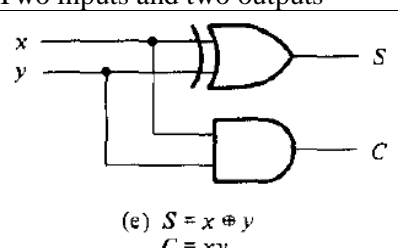
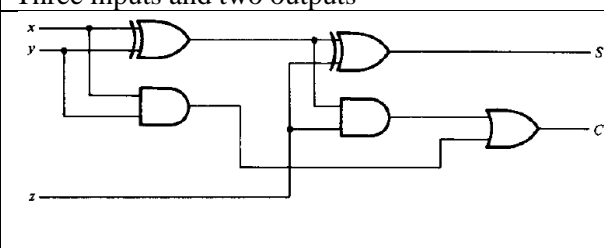
TRUTH TABLE

A	B	$\overline{A+B}$
0	0	1
0	1	1
1	0	1
1	1	0

TRUTH TABLE

A	B	$\overline{A+B}$
0	0	1
0	1	1
1	0	1
1	1	0

19. Compare half adder and full adder. (NOV/DEC 2010)

S.N	HALF ADDER	FULL ADDER
0		
1	Two inputs and two outputs	Three inputs and two outputs
2	 <p>(e) $S = x \oplus y$ $C = xy$</p>	

20. Design a half Subtractor. (APR/MAY 2010), (MAY/JUNE 2014) (MAY/JUNE 2015)

TRUTH TABLE:

A	B	BORROW	DIFFERENCE
0	0	0	0
0	1	1	1
1	0	0	1
1	1	0	0

K-Map for DIFFERENCE:

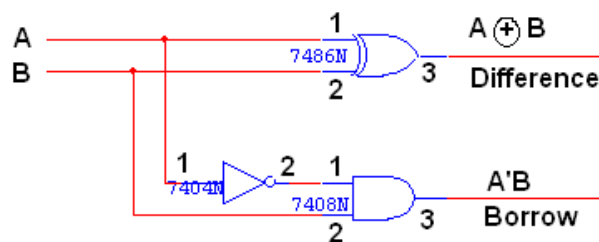
		B	
		00	01
A	00		1
	01	1	

K-Map for BORROW:

		B	
		00	01
A	00		1
	01		

DIFFERENCE = $A'B + AB'$

BORROW = $A'B$



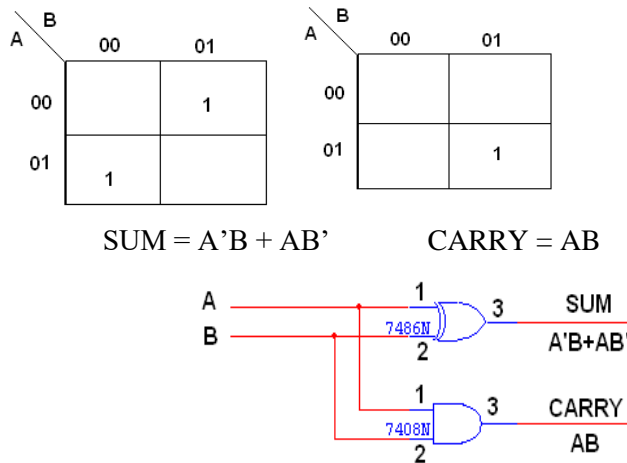
21. Design a half Adder and write its truth table. (MAY/JUNE 2013)

TRUTH TABLE:

A	B	CARRY	SUM
0	0	0	0
0	1	0	1
1	0	0	1
1	1	1	0

K-Map for SUM:

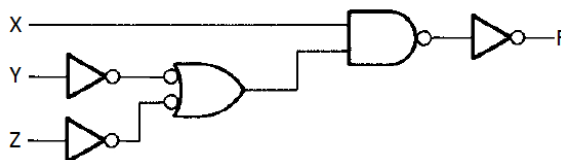
K-Map for CARRY:



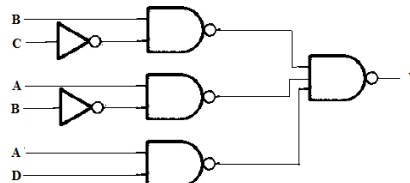
22. Draw the truth table of 2:1 MUX (NOV/DEC 2016)

S	Y
0	A
1	B

23. Implement the following function using only NAND gates $F = (x + y)z$. (APR/MAY 2010)



24. Implement the equation $Y = \overline{BC} + \overline{AB} + AD$ using only NAND gates (MAY/JUNE 2013)



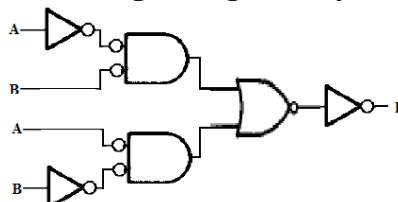
25. What is the use of enable signal? (NOV/DEC 2010)

The enable signal is used as a control signal which can be a active high or a low one depending on the application. When it is active high the circuit gets initiated and the inputs flow into the circuit only when its value is high, else the circuit gets deactivated and no out is produced. The same logic is applicable when it is a active low signal, the circuit gets activated only when it is active low and vice versa

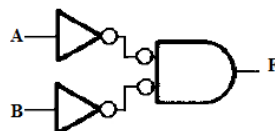
26. Identify the MSI devices 74157 and 74150 (NOV/DEC 2011)

1. 74157 – Quad 2:1 multiplexer
2. 74150 – 8:1 multiplexer

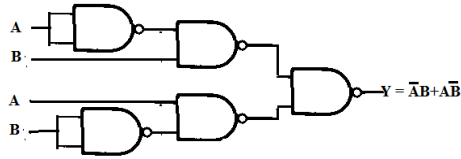
27. Realize the following function using NOR gates only $F = A'B + AB'$ (MAY/JUNE 2014)



28. Implement the function $F = A.B$ using NOR gates (NOV/DEC 2013)



29. Draw the logical diagram of EX-OR gate using NAND gates. (NOV/DEC 2015)

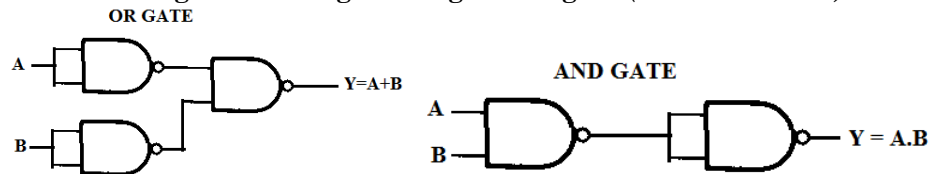


30. Write the POS representation of $f(x,y,z) = \sum m(0,1,3,5,7)$ (MAY/JUNE 2016)

A \ BC	BC			
	00	01	11	10
0	1	1	1	0
1	0	1	1	0

$$F = (B'+C)(A'+C)$$

31. Construct OR gate to AND gate using NAND gate. (NOV/DEC 2016)



32. Show how the JK flip-flop can be modified into a D flip-flop or a T flip-flop (NOV/DEC 2014)

$$J=D, K=D' \qquad J=T, K=T$$

PART – B

- Simplify using K-map $F = \pi M(0,1,3,6,8,9,11,15)$ (APR/MAY 2011) (NOV/DEC 2016) (T2– 76 - 79)
- Simplify the expression $Y = \sum m(3,4,6,7,8,9,10,13,14,15)$ using K-map using logic gates (NOV/DEC 2011), (NOV/DEC 2010) (NOV/DEC 2013) (MAY/JUNE 2014) (NOV/DEC 2016) (NOV/DEC 2015) (NOV/DEC 2016) (T2– 70- 74)
- Obtain the minimum SOP using Quine McClusky's method and verify using K map $F = m_0 + m_2 + m_4 + m_8 + m_9 + m_{10} + m_{11} + m_{12} + m_{13}$ (MAY/JUNE 2012) (T2(2e)(112-120)
- Simplify the following using Quine – McClusky method. Realize the reduced function using NAND gates. $F = \sum m(0,2,3,4,7,8,11,12,13) + \sum d(5,6)$ (APR/MAY 2011), (NOV/DEC 2011), (MAY/JUNE 2013) (NOV/DEC 2013) (MAY/JUNE 2014) (T2(2e)– 112-120)
- Reduce the function after identifying the essential and non essential prime implicants. $F = A'B'C'D' + A'B'C'D + A'B'CD + A'BC'D' + A'BC'D + A'BCD$ (NOV/DEC 2010), (APR/MAY 2010) (T2(2e)– 112-120)
- Design Half adder and Full Adder (APR/MAY 2011), (APR/MAY 2010), (NOV/DEC 2012) (NOV/DEC 2013) (T2– 119-122)
- Design a Half Subtractor and full subtractor circuit (APR/MAY 2011), (NOV/DEC 2011), (NOV/DEC 2010), (MAY/JUNE 2013) (NOV/DEC 2016) (T2– 143-157)
- Explain the carry look ahead adder (NOV/DEC 2010) (T2– 123-126)
- Design a code converter (NOV/DEC 2010), (APR/MAY 2010), (NOV/DEC 2011), (NOV/DEC 2012) (MAY/JUNE 2013) (NOV/DEC 2013) (MAY/JUNE 2014) (T2– 116-118)
- Design a decoder and problems (NOV/DEC 2013) (T2– 134-138)
- Design an encoder (T2– 139-141)
- Design and construct an eight input priority encoder (MAY/JUNE 2012) (T1– 140-141)
- Design a combinational circuit that will multiply two 2 bit binary values (MAY/JUNE 2012), (APR/MAY 2011) (T2- 131-132)
- Design a Magnitude Comparator (APR/MAY 2011), (NOV/DEC 2011), (APR/MAY 2010) (T2– 133-134)
- Design a demultiplexer (NOV/DEC 2011) (Bakshi text book)
- Design a multiplexer (T2– 141-146)

17. Implement the function $F(A, B, C, D) = \sum 1,3,5,6$ using MUX (*NOV/DEC 2010*), (*MAY/JUNE 2013*), (*APR/MAY 2010*) (*MAY/JUNE 2014*) (T2– 144-145)
18. Draw the logic diagram of IC 74138 and explain the operation with truth table (*NOV/DEC 2012*) (T2– 175-179)

Unit – III
SYNCHRONOUS SEQUENTIAL CIRCUITS
PART – A

1. Define sequential circuit?

In sequential circuits the output variables dependent not only on the present input variables but they also depend up on the past history of these input variables.

2. What are the classification of sequential circuits?

The sequential circuits are classified on the basis of timing of their signals into two types. They are,

- 1) Synchronous sequential circuit.
- 2) Asynchronous sequential circuit.

3. What do you mean by present state?

The information stored in the memory elements at any given time defines the present state of the sequential circuit.

4. What do you mean by next state?

The present state and the external inputs determine the outputs and the next state of the sequential circuit.

5. What are the types of sequential circuits?

- Synchronous sequential circuits
- Asynchronous sequential circuits

6. Define synchronous sequential circuit

In synchronous sequential circuits, signals can affect the memory elements only at discrete instant of time. A synchronous sequential circuit is a system whose behavior can be defined from the knowledge of its signals at discrete instants of time.

7. Define Asynchronous sequential circuit?

In asynchronous sequential circuits change in input signals can affect memory element at any instant of time

8. What is edge triggering and what are its types? (*NOV/DEC 2015*)

Flip flop change states when commanded to do so by a synchronizing clock pulse. When the flip flop changes state on the clock edge it is said to be edge triggered. Both positive and negative edge triggered flip flop are commonly available.

9. Define flip-flop

Flip - flop is a sequential device that normally. samples its inputs and changes its outputs only at times determined by clocking signal.

10. What are the applications of flip flops?

1. Shift registers
2. Counters
3. Sequence detector
4. Memory unit
5. Clock pulse generator
6. Serial adder

11. List various types of flip-flop

- 1] SR latch
- 2] D latch
- 3] Clocked J.K. flip-flop
- 4] T flip-flop

12. What is race around condition?

In the JK latch, the output is feedback to the input, and therefore change in the output results change in the input. Due to this in the positive half of the clock pulse if J and K are both high then output toggles continuously. This condition is known as race around condition.

13. What are the two models in synchronous sequential circuits.

- Moore circuit
- Mealy circuit

14. What is Mealy circuit? (NOV/DEC 2015)

When the output of the sequential circuit depends on both the present state of flip-flop and on the input, the sequential circuit is referred to as mealy circuit.

15. What is moore circuit? (NOV/DEC 2015)

When the output of the sequential circuit depends only on the present state of the flip-flop, the sequential circuit is referred to as moore circuit.

16. Differentiate Mealy and Moore model (NOV/DEC 2016), (MAY/JUNE 2016)(NOV/DEC 2014)

S.No	Mealy circuit	Moore circuit
1	When the output of the sequential circuit depends on both the present state of flip-flop and on the input, the sequential circuit is referred to as mealy circuit.	When the output of the sequential circuit depends only on the present state of the flip-flop, the sequential circuit is referred to as moore circuit
2		

17. What is a latch?

A pair of inverting gates (NAND or NOR) arranged such that the output of one gate is connected to the input of the other. This connection scheme permits the latch to remember (by changing state) what the excitation input was. A latch is not considered the same as a flip flop contains latches. A flip flop is clocked and a latch is not.

18. What is a counter?

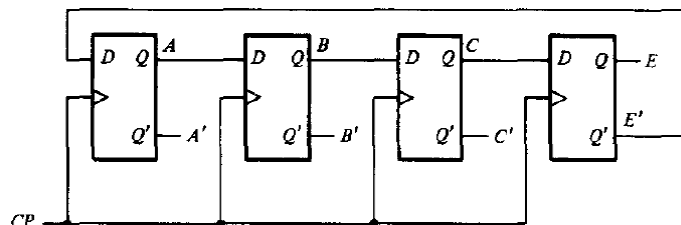
A digital counter is a collection of flip flops arranged in such a manner as to change state in a prescribed sequence. For example, binary counter state variables change state in the binary code. A BCD counter counts in BCD code. Counters can be either synchronous or asynchronous.

19. What are the types of counter?

- Synchronous counter
- Asynchronous Counter

20. What is a Johnson counter?

A Johnson counter is a k-bit switch-tail ring counter with 2k decoding gates to provide outputs for 2k timing signals.



21. Define shift Registers

The binary information in a register can be moved from stage to stage within the register or into or out of the register upon application of clock pulses. This type of bit movement or shifting is essential for certain arithmetic and logic operations used in microprocessors. This gives rise to a group of registers called shift registers.

22. What are the types of shift register?

- Serial in serial out shift register?
- Serial in parallel out shift register
- Parallel in serial out shift register
- Parallel in parallel out shift register
- Bidirectional shift register shift register.

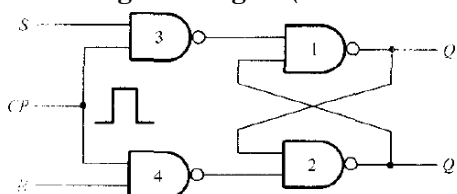
23. What is a ripple counter (MAY/JUNE 2012)(NOV/DEC 2012)

MSI counters come in two categories: ripple counters and synchronous counters. In a ripple counter, the flip-flop output transition serves as a source for triggering other flip flops. In other words, the *CP* inputs of all flip-flops (except the first) are triggered not by the incoming pulses, but rather by the transition that occurs in other flip-flops. A binary ripple counter consists of a series connection of complementing flip-flops (*T* or *JK* type), with the output of each flip-flop connected to the *CP* input of the next higher-order flip-flop. The flip-flop holding the least significant bit receives the incoming count pulses. Ripple counters are sometimes called asynchronous counters.

24. What are the drawbacks of ripple counter? (NOV/ DEC 2012)

- They are asynchronous circuits, and can be unreliable and delay dependent, if more logic is added.
- Large ripple counters are slow circuits due to the length of time required for the ripple to occur.
- Because of new count "rippling" through the flip flops all the bits of the count arrive at different times.
- all the bits are updated at the same time; the flip-flops are all using different clocks.

25. Show how a RSFF can be built using NAND gate (MAY/JUNE 2012)



26. State an application each for D and T flip flop (APR/MAY 2011)

D – Flip flops: shift registers, Delay elements
 T – Flip flops: Counters

27. State the difference between combinational and sequential circuits (APR/MAY 2011)

S.No	COMBINATIONAL CIRCUITS	SEQUENTIAL CIRCUITS
1	The output depends on the present state and not on the past or the future values of the input	The output depends on the present state and also on the past or the future values of the input
2	These circuits do not have memory elements	These circuits have memory elements
3	No feedback path between the input and the output	feedback path is present between the input and the output
4	Example: Parallel Adder	Example: Serial adder

28. Write the rules for the state assignment in a synchronous sequential circuits (NOV/DEC 2011)(APR/MAY 2015)

RULE 1: States having the same state for a given input condition should have assignments that can be formed into a prime implicant.

RULE 2: The next states of a single present state should have state assignments that can be formed into a prime implicant

RULE 3: Adjacent assignments should be given to states that have the same outputs.

29. What do you mean by completely specified and incompletely specified function? (MAY/JUNE 2013) (MAY/JUNE 2014)

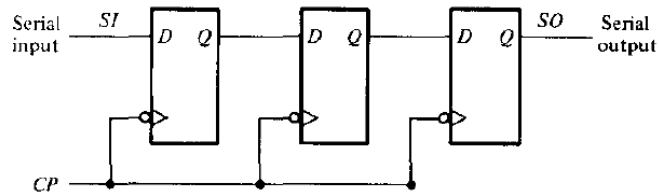
Completely specified functions includes the unused states and considers the don't care conditions.

Incompletely specified functions does not include the unused states and does not consider the don't care conditions.

30. List the applications of shift registers (MAY/JUNE 2013)

- Digital memory
- Converting parallel data to serial data and vice versa
- Used in CDMA

31. Draw the 3 – bit shift register circuit. (NOV/DEC 2011)



32. What is the drawback in RS flip flop? (NOV/DEC 2010)

An indeterminate condition occurs when $CP = 1$ and both S and R are equal to 1. When the CP input goes back to 0 (while S and R are maintained at 1), it is not possible to determine the next state, This indeterminate condition makes the circuit difficult to manage and it is seldom used in practice.

33. Why is state reduction necessary? (NOV/DEC 2010), (NOV/DEC 2013)

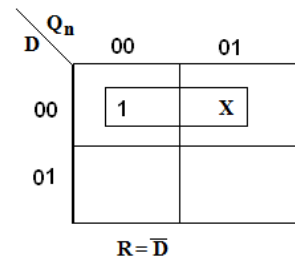
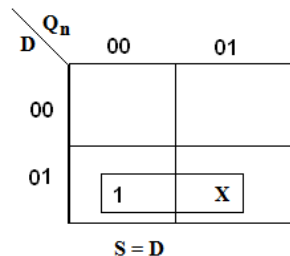
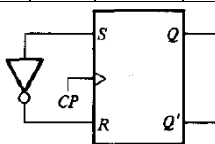
Any design process must consider the problem of minimizing the cost of the final circuit. The two most obvious cost reductions are reductions in the number of flip-flops and the number of gates. The reduction of the number of flip-flops in a sequential circuit is referred to as the *state-reduction*. State-reduction algorithms are concerned with procedures for reducing the number of states in a state table while keeping the external input-output requirements unchanged.

34. Define Equivalent state (APR/MAY 2010)

Two sequential networks are said to be equivalent if every state in the first network has an equivalent state in the second and vice versa

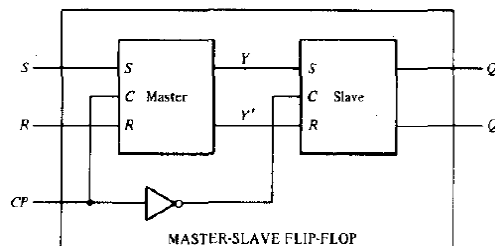
35. Convert SR flip flop to D flip flop (APR/MAY 2010)

D	Q_n	Q_{n+1}	S	R
0	0	0	0	X
0	1	0	0	1
1	0	1	1	0
1	1	1	X	0



36. What is a master slave flip flop

A master-slave flip-flop is constructed from two separate flip-flops. One circuit serves as a master and the other as a slave, and the overall circuit is referred to as a master slave flip-flop.



37. How many flip flops are required to build a binary counter that counts from 0 to 128?(NOV/DEC 2013)

7 flip flops are required

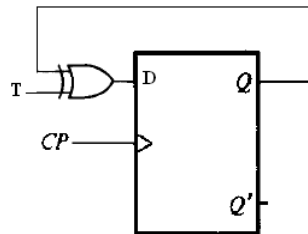
38. Convert D Flip flop to T flip flop (MAY/JUNE 2014)

T	Q _n	Q _{n+1}	D
0	0	0	0
0	1	1	1
1	0	1	1
1	1	0	0

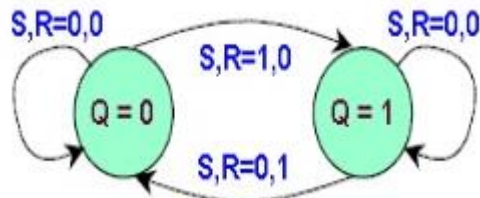
		Q _n	
		00	01
T	00		1
	01	1	

$$D = \bar{T}Q_n + T\bar{Q}_n$$

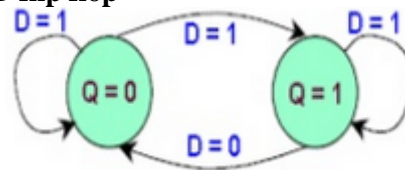
$$= T \oplus Q_n$$



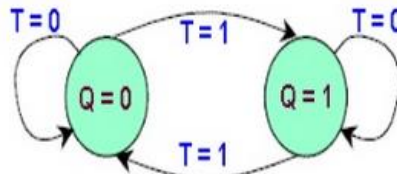
39. Draw the state diagram of SR flip flop (NOV/DEC 2015)



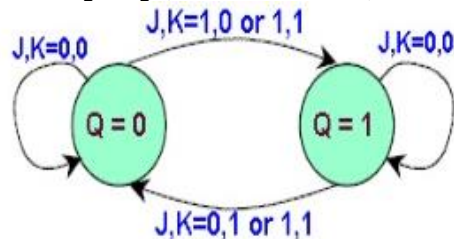
40. Draw the state diagram of D flip flop



41. Draw the state diagram of T flip flop



42. Draw the state diagram of JK flip flop (NOV/DEC 2016)



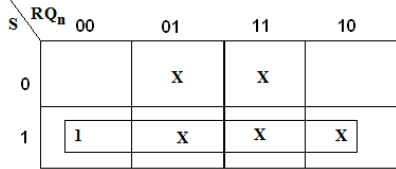
43. Give the characteristic equation and characteristic table of SR flip flop (MAY/JUNE 2015)

S	R	Q	Q'
1	0	1	0
0	0	1	0
0	1	0	1
0	0	0	1
1	1	0	0

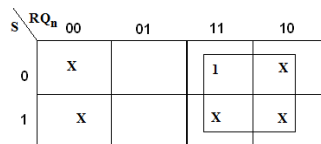
and $Y = SR' + R'y$

44. Convert JK flip flop to SR flip flop (NOV/DEC 2012)

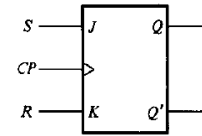
S	R	Q _n	Q _{n+1}	J	K
0	0	0	0	0	X
0	0	1	1	X	0
0	1	0	0	0	X
0	1	1	0	X	1
1	0	0	1	1	X
1	0	1	1	X	0
1	1	0	X	X	X
1	1	0	X	X	X



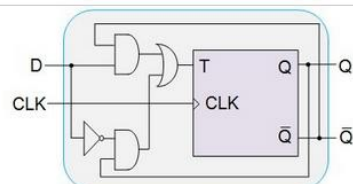
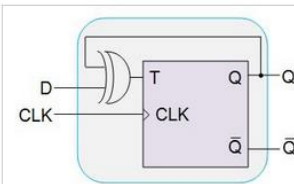
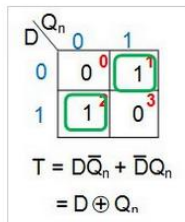
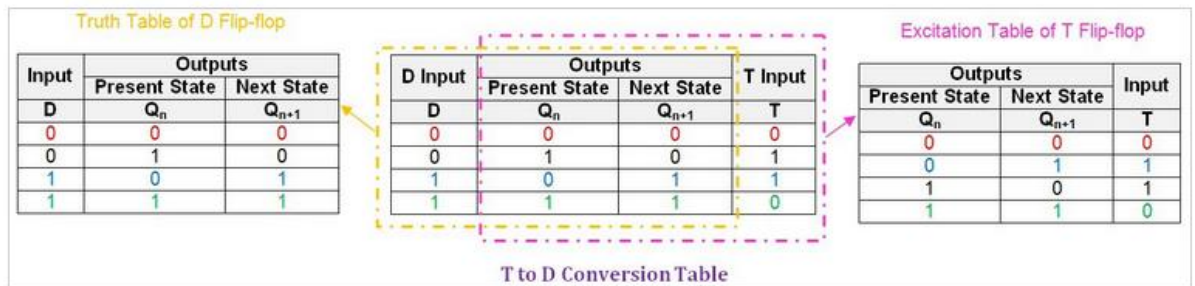
$$J = S$$



$$K = R$$

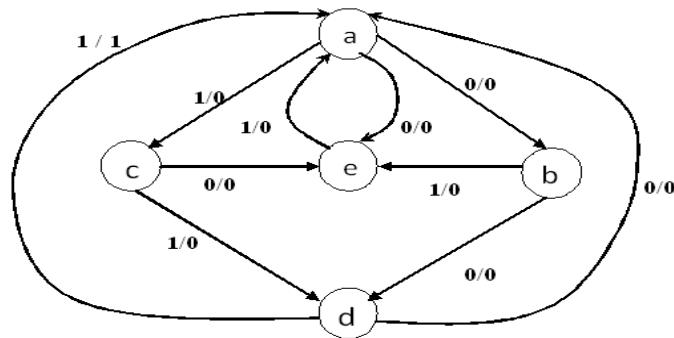


45. Convert T Flip Flop to D Flip Flop. (APR/MAY 2015)



PART – B

1. Compare synchronous and asynchronous sequential circuits (APR/MAY 2010) (Bakshi text book)
2. Draw the state diagram and characteristics equation, excitation table of T FF, D FF and JK FF (NOV/DEC 2011), (NOV/DEC 2010), (NOV/DEC 2012) (NOV/DEC 2013) (T2– 177-178, 180-190, 207)
3. Flip flop conversion (MAY/JUNE 2013) (Bakshi text book)
4. Design a sequential circuit with 4 FF ABCD. The next state of B, C, D are equal to the present states of A, B, C. the next state of A is equal to the ex-OR of the present states of C and D. (MAY/JUNE 2012)
5. Discuss the working of serial in parallel out 4 bit shift register with an example and a timing diagram (APR/MAY 2011), (NOV/DEC 2012) (NOV/DEC 2013) (T2– 219-226)
6. Design and explain the operation of synchronous counter (APR/MAY 2010), (NOV/DEC 2010), (NOV/DEC 2011), (APR/MAY 2011), (MAY/JUNE 2012), (NOV/DEC 2012), (MAY/JUNE 2013) (NOV/DEC 2013)(MAY/JUNE2014)(T2– 232-239)
7. Design a BCD ripple counter (NOV/DEC 2010) (T2- 230-232)
8. Design a sequential circuit for a state diagram shown in the following figure. Use state assignment rules for assigning states and compare the required combinational circuit with straight binary assignment (APR/MAY 2010) (Bakshi text book)



Unit – IV
ASYNCHRONOUS SEQUENTIAL CIRCUITS
PART – A

1. What are compatible states?

Two incompletely specified states that can be combined are said to be *compatible*. Two states are compatible if for each possible input they have the same output whenever specified and their next states are compatible whenever they are specified.

2. What is equivalence class?

A group of states that have the same output sequence for a given input sequence. By grouping or classifying states according to their output sequence for a given input sequence, we can eventually identify the redundant states

3. What is implication table?

The state-reduction procedure for completely specified state tables is based on the algorithm that two states in a state table can be combined into one if they can be shown to be equivalent. Two states are equivalent if for each possible input, they give exactly the same output and go to the same next states or to equivalent next states. The checking of each pair of states for possible equivalence in a table with a large number of states can be done systematically by means of an implication table. The implication table is a chart that consists of squares, one for every possible pair of states that provide spaces for listing any possible implied states. By judicious use of the table, it is possible to determine all pairs of equivalent states.

4. What is implication graph?

A flow graph used to aid in determining the assignment of adjacent binary codes for states. An implication graph is a flow graph with directed arcs indicating the state transition of a sequential machine. Each node on the graph represents a state adjacency pair.

5. Explain state reduction?

State reduction algorithm is stated as “Two states are said to be equivalent if, for each member of the set of inputs they give the same output and send the circuit either to the same state or to an equivalent state. When two states are equivalent, one of them can be removed without altering the input-output relation.

6. What is a hazard?

Hazards are unwanted switching transients that may appear at the output of a circuit because different paths exhibit different propagation delays. Hazards occur in combinational circuits, where they may cause a temporary false output value. When this condition occurs in asynchronous sequential circuits, it may result in a transition to a wrong stable state.

7. What are the different types of hazards in asynchronous circuits? (NOV/DEC 2011)

- Static – 1 hazard
- Static – 0 hazard
- Dynamic Hazard
- Essential Hazard

8. What is a static - 0 hazard? (NOV/DEC 2016)(APR/MAY 2015)

When the output goes to 1 when it should remain at 0 is called static – 0 hazard.



9. What is a static - 1 hazard? (NOV/DEC 2016) (APR/MAY 2015)

When the output goes to 0 when it should remain at 1 is called static – 1 hazard.



10. What is dynamic hazard? (NOV/DEC 2016)

Dynamic hazard causes the output to change three or more times when it should change from 1 to 0 or from 0 to 1.



11. What is essential hazard and how it can be eliminated?

An essential hazard is caused by unequal delays along two or more paths that originate from the same input. An excessive delay through an inverter circuit in comparison to the delay associated with the feedback path may cause such a hazard. Essential hazards cannot be corrected by adding redundant gates as in static hazards. The problem that they impose can be corrected by adjusting the amount of delay in the affected path. To avoid essential hazards, each feedback loop must be handled with individual care to ensure that the delay in the feedback path is long enough compared to delays of other signals that originate from the input terminals.

12. What is merger graph? (MAY/JUNE 2014)

A graphical technique for identifying possible redundant states. A diagram is drawn with a set of nodes where each node represent a state. A line is drawn between the nodes if, for every input, the same next state is reached and the output is the same. If equivalency between two states is dependent on another state pair equivalency, then those state symbols are written adjacent to the line connecting the two state nodes.

13. What is critical race?

If it is possible to end up in two or more different stable states, depending on the order in which the state variables change, then it is a critical race

14. What is a non-critical race?

If the final stable state that the circuit reaches does not depend on the order in which the state variables change, the race is called a noncritical race

15. What is a cycle? (NOV/DEC 2013)

When a circuit goes through a unique sequence of unstable states, it is said to have a *cycle*. Care must be taken when using a cycle that it terminates with a stable state. If a cycle does not terminate with a stable state, the circuit will keep going from one unstable state to another, making the entire circuit unstable.

16. What is a flow table?

A flow table is a tabular method for showing asynchronous circuit state transition. A row exists for every internal state and columns for each input permutations. Each cell in the flow table shows the next internal state. The output values can be included in the next state cell or separated into an output section.

17. What is fundamental mode?

To ensure proper operation, asynchronous sequential circuits must be allowed to attain a stable state before the input is changed to a new value. Because of delays in the wires and the gate circuits, it is impossible to have two or more input variables change at exactly the same instant of time without an uncertainty as to which one changes first. Therefore, simultaneous changes of two or more variables are usually prohibited. This restriction means that only one input variable can change at anyone time and the time between two input changes must be

longer than the time it takes the circuit to reach a stable state. This type of operation is defined as *fundamental mode*. Fundamental-mode operation assumes that the input signals change one at a time and only when the circuit is in a stable condition.

18. Define merging?

The primitive flow table has only one stable state in each row. The table can be reduced to a smaller number of rows if two or more stable states are placed in the same row of the flow table. The grouping of stable states from separate rows into one common row is called merging.

19. What is the use a merger graph (MAY/JUNE 2013)

Merger table is a substitute application of Merger graph. From a Merger graph we can get the compatible pairs and implied pairs. If number of states of a machine increases, number of combination pair increases. For a machine of n states, number of two state combinations are nC_2 i.e. $n(n-1)/2$. If $n=(n-1)$, number of combinations are $(n-1)(n-2)/2$. Number of combination increases to $(n-1)$ if number of states increases from $(n-1)$ to n . It is difficult to connect two states by arcs in a merger graph, if number of states increase. Hence a Merger table is an easier process to find compatible pairs and implied pairs.

20. List the advantages of SM chart (MAY/JUNE 2012)

- The ASM chart resembles a conventional flow chart, but is interpreted somewhat differently.
- The ASM chart describes the sequence of events as well as the timing relationship between the states of a sequential controller and the events that occur while going from one state to the next.
- It is specifically adapted to specify accurately the control sequence and data processing operations in a digital system, taking into consideration the constraints of digital hardware.

21. What is a pulse mode circuit? (APR/MAY 2011)

The input variables are pulses instead of levels. The width of the pulses is long enough for the circuit to respond to the input. The pulse width must not be so long that it is still present after the new state is reached.

22. What is a Moore machine? (APR/MAY 2011)

In the Moore model, the outputs are a function of the present state only and not on the inputs .

23. What is triggering of flip flops. (NOV/DEC 2010)

The state of a flip-flop is switched by a momentary change in the input signal. This momentary change is called a *trigger* and the transition it causes is said to trigger the flip flop. Clocked flip-flops are triggered by *pulses*. A pulse starts from an initial value of 0, goes momentarily to 1, and after a short time, returns to its initial 0 value.

24. What are the two types of Asynchronous sequential circuits (APR/MAY 2010), (MAY/JUNE 2014) (MAY/JUNE 2016)

- Fundamental mode
- Pulse mode

25. Compare pulse mode and fundamental mode (NOV/DEC 2015)

S.No	PULSE MODE	FUNDAMENTAL MODE
1	the inputs and outputs are represented by pulses.	No simultaneous changes of two or more variables
2	only one input is allowed to have pulse present at any time.	The time between two input changes must be longer than the time it takes the circuit to a stable state
3	Similar to synchronous sequential circuits except without a clock signal	The input signals change one at a time and only when the circuit is in a stable condition Fundamental Mode

26. What are the problems involved in asynchronous circuits?

The asynchronous sequential circuits have three problems namely,

- a. Cycles
- b. Races
- c. Hazards

27. What are races? How can it be avoided? (APR/MAY 2010)(NOV/DEC2012), (MAY/JUNE 2013), (NOV/DEC 2016)

When 2 or more binary state variables change their value in response to a change in an input variable, race condition occur in an asynchronous sequential circuit. In case of unequal delays, a race condition may cause the state variable to change in an unpredictable manner. Races may be avoided by making a proper binary assignment to the state variables.

28. Differentiate stable and unstable states. (NOV/ DEC 2012)

S.No	STABLE STATE	UNSTABLE STATE
1	The state is stable if the present and next state are same	The state is unstable if the present and next state are not same

29. Explain state assignment?

Sequential machine states are assigned binary codes. The process of making the assignment of the codes to the states is called state assignment

30. What is primitive flow table? (NOV/DEC 2013)

It is a flow table that has only one stable state for each row in the table. The synthesis process usually starts by the construction of a primitive flow table based on the problem statement.

31. What are the type's state assignments? shared row state assignment, multiple row state assignment, one hot state assignment

32. What is a PLD?

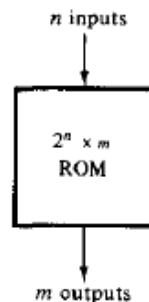
A programmable logic device (PLD) is an integrated circuit with internal logic gates that are connected through electronic fuses. Programming the device involves the blowing of fuses along the paths that must be disconnected so as to obtain a particular configuration. The word "programming" here refers to a hardware procedure that specifies the internal configuration of the device. The gates in a PLD are divided into an AND array and an OR array that are connected together to provide an AND-OR sum of product implementation. The initial state of a PLD has all the fuses intact. Programming the device involves the blowing of internal fuses to achieve a desired logic function.

33. List the basic types of PLD's.

- a. PROM – Programmable Read Only memory
- b. PLA – Programmable Logic Array
- c. PAL – Programmable Array Logic
- d. FPGA – Field Programmable Gate Array
- e. CPLD – Complex Programmable Logic Devices

34. Define ROM

A read only memory is a device that includes both the decoder and the OR gates within a single IC package. A ROM is essentially a memory (or storage) device in which permanent binary information is stored. The binary information must be specified by the designer and is then embedded in the unit to form the required interconnection pattern. ROMs come with special internal electronic fuses that can be "programmed" for a specific configuration. Once the pattern is established, it stays within the unit even when power is turned off and on again.



35. What are the types of ROM

- Masked ROM.
- Programmable Read only Memory
- Erasable Programmable Read only memory.
- Electrically Erasable Programmable Read only Memory.

36. What is programmable logic array? How it differs from ROM?

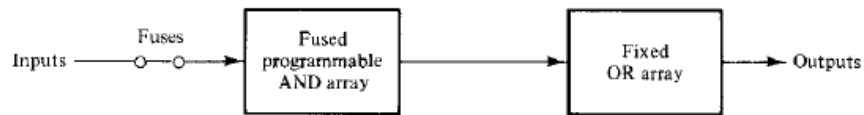
In some cases the number of don't care conditions is excessive, it is more economical to use a second type of LSI component called a PLA. A PLA is similar to a ROM in concept; however it does not provide full decoding of the variables and does not generate all the minterms as in the ROM.

37. What is the advantage of using PLD's in the digital design?

The advantage of using PLDs in the design of digital systems is that they can be programmed to incorporate complex logic functions within one LSI circuit. The use of programmable logic devices is an alternative to another design technology called VLSI design.

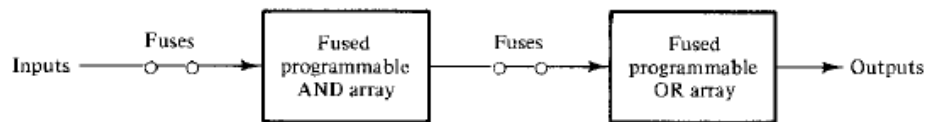
38. What is PAL?

It is a PLD that has fixed OR gates and a programmable AND array.



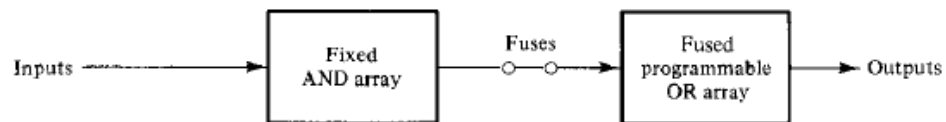
39. What is a PLA? (NOV/DEC 2010)(NOV/DEC 2014)

It is a PLD where both AND and OR array is programmable.



40. What is PROM? (NOV/DEC 2015)(APRIL/MAY 2015)

It is a PLD where AND array is fixed and OR array is programmable



41. Compare PROM, PLA, PALs (MAY/JUNE 2016)

S.No	PROM	PLA	PAL
1.	AND array is fixed and OR array is programmable	Both AND and OR array is programmable	OR is fixed and AND array is programmable
2.	Cheaper and simple to use	Cheaper and simpler	Costlier and complex than PLA and PROM
3.	All minterms are decoded	And array can be programmed to get the desired minterms	AND array can be programmed to get the desired minterms
4.	Only Boolean functions in standard SOP form can be implemented using PROM.	Any Boolean function in SOP form can be implemented using PLA.	Any Boolean function in SOP form can be implemented using PAL.

42. What are the terms that determine the size of a PAL?

The size of a PLA is specified by the

- Number of inputs
- Number of products terms
- Number of outputs

43. What is CLB?

A Configurable Logic Block consists of a programmable look up table, multiplexers, registers and paths for control signals. Two function generators (F and G) of the look up table can generate any arbitrary function of four inputs, and the third (H) can generate any Boolean function of three inputs.

44. What is EEPROM?

EEPROM refers to Electrically Erasable Programmable Read Only Memory. Wherein the data stored can be erased or altered by applying the electrical signals. The desired part of data can be erased

45. What is EPROM? (APR/MAY 2011)

EPROM refers to Erasable Programmable read only memory. The data stored can be erased by passing the UV rays. The main drawback of this type of memory is that a block of data cannot be erased the entire content is erased in this type.

46. List the applications of EPROM

- Some microcontroller before the era of the E²PROM and flash memory, use an on-chip EPROM to store their program
- Storing prices of vegetables.

47. Compare RAM and ROM.

S.No	RAM	ROM
1.	Volatile memory	Non-volatile memory
2.	Read write control is present	Read write control is absent

48. List the applications of ROM

- Storing values of logarithms
- For storing the look up tables containing mathematical constants

49. List the applications of PROM

- Emergency stop procedure for an industrial mill now the design stage
- All applications where data does not change but the required data will not be available until a later time suggests the use of a PROM.

50. What are the applications of PLA? (MAY /JUNE 2012), (NOV/DEC 2011), (NOV/DEC 2010)

1. To implement the control over data path
2. To implement the combinational circuits
3. To implement various sequential circuits
4. To implement glue logic

What is memory expansion? (NOV/DEC 2013)

Memory expansion is providing additional memory beyond the limit of the conventional memory of the system.

51. What is FPGA?

A FPGA is a VLSI circuit that consists of look up tables, multiplexers, gates and flip flops surrounded by programmable input and output blocks and connected together via programmable interconnections.

What are the various components of FPGA?

The Xilinx FPGA family of IC devices consists of an array of configurable logic blocks (CLBs). 110 blocks (IOBs). and a switching interconnect matrix

52. What are the applications of FPGA

FPGAs are suitable for implementation of circuits over a large range of size, from about 1000 to more than a million equivalent logic gates. In addition to size a designer will consider other criteria, such as the needed speed of operation of a circuit, power dissipation constraints, and the cost of the chips.

53. What do you mean by logic level?

Two voltage levels used to represent two logic states are called logic levels. There are two types namely,

- Positive logic system
- Negative logic system

54. What are the advantages of digital integrated circuits?

- The traditional method of designing combinational circuits is effective for small circuit. But time consuming and less reliable for complex circuits digital ICs take care of problem.
- Digital ICs reduce system cost.
- They are smaller in size.
- Less power is required for the system
- Lesser number of external wire connections which improves reliability of the system
- Depending upon circuit complexity, any of the 5 levels of integration can be chosen.

55. What is RAM and what are its types?

RAM refers to read only memory, wherein the data can only be read and not written. It is a volatile memory. The two types of RAM are,

1. SRAM
2. DRAM

56. Compare SRAM and DRAM?

S.No	SRAM	DRAM
1.	It refers to Static RAM	It refers to dynamic RAM
2.	It uses flip flops as storage elements	It uses capacitors as storage devices
3.	SRAM cell is complex	DRAM cell is much easier
4.	Data can be read much faster from SRAM than from DRAM	Data can be read slower than from SRAM

57. Compare RAM and ROM.

S.No	RAM	ROM
1	Volatile memory	Non-volatile memory
2	Read write control is present	Read write control is absent
3	Types: SRAM, DRAM	Types: PROM, EPROM, EEPROM

58. What are the advantages of RAM?

The advantages of RAM are

- Non-destructive read out
- Fast operating speed
- Low power dissipation
- Compatibility Economy

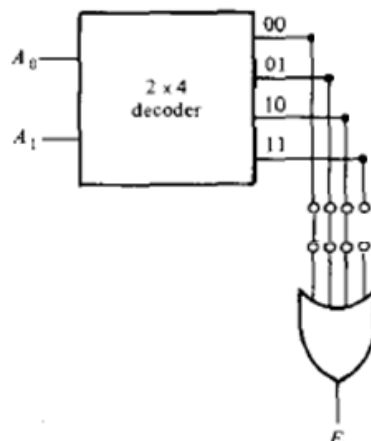
59. List the applications of RAM

- Main memory of hand calculator
- Main memory of computer

60. What are the various types of hazards in synchronous sequential circuits?

1. Static – 0 Hazard
2. Static – 1 Hazard
3. Dynamic Hazard
4. Essential Hazard

61. Implement the following using a suitable PROM $F = \sum m(0,1,2)$ (APR/MAY 2010)



62. What are the rules of state assignment (APR/MAY 2015)

63. Differentiate synchronous and Asynchronous sequential circuits. (NOV/DEC 2011), (MAY/JUNE 2012)

S.No	SYNCHRONOUS CIRCUIT	ASYNCHRONOUS CIRCUIT
------	---------------------	----------------------

1	A sequential circuit is specified by a time sequence of inputs, outputs, and internal states.	Asynchronous sequential circuits do not use clock pulses.
2	In synchronous sequential circuits, the change of internal state occurs in response to the synchronized clock pulses.	The change of internal state occurs when there is a change in the input variables.
3	The memory elements in synchronous sequential circuits are clocked flip flops.	The memory elements in asynchronous sequential circuits are either unclocked flip-flops or time-delay elements.
4	Design is easy	Design is difficult

64. What is asynchronous sequential circuit? (NOV/DEC 2010)

Asynchronous sequential circuits do not use clock pulses. The change of internal state occurs when there is a change in the input variables. The memory elements in asynchronous sequential circuits are either unclocked flip-flops or time-delay elements. Design is difficult

65. What are the steps involved in designing a asynchronous sequential circuit?

- State the design specifications.
- Derive a primitive flow table.
- Reduce the flow table by merging the rows.
- Make a race-free binary state assignment.
- Obtain the transition table and output map.
- Obtain the logic diagram using *SR* latches.

66. What is a deadlock condition? (NOV/DEC 2014)

67. What are the applications of asynchronous sequential circuits?

- Digital system must respond quickly without having to wait for a clock pulse.
- In small independent systems that require only a few components
- In applications where the input signals to the system may change at any time, independently of an internal clock.
- The communication between two units, with each unit having its own independent clock, must be done with asynchronous circuits.

PART – B

1. How do you identify and eliminate static and dynamic hazards from an asynchronous sequential circuit? Explain. (MAY/JUNE 2012) (NOV/DEC 2011) (NOV/DEC 2012) (R6– 232-237, 474 - 477)
2. Find whether static ‘O’ hazard does not exist in implementing the Boolean expression: $Y = x_1x_3 + x_1x_2x_3 + \overline{x_2}x_3$. If exists, then find the static hazards present (MAY/JUNE 2012) (R6– 232-237)
3. Construct a Mealy state diagram that will detect a serial input sequence of 10110. The detection of the required bit pattern can occur in a longer data string and the correct pattern can overlap with another pattern. When the input pattern has been detected, cause an output ‘Z’ to be asserted high (MAY/JUNE 2012) (R6– 349- 351)
4. Design a two input (x_1, x_2), two output (z_1, z_2) fundamental circuit that has the following specifications. When $x_1x_2 = 00$, $z_1z_2 = 00$. The output 10 will be produced following the occurrence of the input sequence 00 – 01 – 11. The output will remain 10 until the input returns to 00, at which time it becomes 00. An output of 01 will be produced following the receipt of the input sequence 00 -10 -11. And once again, the output will remain 01 until occurs, which returns the output to 00. (APR/MAY 2011) (BAKSHI TEXT BOOK)
5. Design a pulse mode circuit having two input lines x_1 and x_2 and output line Z. the circuit should produce an output pulse to coincide with the last input pulse in the sequence $x_1 - x_2 -$

- x_2 . No other input sequence should produce an output pulse. (*APR/MAY 2011*), (*MAY/JUNE 2013*) (**BAKSHI TEXT BOOK**)
6. Design an asynchronous sequential circuit that has the inputs X_1 and X_2 and one output Z . when $X_1 = 0$, the output Z is 0. The first change in X_2 that occurs while X_1 is 1 will cause output Z to be 1. The output Z will remain 1 until X_1 returns to 0. (*NOV/DEC 2011*), (*MAY/JUNE 2013*) (**R6– 465-469**)
 7. Develop the state diagram and primitive row flow table for a logic system that has two inputs S and R and a single output Q . the device is to be an edge triggered SR flip flop but without a clock. The device changes state on the rising edge of the two inputs. Static input values are not to have any effect in changing the Q input. (*NOV/DEC 2010*) (**R6– 453-455**)
 8. An asynchronous sequential circuit is described by the following excitation and output functions

$$Y = X_1 X_2 + (X_1 + X_2)Y$$

$$Z = Y$$
 - a. Draw the logic diagram of the circuit
 - b. Derive the transition table and the output map
 - c. Describe the behaviour of the circuit
 9. An asynchronous circuit has two internal states and one output. The excitation and output function describing the circuit are as follows (*APR/MAY 2010*) (**BAKSHI TEXT BOOK**)

$$Y = x_1 x_2 + x_1 y_2 + x_2 y_1$$

$$Y = x_2 + x_1 y_1 y_2 + x_1 y_1$$

$$Z = x_2 + y_1$$
 - a. Draw the logic diagram of the circuit
 - b. Derive the transition table and the output map
 - c. Describe the behaviour of the circuit
 10. Design an asynchronous sequential circuit with 2 inputs T and C . The output attains a value of 1 when $T = 1$ & C moves from 1 to 0. Otherwise the output is 0. (*NOV/DEC 2013*) (**BAKSHI TEXT BOOK**)
 11. Design an asynchronous circuit that has two inputs x_1 and x_2 and one single output z . The circuit is required to give an output whenever the input sequence 00, 10, 11 and 01 are received but only in that order. (*NOV/DEC 2012*) (**BAKSHI TEXT BOOK**)
 12. Briefly comment on Races and their implication. (*NOV/DEC 2012*) (**R6– 456-458**)
 13. What are the various state assignment methods in asynchronous circuits (*NOV/DEC 2013*) (**R6– 389-398**)
 14. Write notes on PLA, PAL and PROM (*APR/MAY 2011*), (*APR/MAY 2010*), (*NOV/ DEC 2010*), (*MAY/JUNE 2013*) (*NOV/DEC 2013*) (**T2– 275 - 283**)
 15. Write detailed notes on FPGA (*MAY/JUNE 2012*), (*NOV/ DEC 2011*) (*NOV/ DEC 2012*) (*MAY/JUNE 2014*)(**T2 (2e)– 339-345**)
 16. Write detailed notes on PROM (*MAY/JUNE 2012*), (*APR/MAY 2010*) (**T2– 275 -276**)
 17. What is a RAM? Draw and explain the circuit of a typical cell of bipolar RAM (*NOV/ DEC 2011*) (*NOV/DEC 2013*) (*MAY/JUNE 2014*) (**T2 – 256 – 262**)
 18. Problems using ROM (*NOV/ DEC 2012*) (*MAY/JUNE 2013*) (*NOV/DEC 2013*) (**T2– 270 - 276**)

Unit - V

VHDL PROGRAMMING

PART-A

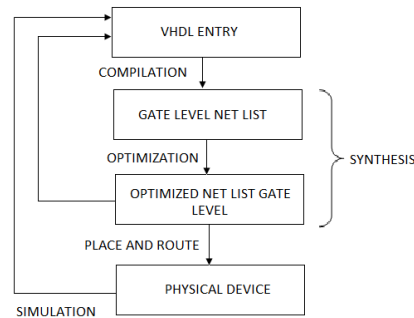
1. **What is VHDL?**
VHSIC Hardware Description Language
2. **What is VHSIC?**
Very High Speed Integrated Circuits.
3. **Write the program for AND gate in VHDL.**
entity andgate is

```

Port ( a : in std_logic;
      b : in std_logic;
      c : out std_logic);
end andgate;
architecture dataflow of andgate is
begin
  c<= a and b;
end andgate;

```

4. Draw the VHDL design flow.



5. What are the various operators in VHDL? (NOV/DEC 2015)

- Logical operators
- Relational operators
- Shift operators
- Adding operators
- Multiply operators
- Miscellaneous operators

6. What are the data types available in VHDL?

- Scalar type
- Composite type
- Access type
- File type

7. What are the various scalar types

- Enumeration
- Integer
- Physical
- Floating point

8. What are the types of subprograms?

- Functions
- Procedure

9. Define Entity.

It is used to specify the input/output pins of the circuit.

10. Define architecture

It contains the VHDL code which describes the behavior of the circuit

11. Define mode

The mode of the signal can be IN, OUT, INOUT, BUFFER

12. Define type

The type of the signal can be BIT, STD-LOGIC, INTEGER.

13. Define name

The name of the entity can be any name except VHDL reserved words.

14. What is Library declaration?

It contains a list of all libraries which are used in the design. Eg: ieee, std, work.

15. What is the use of actual?

Actual in a subprogram call is used to pass the values from and to a subprogram.

16. Write the syntax of procedure body

Procedure procedure name (parameter list)

17. What is test bench?

A test bench is a model which is used to exercise and verify the correctness of a hardware model.

18. What are the two methods to generate stimulus values?

- To create waveforms and apply stimulus at discrete time intervals
- To generate stimulus based on the state of the entity or output of the entity.

19. Differentiate between data flow modeling and structural modeling in VHDL.

S.No	Data Flow Modeling	Structural Modeling
1	A data flow model specifies the functionality of the entity without explicitly specifying its structure	Structural modeling specifies the functionality of the entity with explicitly specify its structure
2	The entity is not modeled as a set of components rather it represents sequential flow.	The entity is modeled as a set of components connected by a signal that is as a netlist.

20. What is data flow modeling in VHDL? Give its basic mechanism?

A data flow model specifies the functionality of the entity without explicitly specifying its structure. The entity is not modeled as a set of components rather it represents sequential flow.

Example:

```
library IEEE;
entity hadd is
  Port ( a : in std_logic;
        b : in std_logic;
        sum : out std_logic;
        carry : out std_logic);
end hadd;
architecture dataflow of hadd is
begin
  sum <= a xor b;
  carry <= a and b;
end dataflow;
```

21. What are Enumeration types?

It defines a type that has a set of user defined values consisting of identifiers and character literals

22. What are Integer types?

It defines a type whose set of values fall within a specific integer range.

23. What are Floating point types?

It has a set of values in a given range of real numbers.

24. What are Physical types?

It contains values that represent measurement of some physical quantity like time, length voltage or current.

25. What are Composite types?

These are composed of elements of a single type (an array type) or elements of different type(a record type)

26. What are Array types?

An object of an array type consists of elements of same or different types.

27. What are Record types?

An object of record type is composed of elements of same or different types.

28. What are Access types?

These provide access to objects of a given type. Values belonging to an access type are pointers to a dynamically allocated object of some other type.

29. What are File types?

These provide access to objects that contain a sequence of values of a given type. It provides a mechanism by which VHDL design communicates with the host environment.

Syntax: type file_type_name is file of type_name;

30. What are packages? (APR/MAY 2016)

A package is used to provide a convenient method to store and share declarations that are common for many design units.

31. What is package declaration?

It contains a set of declarations that many be shared by various design units. It defines items which are made visible to other design units.

32. Write the syntax for package declaration?

```
PACKAGE identifier IS
    package_declarative_part
END [ PACKAGE ] [ package_simple_name ] ;
```

33. What are the 2 possible delays in VHDL?

- Inertial delay
- Transport delay

34. State the advantage of package declaration over componenet declaration (NOV/DEC 2014)

A component declaration declares a virtual design entity interface that may be used in component instantiation statement.

35. What is package body?

It contains the behavior of the subprograms and the values of the deferred constants which are declared in a package declaration.

36. What is a Function?

These are used for computing a single value. It executes in zero simulation time.

37. What is a Procedure?

These are used to partition large behavioral descriptions. Procedures can return zero or more values. It may or may not execute in zero simulation time. It depends whether the wait statement is used or not.

38. Write the VHDL code to realize a 2:1 mulitplexer using data flow modeling (MAY/JUNE 2016)(NOV/DEC 2014)

```
LIBRARY IEEE;
USE IEEE.STD_LOGIC_1164.ALL;
ENTITY Multiplexer IS
PORT(S: IN STD_LOGIC_VECTOR(1 DOWNT0 0);
D0, D1, D2, D3: IN STD_LOGIC);
Y: OUT STD_LOGIC);
END Multiplexer;
ARCHITECTURE Dataflow OF Multiplexer IS
BEGIN
SIGNAL S00,S11,M0,M1,M2,M3: STD_LOGIC;
S00 <= (NOT S0);
S11 <= (NOT S1);
M0 <= (S11 AND S00 AND D0);
M1 <= (S11 AND S0 AND D1);
M2 <= (S1 AND S11 AND D2);
M3 <= (S1 AND S0 AND D3);
Y <= M0 OR M1 OR M2 OR M3;
END Dataflow;
```

39. Write the VHDL entity for a full adder

```
LIBRARY IEEE;
USE IEEE.STD_LOGIC_1164.ALL;
ENTITY fa IS
```



```

PORT (
            Ci, Xi, Yi: IN STD_LOGIC;
            Ci1, Si: OUT STD_LOGIC);
END fa;
ARCHITECTURE Dataflow OF fa IS
BEGIN
    Ci1 <= (Xi AND Yi) OR (Ci AND (Xi XOR Yi));
    Si <= Xi XOR Yi XOR Ci;
END Dataflow;

```

- 40. Write the VHDL code for a logical gate which gives high output only when both the inputs are high (NOV/DEC 2016)**

```

LIBRARY IEEE;
USE IEEE.STD_LOGIC_1164.ALL;
ENTITY and2 IS
PORT (
            a,b: IN STD_LOGIC;
            c: OUT STD_LOGIC);
END and2;
ARCHITECTURE Dataflow OF and2 IS
BEGIN
    C <= (a AND b);
END Dataflow;

```

- 41. Write the VHDL code for a D-flip flop (NOV/DEC 2016, 2015)(APR/MAY 2015)**

```

LIBRARY IEEE;
USE IEEE.STD_LOGIC_1164.ALL;
ENTITY D_flipflop IS
PORT (
            D, Clock: IN STD_LOGIC;
            Q: OUT STD_LOGIC);
END D_flipflop;
ARCHITECTURE Behavior OF D_flipflop IS
BEGIN
    PROCESS(Clock)
    BEGIN
        IF Clock'EVENT AND Clock = '1' THEN
            Q <= D;
        END IF;
    END PROCESS;
END Behavior;

```

PART-B

1. Explain About operator and data types in VHDL.
2. Write short notes on package and subprograms
3. Write a note on simulation and synthesis
4. Write VHDL program for T-flip flop in all three modelling methods.
5. Write VHDL program for D-flip flop in all three modelling methods.
6. Write VHDL program for a 4:1 multiplexer in all three modelling methods.
7. Write VHDL program for a 4 bit counter using behavioural modelling
8. Write the VHDL code for full adder using data flow, structural and behavioural modelling
9. Write VHDL program for a 1:8 demultiplexer in all three modelling methods.
10. Write the test bench for a FSM used to detect the sequence 1101
11. Explain the different timing control available in VHDL with suitable examples

ANNA UNIVERSITY PAPERS

Reg. No. :

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Question Paper Code : 50473

B.E./B.Tech. DEGREE EXAMINATION, NOVEMBER/DECEMBER 2017
Third Semester

Electrical and Electronics Engineering
EE 6301 – DIGITAL LOGIC CIRCUITS

Common to Electronics and Instrumentation Engineering/Instrumentation and
Control Engineering)
(Regulations 2013)

Time : Three Hours

Maximum : 100 Marks

Answer ALL questions

PART – A

(10×2=20 Marks)

1. Convert $(115)_{10}$ and $(235)_{10}$ to hexadecimal numbers.
2. What is a gray code and mention its advantages.
3. What is a K-map ?
4. Compare decoder and demultiplexer.
5. What do you mean by race around condition in a flip-flop ?
6. What is a preset table counter and ripple counter ?
7. What happens to the information stored in a memory location after it has been read and write operation ?
8. What is Programmable Logic Array ?
9. Define modularity.
10. What are the languages that are combined together to get VHDL language ?

50473

PART - B

(5×13=65 Marks)

11. a) Explain in detail about error detecting and error correcting code.
(OR)

b) Write short notes on following :

i) RTL

ii) DTL

iii) TTL and

iv) ECL

12. a) I) Plot the logical expression $ABCD + A\bar{B}\bar{C}\bar{D} + A\bar{B}C + AB$ on a 4-variable K-map; obtain the simplified expression from the map.
II) Express the function $Y = A + \bar{B}C$ in canonical SOP and canonical POS form.

(OR)

b) Design a 4-bit gray code to binary converter and express using logic gates.

13. a) Explain the operation, state diagram and characteristics of T-flip-flop and master-slave JK flip-flop.

(OR)

b) Explain in detail about different shift registers.

14. a) Discuss about the hazards in asynchronous sequential circuit and the ways to eliminate them.

(OR)

b) I) Write short notes on PLA and PAL.

II) What is hazards? Explain hazards in digital circuits.

15. a) Write a VHDL code to realize a full adder using behavioural modeling and structural modeling.

(OR)

b) I) Discuss briefly the packages in VHDL.

II) Write an VHDL coding for realization of clocked SR flip-flop.

PART - C

(1×15=15 Marks)

16. a) Design an asynchronous sequential circuit with two inputs x_1 and x_2 and one output Z . Initially, both inputs are equal to zero. When x_1 or x_2 becomes 1, the output Z becomes 1. When the second input also becomes 1, the output changes to 0. The output stays at 0 until the circuit goes back to the initial state.

(OR)

b) I) Design a full adder using 4×1 multiplexer, also write its truth table and draw the logical diagram.

II) Describe level triggering and edge triggering.

Reg. No.

A U H I P P O . C O M *

Question Paper Code : 71764

B.E./B.Tech. DEGREE EXAMINATION, APRIL/MAY 2017.

Third Semester

Electrical and Electronics Engineering

EE 6301 — DIGITAL LOGIC CIRCUITS

(Common to Electronics and Instrumentation Engineering, Instrumentation and Control Engineering)

(Regulations 2013)

Time : Three hours

auhippo.com

Maximum : 100 marks

Answer ALL questions.

PART A — (10 × 2 = 20 marks)

1. Reduce $a(b + bc') + ab'$.
2. Convert 143_{10} into its binary and binary coded decimal equivalent.
3. Write the *POS* form of the *SOP* expression $f(x, y, z) = x'yz + xyz' + xy'z$.
4. Design a Half Subtractor.
5. Give the characteristic equation and characteristic table of a T Flip Flop.
6. State the differences between Moore and Melay state machines.
7. What is a flow table? Give example.
8. State the difference between PROM, PAL and PLA.
9. Give the syntax for package declaration and package body in VHDL.
10. Write the VHDL code for a 2×1 multiplexer using behavioral modeling.

PART B — (5 × 13 = 65 marks)

11. (a) (i) Design an odd-parity hamming code generator and detector for 4-bit data and explain their logic.
 (ii) Convert $FACE_{16}$ into its binary, octal and decimal equivalent.

Or

- (b) (i) With circuit schematic explain the working of a two-input TTL NAND gate.
 (ii) Compare Totem Pole and open collector outputs.
12. (a) (i) Reduce the following minterms using Karnaugh – Map
 $f(w, x, y, z) = \sum m(0, 1, 3, 5, 6, 7, 8, 12, 14) + \sum d(9, 15)$. (7)
 (ii) Implement the following function using a suitable multiplexer
 $f(a, b, c) = \sum m(3, 7, 4, 5)$. (6)

Or

- (b) (i) Design a 3×8 decoder and explain its operation as a minterm generator. (7)
 (ii) Design a full adder using only NOR gates. (6)
13. (a) (i) Draw and explain the operation of a Master – Slave JK Flip Flop. (7)
 (ii) Design a 5-bit ring counter and mention its applications. (6)

Or

- (b) (i) Design a 4-bit parallel-in serial-out shift register using D Flip Flops. (7)
 (ii) Using partitioning minimization procedure reduce the following state table : (6)

Present state	Next state		Output Z
	$w = 0$	$w = 1$	
A	B	C	1
B	D	F	1
C	F	E	0
D	B	G	1
E	F	C	0
F	E	D	0
G	F	G	0

- (a) A control mechanism for a vending machine accepts nickels and dimes. It dispense merchandise when 20 cents is deposited ; it does not give change if 25 cents is deposited. Design the FSM that implements the required control, using as few states as possible. Find a suitable assignment and derive next-state and output expressions. (13)

Or

- (b) (i) Implement the following logic and analyse for the presence of any hazard $f = x_1x_2 + \bar{x}_1x_3$. If hazard is present briefly explain the type of hazard and design a hazard-free circuit. (7)
- (ii) Implement the following functions using programmable logic array :
 $f_1(x, y, z) = \sum m(0, 1, 3, 5, 7)$
 $f_2(x, y, z) = \sum m(2, 4, 6)$. (6)

- (a) Design a 3-bit magnitude comparator and write the VHDL code to realize it using structural modeling. (13)

Or

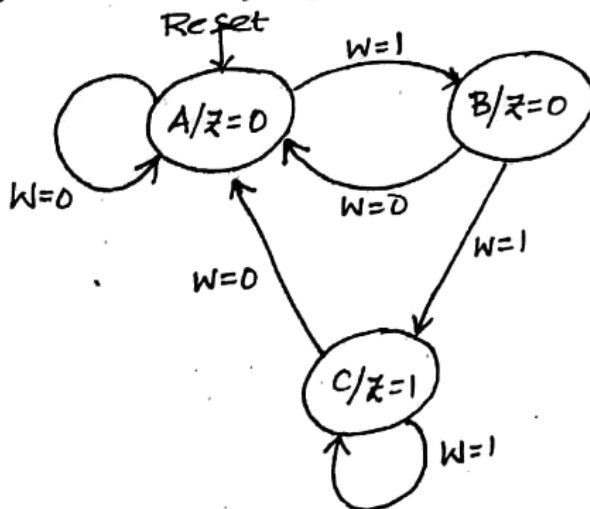
- (b) Design a 4×4 array multiplier and write the VHDL code to realize it using structural modeling. (13)

PART C — (1 × 15 = 15 marks)

- (a) Design a CMOS inverter and explain its operation. Comment on its characteristics such as Fan-in, Fan-out power dissipation, propagation delay and noise margin. Compare its advantages over other logic families. (15)

Or

- (b) Write the VHDL code for the given state diagram, using behavioral modeling. Design it using one-hot state assignment and implement it using Programmable Array Logic (PAL). (15)



NOV/DEC 2016

PART – A (Answer All questions)

(10X2=20)

1. Construct OR gate to AND gate using NAND gate.
2. Convert the following Excess – 3 number into decimal numbers
 - a. 1011
 - b. 1001 0011 0111
3. Convert the given expression in canonical SOP form $Y = AB + A'C + BC'$
4. Draw the truth table of 2:1 MUX
5. Differentiate Mealy and Moore model
6. Draw the state diagram of JK flip flop
7. What is static hazard and dynamic hazard
8. Define races in asynchronous sequential circuits
9. Write VHDL behavioural model for D flip flop
10. Write the VHDL code for a logical gate which gives high output only when both the inputs are high

PART – B (Answer all questions)

(5X13=65)

11. (a) (i) Explain with an aid of circuit diagram the operation of 2 input CMOS NAND gate and list out its advantages over other logic families

(ii) Given the two binary numbers $X = 1010100$ and $Y = 1000011$. Perform the subtraction $Y - X$ by using 2's complement.

(OR)

(b) (i) Explain in detail the usage of hamming codes for error detection and error correction with an example considering the data bits as 0101

(ii) Convert $(23.625)_{10}$ to octal (base 8)

12. (a) Simplify the logical expression K-map in SOP and POS form. $F(A,B,C,D) = \sum(0,2,3,6,7) + d\sum(8,10,11,15)$

(OR)

(b) Design a full subtractor and realise using logic gates also implement the same using half subtractors.

13. (a) Design a sequence detector that produces an output 1 whenever the non-overlapping sequence 101101 is detected.

(OR)

(b) (i) Explain the realization of JK flip flop from T flip flop

(ii) Write short notes on SIPO and draw the output waveforms.

14. (a) Design an asynchronous circuit that has 2 inputs X1 and X2 and one output Z. the circuit is required to give an output whenever the input sequence (0,0), (0,1) and (1,1) received but only in that order.

(OR)

(b) (i) Design a PLA structure using AND and OR logic for the following functions.

$F1 = \sum m(0,1,2,3,4,7,8,11,12,15)$, $F2 = \sum m(0,2,3,6,7,8,9,12,13)$, $F3 = \sum m(0,1,3,7,8,11,12,15)$, $F4 = \sum m(0,1,4,8,11,12,15)$

(ii) Compare PLA and PAL circuits

15. (a) Explain in detail the concept of structural modelling in VHDL with an example of Full adder

(b) (i) Write in short notes on built in operators used in VHDL programming

(ii) Write VHDL coding for 4X1 Multiplexer

PART – C (Answer all questions)

(1X15=15)

16. (a) Assume that there is a parking area in a shop whose capacity is 10. No more than 10 cars are allowed inside the parking area and the gate is closed as soon as the capacity is reached. There is a gate sensor to detect the entry of car which is to be synchronized with the clock pulse. Design an implement a suitable counter using JK flip flop. Also determine the number of flip flops to be used if the capacity is increased to 50.

(OR)

(b) Design a 4 bit code converter which converts given binary code into a code in which the adjacent number differs by only 1 by the preceding number. Also develop VHDL coding for the above mentioned code converter.

MAY/JUNE 2016

PART – A (Answer All questions)

(10X2=20)

1. Convert the following binary code into a gray code 1010111000_2
2. Define fan in and fan out
3. Write the POS representation of the following SOP function $f(x,y,z) = \sum m(0,1,3,5,7)$
4. Design a Half subtractor
5. Give the characteristic function and equation of SR flip flop
6. State any 2 differences on Moorey and Mealy state machines
7. What are the 2 types of asynchronous sequential circuits.
8. State the differences between PROM, PLA and PAL
9. What is data flow modelling in VHDL. Give its basic mechanism
10. Write the VHDL code to realize 2X1 multiplexer.

PART – B (Answer any 2 questions)

(5X16=80)

11. (a) (i) Convert 1010111011101100_2 into its octal, decimal and hexa decimal equivalent.
(ii) Deduce the odd parity hamming code for the data 1010. Introduce an error in the LSB of the hamming code and deduce the steps to detect the error.
(OR)
- (b) (i) With circuit schematic explain the operation of 2 input TTL NAND gate.
(ii) With circuit schematic and explain the operation and characteristics of a ECL gate.
12. (a) (i) Simplify the following function using K-map $f(a,b,c,d) = \sum m(0,1,3,9,10,12,13,14) + \sum d(2,5,6,11)$
(ii) Implement the following function using only NAND gate $f(x,y,z) = \sum m(0,2,4,6)$
(OR)
- (b) (i) Design a BCD to Excess-3 code converter
(ii) Design a Full adder and implement using suitable multiplexer
13. (a) (i) Explain the operation of JK master slave flip flop.
(ii) Design a Mod – 5 counter using T flip flops
(OR)
- (b) (i) Design a serial adder using Mealy state model
(ii) Explain the state minimization using partitioning procedure with a suitable example.
14. (a) (i) What are Static – 0 and static – 1 hazards. Explain the removal of hazard using hazards cover in K- map
(ii) Explain cycles and races in asynchronous sequential circuits
(OR)
- (b) (i) What are transition table and flow table? Give suitable examples
(ii) Implement the following function using PLA and PAL $f(x,y,z) = \sum m(0,1,3,5,7)$
15. (a) (i) Explain the various operators supported by VHDL
(ii) Write the VHDL code to realize a decade counter with behavioural modelling
(OR)
- (b) (i) Explain functions and subprograms with suitable examples
(ii) Write the VHDL code to realize the 4 bit parallel binary adder with structural modelling and write the test bench to verify its functionality

NOV/DEC 2015

PART – A (Answer All questions)

(10X2=20)

1. What is a unit distance code? Give an example
2. Define fan out
3. Convert the given expression in canonical SOP form $Y = AB + A'C + BC'$
4. Draw the logical diagram of X-OR gate using NAND gates
5. Draw the truth table and state diagram of SR flip flop
6. What is edge triggered flip flop?
7. What is PROM?
8. Compare pulsed mode and fundamental mode asynchronous circuit.
9. Write the behavioural model of D – Flip flop
10. List out the operators present in VHDL.

PART – B (Answer any 2 questions)

(5X16=80)

11. (a) (i) Draw the CMOS logic circuit for NOR gate and explain its operation
(ii) Perform the following operation $(756)_8 - (437)_8 + (725)_{16}$. Express the answer in octal form
(OR)
- (b) (i) A 12 bit hamming code word containing 8 bits of data and 4 parity bits is read from memory. What was the original 8 bit data word that was written into memory if the 12 bit word read out is as (1) 101110010100 (2) 111111110100
(ii) Briefly discuss weighted binary code.
12. (a) (i) Simplify the boolean function using K- map and implement using only NAND gates.
 $f(a,b,c,d) = \sum m(0,8,11,12,15) + \sum d(1,2,4,7,10,14)$. mark the essential and non-essential prime implicants

(ii) Design a full subtractor and implement using logic gates.

(OR)

(b)(i) Design a 4 – bit BCD to excess – 3 code converter and implement using logic gates

(ii) What is a multiplexer? Implement the following boolean function with 8X1 MUX and external gates $f(a,b,c,d) = \sum m(1,3,4,11,12,13,14,15)$

13. (a) (i) A sequential circuit with 2 D- flip flops A and B, input X and output Y is specified by the following next state and output equations. $A(t+1) = Ax + Bx$, $B(t+1) = A'x$
 $Y = (A+B)x'$, draw the logic diagram, derive the state table and state diagram

(ii) Realise the T-flip flop using JK flip flop.

(OR)

(b) (i) Design a synchronous decade counter using T flip flop and construct the timing diagram

(ii) Design a Mealey model of sequence detector to detect the pattern 1001

14. (a) Design an asynchronous sequential circuit (with detailed steps involved) that has 2 inputs x_1 and x_2 and one output z. The circuit is required to give an output $z=1$ when $x_1=1$, $x_2=1$ and $x_1=1$ being first.

(OR)

(b) Show how to program the fusible links to get a 4 bit Gray code from the binary inputs using PLA and PAL and compare the design requirements with PROM.

15. (a) (i) Write a VHDL program for 1 to 4 Demux using dataflow modelling.

(ii) Write a VHDL program for full adder using structural modelling.

(OR)

(b) Explain in detail the RTL design procedure.

MAY/JUNE 2015

PART – A (Answer All questions)

(10X2=20)

- Convert (a) $(475.25)_8$ to its decimal equivalent. (b) $(549.B4)_{16}$ to its binary equivalent.
- Define propagation delay.
- Convert the given expression in canonical SOP form $Y = AC + AB + BC$
- Simplify the expression $Z = AB + AB'((A'.C)')$.
- Convert T Flip Flop to D Flip Flop.
- State the rules for state assignment.
- State the difference between static 0 and static 1 hazard.
- What is a PROM?
- What is a package in VHDL?
- Write the behavioural modeling code for a D Flip Flop.

PART – B (Answer any 2 questions)

(5X16=80)

11. (a) (i) Perform the following addition using BCD and Excess-3 addition (205+569).
(ii) Encode the binary word 1011 into seven bit even parity Hamming code.

(OR)

(b) (i) With circuit schematic explain the operation of 2 input TTL NAND gate with totem-pole output.

(ii) Compare totem pole and open collector outputs..

12. (a) (i) Reduce the following function using K-map $f(a,b,c,d) = \sum m(0,2,3,8,9,12,13,15)$
(ii) Implement the following function using only NAND gate $f(x,y,z) = \sum m(0,2,4,6)$

(OR)

(b) (i) Design a BCD to Excess-3 code converter

(ii) Implement the following Boolean function using 8:1 multiplexer

$$f(a,b,c,d) = \sum m(0,1,3,4,8,9,15)$$

13. (a) (i) Explain the operation of JK master slave flip flop.
 (ii) Design a 3 bit bidirectional shift register
(OR)
- (b) (i) Design a Mod 5 synchronous counter using JK flip-flops.
 (ii) Design a sequence detector to detect the sequence 101 using JK flip flop.
14. (a) Design an asynchronous sequential circuit that has two inputs X_2 and X_1 and one output Z . when $X_1 = 0$, the output Z is 0. The first change in X_2 that occurs while X_1 is 1 will cause output Z to be 1. The output Z will remain 1 until X_1 returns to 0.
(OR)
- (b) (i) Implement the following function using PLA $f(x,y,z) = \sum m(1,2,4,6)$
 (ii) For the given boolean function, obtain the hazard free circuit
 $f(a,b,c,d) = \sum m(1,3,6,7,13,15)$
15. (a) Write the VHDL code to realize a full adder using
 (i) Behavioural modelling
 (ii) Structural modelling
(OR)
- (b) (i) Write the VHDL code to realize a 3 bit Gray code counter using case statement.

NOV/DEC 2014

PART – A (Answer All questions) (10X2=20)

1. Determine $(377)_{10}$ in octal and hexa decimal equivalent
2. Compare the totem pole output with open collector output
3. Given $F = B' + A'B + A'C'$: Identify the redundant term using K-map.
4. Give one application each for multiplexer and decoder.
5. Show how the JK flip flop can be modified into a D flip flop or a T Flip flop
6. Differentiate between Mealy and Moore models
7. What is a deadlock condition?
8. Draw the block diagram of PLA
9. Write a VHDL code for 2 X 1 MUX
10. State the advantages of package declaration over component declaration.

PART – B (Answer any 2 questions) (5X16=80)

11. (a) (i) Given that a frame with bit sequence 1101011011 is transmitted, it has been received as 1101011010. Determine the method of detecting the error using any one error detecting code.
 (ii) Draw the MOS logic circuit for NOT gate and explain its operation
(OR)
- (b) (i) Explain Hanning code with an example. State its advantages over parity code
 (ii) Design a TTL logic circuit for a 3 – input NAND gate.
12. (a) (i) Minimize the function $F(a,b,c,d) = \sum m(0,4,6,8,9,10,12)$ with $\sum d(2,13)$. Implement the function using only NOR gates.
 (ii) Design a full subtractor and implement it using logic gates
(OR)
- (b) (i) Implement the function $F(p,q,r,s) = \sum m(0,1,2,4,7,10,11,12)$ using decoder.
 (ii) Design a 4 bit binary to gray code converter and implement it using logic gates.
(OR)
13. (a) (i) Design an asynchronous modulus – 8 down counter using JK flip flop
 (ii) Explain the circuit of a SR flip flop and explain its operation.
(OR)
- (b) (i) Design synchronous sequential circuit that goes through the count sequence 1,3,4,5 repeatedly. Use T flip flop for your design
 (ii) Explain the various types of triggering with suitable diagrams. Compare their merits and demerits
14. (a) Explain the various types of hazards in sequential circuit design and the methods to eliminate them. Give suitable examples.

(OR)

- (b) Describe the reasons, the effect of races in asynchronous sequential circuit design. Explain its types with illustrations. Show the method of race-free state assignments with examples
15. (a) (i) Explain the digital system design flow sequence with the help of a flow chart.
 (ii) Write a VHDL code for a 4-bit universal shift register

(OR)

- (b) Explain the concept of behavioural modelling and structural modeling in VHDL. Take the example of full adder design for both and write the coding.

MAY/JUNE 2014

PART – A (Answer All questions)

(10X2=20)

1. State Demorgan's theorem
2. Simplify $F = ABC + AB'C + A'C + AB'$
3. Design a half subtractor.
4. Realize the following function using NOR gates only $F = A'B + AB'$
5. Convert D flip flop into T flip flop
6. What is an incompletely specified circuit?
7. What are the two types of asynchronous sequential circuits?
8. What is a merger diagram? Give example.
9. Define Noise Margin.
10. Define propagation delay.

PART – B (Answer any 2 questions)

(5X16=80)

11. (a) (i) Prove that $(X+Y)(X+Y') = X$ using truth table method (4)
 (ii) State and prove consensus theorem (4)
 (iii) Convert all 4-bit binary numbers to excess 3 numbers (8)

(OR)

- (b) (i) Simplify the following functions $z = \sum m(0,3,6,9) + \sum d(10,11,12,13,14,15)$ (8)
 (ii) Minimize the following functions using Quine Mcclusky method
 $f(a,b,c,d) = \sum m(0,1,2,5,6,7,8,9,10,14)$ (8)

12. (a) (i) Simplify the following functions and implement it using only two OR gates and two AND gates $F = (V+W+Z)(V+X+Y)(V+Z)$ (8)
 (ii) Implement the function using only NAND gates $F = a'(b'+c(d+e'))+f'g'+hi'j+k$ (8)

(OR)

- (b) (i) Design a BCD to 7 segment decoder (10)
 (ii) Implement the function using suitable multiplexer $f = \sum m(0,1,3,5,9,10,11,12)$ (6)
13. (a) (i) What is a race around condition? How it is avoided in master slave JK flip flops (8)
 (ii) Give the state assignment guidelines. Apply the state assignment guidelines for the following state machine. (8)

Present State	Next state		Output	
A	a	c	0	0
B	d	f	0	1
C	c	a	0	0
D	d	b	0	1
E	b	f	1	0
F	c	e	1	0

(OR)

- (b) (i) Design a 3-bit synchronous updown counter (8)
 (ii) Design a sequence detector to detect the sequence 101 (8)
14. (a) For the given flow table
 (i) Find all critical races and justify why they are critical (6)
 (ii) Find all non-critical races (5)
 (iii) Find all cycles (5)

Present State	Next State X_1X_2				Output Z			
	00	01	11	10	00	01	11	10
00	a)	c	b	c	0	0	0	0
01	c	b)	b)	d	1	0	1	0
11	d	c)	b	d	0	1	0	0
10	c	d)	b	d)	1	1	0	0

(b) Design an asynchronous network that has two inputs and one output. The input sequence $X_1 X_2 = 00, 01, 11$ causes the output to become 1. The next input change then causes the output to return to 0. No other input sequence will produce a 1 output.

15. (a) (i) Write a note on static and dynamic RAM
(ii) Design a Full adder and implement it using a suitable PAL
(OR)

- (b) (i) Explain the operation of a two input TTL NAND gate.
(ii) Write a note on FPGA.

NOV/DEC 2013

PART – A (Answer All questions) (10X2=20)

- What is hamming code?
- What are redundant prime implicants?
- How the decoder is used as a demultiplexer?
- Implement the function $F = A .B$ using NOR gates.
- How many flip flops are required to build a binary counter that counts from 0 to 128?
- Why is state reduction necessary?
- What is primitive flow table?
- State the advantages of totem pole input.
- What is memory expansion?
- Define cycle in asynchronous circuits.

PART – B (Answer any 2 questions) (5X16=80)

11. (a) (i) Convert the function $f(A, B, C) = (A + \bar{B} + C)(\bar{A} + B + \bar{C})$ into standard SOP. (5)
(ii) The Hamming code 101101101 is received. Correct it if any errors. There are four parity bits and odd parity is used. (5)
(iii) Convert the following $(61.3)_{10} = ()_2, (37.29)_{10} = ()_8, (101011)_2 = \text{Gray code}$ (6)
(OR)

(b) Determine the essential prime implicants of the following function and verify using the following and verify using k-map $f = \sum m(3,4,5,7,9,13,14,15) + \sum d(0,1)$ (16)

12. (a) (i) Compare serial and parallel adder (6)
(ii) Implement the following multiple output function using decoder and logic gates
 $f_1(A, B, C) = \sum m(1,4,5,7), f_2(A, B, C) = \pi M(2,3,6,7)$

(10)

(OR)

- (b) (i) Convert a Binary to BCD code converter using full address (10)

(ii) Design a combinational logic circuit with 3 input variables that will produce logic 1 output when more than one input variables are logic 1 (6)

13. (a) (i) Draw and explain the working of 4 bit *up/down* synchronous counter (12)
(ii) Give the excitation table for T- flip flop (4)

(OR)

- (b) (i) Design a synchronous counter with states 0, 1, 2, 3, 4, 5, 0, 1... using JK ff's (12)
(ii) Explain the concept of Bidirectional shift register (4)

14. (a) Design a T –Flip Flop from logic gates (16)

(OR)

- (b) (i) An asynchronous sequential circuit is described by the following excitation and

output functions

$$Y = X_1 X_2 + (X_1 + X_2)Y$$

$$Z = Y$$

- a. Draw the logic diagram of the circuit
 - b. Derive the transition table and the output map
 - c. Describe the behaviour of the circuit (10)
- (a) (i) Design a BCD to Excess – 3 code converter and implement using suitable PLA(10)
- (ii) Give the classification of semiconductor memory (6)
- (OR)**
- (b) (i) Draw and explain the circuit for tri-state TTL inverter (10)
- (ii) Give the characteristics of ECL family (6)

MAY/JUNE 2013

PART – A (Answer All questions) (10X2=20)

1. What are cyclic codes?
2. Simplify the function $Y = \sum m(1,3,5,7)$
3. Implement the equation $Y = \overline{BC} + \overline{AB} + AD$ using only NAND gates
4. Write the truth table of a half adder
5. What do you mean by completely specified and incompletely specified function?
6. List the applications of shift registers
7. What is the use a merger graph
8. Define Races
9. What are the uses of a buffer?
10. A certain gate draws 1.8mA when its output is high and 3.2mA when its output is low. What is the average power dissipation if Vcc is 5V and it is operated on a 50% duty cycle

PART – B (Answer any 2 questions) (5X16=80)

11. (a) (i) Perform the excess – 3 addition of 8 and 6 [4]
- (ii) Convert $(11001011.01101)_2$ into decimal [4]
- (iii) Convert the gray code 101011 into its binary equivalent [4]
- (iv) Convert the expression $A+BC$ in standard product of sum form [4]
- (OR)**
- (b) Reduce the Boolean function $f(A,B,C,D) = \pi M(0,2,3,8,9,12,13,15)$ using K – map and Quine Mcclusky method [16]
12. (a) (i) Implement the function using suitable multiplexer $F(A,B,C) = \sum m(1,3,5,6)$ [8]
- (ii) Design a full subtractor with half subtractors [8]
- (OR)**
- (b) (i) Design a code converter for BCD to gray code conversion [10]
- (ii) Explain how the demultiplexer used as a decoder [6]
13. (a) (i) Explain the Johnson counter (4 bit) with neat diagram [10]
- (ii) Realize the SR flip flop using D flip flop [6]
- (OR)**
- (b) Design a 4 bit up/down ripple counter with a control for up/down counting [16]
14. (a) Design a pulse mode circuit having two input lines x_1 and x_2 and output line Z. the circuit should produce an output pulse to coincide with the last input pulse in the sequence $x_1 - x_2 - x_2$. No other input sequence should produce an output pulse. [16]
- (OR)**
- (b) Design an asynchronous sequential circuit that has the inputs X_1 and X_2 and one output Z. when $X_1 = 0$, the output Z is 0. The first change in X_2 that occurs while X_1 is 1 will cause output Z to be 1. The output Z will remain 1 until X_1 returns to 0. [16]
15. (a) (i) Compare PROM, PLA and PAL [8]
- (ii) Design a switching circuit that converts a 4 bit binary code into a 4 bit gray code using ROM array [8]
- (OR)**
- (b) (i) Explain the operation of ECL NOR/OR gate with neat sketch [10]
- (ii) Write the characteristics of ECL family [6]

NOV/DEC 2012

PART – A (Answer All questions)

(10X2=20)

- 1.State and prove Distributive laws
- 2.What are weighed binary codes? Give two examples.
- 3.Realise the logic expression $Y = \overline{AB} + A + (B + C)$ using NAND gates
- 4.What is the function of a multiplexers select inputs?
- 5.Draw the block diagram to realise J- K flip flop using S-R flip flop
- 6.What is a ripple counter? State the drawbacks of ripple counter.
- 7.What is meant by fusible link? How many types of fuse technologies are used in PROM?
- 8.Draw the logic circuit for CMOS NAND gate
- 9.Define the races in asynchronous sequential circuits
10. Differentiate stable and unstable states.

PART – B (Answer any 2 questions)

(5X16=80)

11. (a) (i) Convert the following numbers (8)
 - (1) $(A3B)_{16} = ()_{10}$
 - (2) $(444.456)_{10} = ()_8$
 - (3) $(59.58)_8 = ()_2$
 - (4) $(4097.188)_{10} = ()_2$

(ii) Obtain the canonical form sum of product and product of sum of the following expression $A+AB+BC$ (8)

(OR)

(b) (i) Encode data bits 1101 into a 7 – bit even parity Hamming code (8)

(ii) Explain prime implicants minterms, maxterms, essential prime implicants (8)
12. (a) (i) Draw the logic diagram of IC 74138 and explain the operation with truth table(10)

(ii) Design a full adder circuit using only NOR gates (6)

(OR)

(b) (i) List the applications of magnitude comparator and multiplexer (6)

(ii) Design a code converter that converts a BCD into excess – 3 code

13. (a) Design a synchronous MOD – 10 counter using J-K flip flop (16)

(OR)

(b) (i) Describe the parallel in serial out shift register with neat logic diagram (8)

(ii) Explain the function of J-K flip flop using a suitable diagram and discuss how does it differ from S-R flip flop (8)
14. (a) (i) Design an asynchronous circuit that has two inputs x_1 and x_2 and one single output z . The circuit is required to give an output whenever the input sequence 00, 10, 11 and 01 are received but only in that order. (12)

(ii) Write short notes on Hazards (4)

(OR)

(b) (i) Discuss the procedural steps for implication table and merging of the flow table.(12)

(ii) Briefly comment on Races and their implication. (4)

15. (a) (i) Explain the formation of inverter using CMOS and its operation (8)

(ii) Discuss the characteristics of Emitter Coupled Logic Circuit (8)

(OR)

(b) (i) Design a combinational circuit that accepts a 3-bit number as input and generates an output binary number equal to the square of the input number using ROM(10)

(ii) Explain the steps involved in programming of FPGA (6)

MAY/JUNE 2012

PART – A (Answer All questions)

(10X2=20)

1. What is the value of ‘b’ if $\sqrt{41_b} = 5$?
2. List the advantage of Karnaugh map.
3. Draw a 4X16 decoder constructed with two 3 X 8 decoders
4. Give the differences between DMUX and MUX
5. Show how a RSFF can be built using NAND gate

6. What is a ripple counter
7. List the advantages of SM chart
8. Differentiate : Synchronous and Asynchronous sequential circuits
9. Mention the applications of PLA
10. What can happen if TTL output is connected to more unit loads that its output rating specifications?

PART – B (Answer any 2 questions) (5X16=80)

11. (a) Obtain the minimum SOP using Quine McClusky's method and verify using K map

$$F = m_0 + m_2 + m_4 + m_8 + m_9 + m_{10} + m_{11} + m_{12} + m_{13}$$

(OR)

 (b) Reduce the following using tabulation method

$$F = m_2 + m_3 + m_4 + m_6 + m_7 + m_9 + m_{11} + m_{13}$$
12. (a) Design and construct an eight input priority encoder

(OR)

 (b) (i) Design the logic so an active low output is generated when power is on (an active high signal), the system is not reset (an active low signal), an interlock is closed (an active low signal), a run signal is present (active low) and data are ready (active high)
 (ii) Design a combinational circuit that will multiply two 2 bit binary values
13. (a) Design a sequential circuit with 4 FF ABCD. The next state of B, C, D are equal to the present states of A, B, C. the next state of A is equal to the ex-OR of the present states of C and D.

(OR)

 (b) Design a counter with the sequence 0, 1, 3, 7, 6, 4, 0
14. (a) (i) How do you identify and eliminate static and dynamic hazards from an asynchronous sequential circuit? Explain
 (ii) Find whether static 'O' hazard does not exist in implementing the Boolean expression: $Y = x_1x_3 + x_1x_2x_3 + \overline{x_2x_3}$. If exists, then find the static hazards present

(OR)

 (b) Construct a Mealey state diagram that will detect a serial input sequence of 10110. The detection of the required bit pattern can occur in a longer data string and the correct pattern can overlap with another pattern. When the input pattern has been detected, cause an output 'Z' to be asserted high
15. (a) Using the NOR outputs of two ECL gates, show that when connected together to an external resistor and negative supply voltage, the wired connection produces an 'OR' function
 (b) Write detailed notes on the following
 - a. FPGA
 - b. PROM
 - c. CMOS technology

APR/MAY 2011

PART – A (Answer All questions) (10X2=20)

1. Convert $(108.2)_{10}$ and $(10110.110)_2$ into hexadecimal numbers.
2. Simplify $X\overline{Y} + ZX\overline{Y}$
3. What is positive logic system? Give an example.
4. Give the truth table of EX-OR gate. Give an example for EX-OR gate.
5. State an application each for D and T flip flop
6. State the difference between combinational and sequential circuits
7. What is a pulse mode circuit?
8. What is a Moore machine?
9. Give the fan – in, fan – out and noise margin range of a TTL family NAND gate.
10. What is EPROM?

PART – B (Answer any 2 questions) (5X16=80)

11. (a) (i) State and prove Demorgan's theorem [10]
(ii) Simplify the following using K-map

$$F = \pi M(0,1,3,6,8,9,11,15)$$
 [6]
(OR)
(b) Simplify the following using Quine – McClusky method. Realize the reduced function using NAND gates. $F = \sum m(0,2,3,4,7,8,11,12,13) + \sum d(5,6)$ [16]
12. (a) Design the following circuits of Full Adder and Magnitude Comparator [16]
(OR)
(b) Design the following circuits of Subtractor and M to 1 multiplier [16]
13. (a) Define the following:
1. Completely specified sequential circuits and incompletely specified sequential circuits [4]
2. Discuss the working of serial in parallel out 4 bit shift register with an example and a timing diagram [12]
(OR)
(b) Explain the working of Up down counter and Johnson Counter [16]
14. (a) Design a two input (x_1, x_2), two output (z_1, z_2) fundamental circuit that has the following specifications. When $x_1x_2 = 00$, $z_1z_2 = 00$. The output 10 will be produced following the occurrence of the input sequence 00 – 01 – 11. The output will remain 10 until the input returns to 00, at which time it becomes 00. An output of 01 will be produced following the receipt of the input sequence 00 -10 -11. And once again, the output will remain 01 until occurs, which returns the output to 00. [16]
(OR)
(b) Design a pulse mode circuit having two input lines x_1 and x_2 and output line Z. the circuit should produce an output pulse to coincide with the last input pulse in the sequence $x_1 - x_2 - x_2$. No other input sequence should produce an output pulse. [16]
15. (a) (i) Explain the working of two input NOR gates. [8]
(ii) Compare ECL and CMOS logic families [8]
(OR)
(b) (i) Explain the working of three input TTL NAND totem pole output gate [10]
(ii) Write notes on PLA. [6]

NOV/DEC 2011

PART – A (Answer All questions) (10X2=20)

1. What is meant by even parity and odd parity?
2. Simplify the expression $\overline{ABC} + BC + AC$
3. Write the truth table of universal gates.
4. Identify the MSI devices 74157 and 74150
5. Write the rules for the state assignment in a synchronous sequential circuits
6. Draw the 3 – bit shift register circuit.
7. Differentiate synchronous and asynchronous sequential circuits.
8. What are the different types of hazards in asynchronous circuits.
9. List the applications of PLA
10. Define fan in and fan out.

PART – B (Answer All questions) (5X16=80)

11. (a) (i) Convert the following numbers to their decimal equivalents [6]
1. BC_{216}
2. 11011.011_2
(ii) Simplify $Y = \sum m(0,2,6,10,11,12)$ using Quine McClusky method [10]
(OR)
(b) (i) Express the function $Y = AB + \overline{BC} + \overline{AC}$ in canonical sum of product form. [6]
(ii) Simplify the expression $Y = \sum m(3,4,6,7,8,9,10,13,14,15)$ using K-map [10]

12. (a) (i) Design a 4 bit comparator using logic gates. [10]
(ii) Realize $Y = A + B\overline{C}\overline{D}$ using NAND gate [6]
(OR)
(b) (i) Implement the full subtractor using demultiplexer [6]
(ii) Design a circuit for BCD to seven segment code convertor [10]
13. (a) (i) Derive the excitation table for the JK flip flop and D flip flop. Also describe the parallel in parallel out and serial in serial out shift register [10]
(ii) Explain the operation of Johnson counter with suitable timing diagram. [6]
(OR) (b) Design a MOD 13 counter [16]
14. (a) Design an asynchronous sequential circuit that has the inputs X_1 and X_2 and one output Z . when $X_1 = 0$, the output Z is 0. The first change in X_2 that occurs while X_1 is 1 will cause output Z to be 1. The output Z will remain 1 until X_1 returns to 0. [16]
(OR)
(b) Discuss the problems in asynchronous circuits.
15. (a) Explain the two input NAND and NOR gate using transistor logic with neat diagrams.
(OR)
(b) (i) What is a RAM? Draw and explain the circuit of a typical cell of bipolar RAM.
(ii) Explain the steps involved in programming of FPGA.

NOV/DEC 2010

PART – A (Answer All questions) (10X2=20)

1. What is the decimal equivalent of $(8963)_{16}$?
2. State the DeMorgan's theorem and absorption theorem in Boolean algebra.
3. What is the use of enable signal?
4. Compare half adder and full adder.
5. What is the drawback in RS flip flop?
6. Why is state reduction necessary?
7. What are asynchronous sequential circuits?
8. What is triggering of flip flops?
9. What is PLA? What are its uses?
10. Compare TTL, ECL, CMOS families for switching speed.

PART – B (Answer All questions) (5X16=80)

11. (a) (i) Prove that $\overline{AB} + \overline{A} + AB = 0$ [4]
(ii) Reduce the following expression using K – map and implement using NOR gates
 $F = \sum 0,1,2,3,4,6,8,9,10,11$ [12]
(OR)
b(i) Why do we need many number systems in computer systems [4]
(ii) Reduce the following function after identifying the essential and non essential prime implicants.
 $F = A'B'C'D' + A'B'C'D + A'B'CD + A'BC'D' + A'BC'D + A'BCD$ [12]
12. (a) (i) Show how a full subtractor can be built from two half subtractor [8]
(i) Design a BCD to gray code converter [8]
(OR)
(b) (i) Implement the function $F(A, B, C, D) = \sum 1,3,5,6$ using MUX [6]
(ii) Design a 4 bit carry look ahead adder using gates [10]
13. (a) (i) Design a synchronous 3 bit up/down counter with a gray code sequence. The counter should count up when up/down control input is 1 and count down when the control input is 0 [10]
(ii) Draw SISO shift register circuit using D flip flop [6]
(OR)
(b) Design a counter with the following sequence 0, 1, 3, 2, 6, 4, 5, 7 and repeat using RS flip flop [16]

14. (a) (i) Distinguish between truth table and excitation table. Show how one can be obtained from another with an example [5]
(ii) Design a BCD ripple counter [11]
(b) Develop the state diagram and primitive row flow table for a logic system that has two inputs S and R and a single output Q. the device is to be an edge triggered SR flip flop but without a clock. The device changes state on the rising edge of the two inputs. Static input values are not to have any effect in changing the Q input. [16]
15. (a) Design the circuit using all the Programmable logic device
 $Q(K, L, M, N) = \sum 1,3,6,9,11,1,2,14$ [16]
(b) Describe the characteristics and implementation of [16]
1. TTL
2. CMOS

APR/MAY 2010

PART – A (Answer All questions)

(10X2=20)

1. State Demorgan's theorem
2. What is prime implicant?
3. Design a half subtractor.
4. Implement the following function using only NAND gates $F = (x + y) z$.
5. Convert SR flip flop to D flip flop
6. Define Equivalent state
7. What are the two types of Asynchronous sequential circuits
8. What are races? How can it be avoided?
9. Implement the following using a suitable PROM $F = \sum m(0,1,2)$
10. List any two advantages of ECL family

PART – B (Answer All questions)

(5X16=80)

11. (a) (i) Convert the following binary number to Decimal, Hexadecimal and Octal form.
 $(11011011.100101)_2$ [12]
(ii) Encode the binary word 1011 into seven bit even parity Hamming code [4]

(OR)

- (b) (i) Add the following hexadecimal numbers $(4FB)_{16}$, $(75D)_{16}$, $(A12)_{16}$ and $(C39)_{16}$ [8]
(ii) Minimize the expression:
 $Y = \overline{A}BCD + \overline{A}BC\overline{D} + A\overline{B}CD + \overline{A}\overline{B}CD + A\overline{B}C\overline{D} + \overline{A}B\overline{C}D$ [8]

12. (a) (i) Design a Full adder and realize it using NOR gates [8]
(ii) Design a 2-bit Magnitude comparator to compare two bit numbers [8]

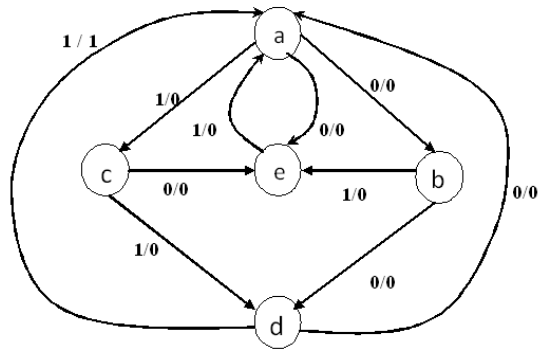
(OR)

- (b) (i) Design a 4-bit binary to Gray code converter [10]
(ii) Implement the following function using a suitable multiplexer
 $F(A, B, C, D) = \sum m(0,1,3,5,6,7,10,12,14)$ [6]

13. (a) (i) Compare synchronous and asynchronous sequential circuits [4]
(ii) Design and explain the operation of four bit synchronous binary counter [12]

(OR)

- (b) Design a sequential circuit for a state diagram shown in the following figure. Use state assignment rules for assigning states and compare the required combinational circuit with straight binary assignment [16]



14. (a) An asynchronous sequential circuit is described by the following excitation and output functions

$$Y = X_1 X_2 + (X_1 + X_2) Y$$

$$Z = Y$$

- Draw the logic diagram of the circuit [4]
- Derive the transition table and the output map [8]
- Describe the behavior of the circuit [4]

(OR)

(b) An asynchronous circuit has two internal states and one output. The excitation and output function describing the circuit are as follows

$$Y = x_1 x_2 + x_1 y_2 + x_2 y_1 \quad [4]$$

$$Y = x_2 + x_1 y_1 y_2 + x_1 y_1 \quad [8]$$

$$Z = x_2 + y_1 \quad [4]$$

- Draw the logic diagram of the circuit
- Derive the transition table and the output map
- Describe the behavior of the circuit

15. (a) (i) With an example, explain the following programmable logic devices [5+5+6]

- PROM
- PAL
- PLA

(OR)

(b) Explain the following characteristics of CMOS [16]

- Operating speed
- Voltage levels and noise margin
- Fan – out
- Power dissipation
- Propagation delay
- Latch up
- Unused inputs
- Static charge susceptibility