JEPPIAAR ENGINEERING COLLEGE

Jeppiaar Nagar, Rajiv Gandhi Salai – 600 119

DEPARTMENT OF

ELECTRONICS AND COMMUNICATION ENGINEERING

QUESTION BANK

VI SEMESTER

CS6303 – COMPUTER ARCHITECTURE

Regulation – 2013(Batch: 2015 -2019)

Academic Year 2017 – 18

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SUBJECT : CS6303– COMPUTER ARCHITECTURE

YEAR /SEM: III /VI

UNIT I OVERVIEW AND INSTRUCTIONS				
Eight ideas – Components of a computer system – Technology – Performance – Power wall – Uniprocessors to multiprocessors; Instructions – operations and operands – representing instructions – Logical operations – control operations – Addressing and addressing modes.				
PART – A				
CO Mapping : C310.1				
Q.No	**Questions**	**BT Level**	**Competence**	**PO**
1	**List the major components of a computer system.**	BTL-1	Remembering	PO1,PO3
2	**Define addressing modes and its various types.**	BTL-1	Remembering	PO1,PO2,PO3
3	**What is indirect addressing mode?**	BTL-1	Remembering	PO1,PO2
4	**Define ALU. What are the various operations performed in ALU?**	BTL-1	Remembering	PO1,PO2
5	**How to represent instruction in a computer system?**	BTL-2	Understanding	PO1,PO3
6	**What is auto increment and auto decrement addressing mode?**	BTL-1	Remembering	PO1,PO4
7	**What are the eight ideas in computer architecture?**	BTL-1	Remembering	PO1,PO2
8	**Distinguish pipelining from parallelism.**	BTL-2	Understanding	PO1,PO2,PO3
9	**Define Relative mode addressing.**	BTL-1	Remembering	PO1
10	**State Amdahl's Law.**	BTL-1	Remembering	PO1,PO3
11	**Define Little Endian arrangement.**	BTL-1	Remembering	PO1
12	**Define multiprogramming**	BTL-1	Remembering	PO1
13	**What is a bus? What are the different buses in a CPU?**	BTL-1	Remembering	PO1,PO2,PO3
14	**What is meant by MAR and MDR?**	BTL-1	Remembering	PO1,PO2
15	**What is meant by stored program concepts?**	BTL-2	Understanding	PO1,PO2

16	**What is meant by VLSI technology?**	**BTL-1**	**Remembering**	**PO1,PO3**
17	**Define multiprocessing**	**BTL-1**	**Remembering**	**PO2,PO4**
18	**Define power wall.**	**BTL-1**	**Remembering**	**PO1,PO3**
19	**What is uniprocessor?**	**BTL-1**	**Remembering**	**PO1,PO2**
20	**What is multicore processor?**	**BTL-1**	**Remembering**	**PO1,PO2**
21	**Differentiate between minicomputer and microcomputer.**	**BTL-2**	**Understanding**	**PO1,PO2,PO3**
22	**What is workstation?**	**BTL-1**	**Remembering**	**PO1,PO2**
23	**What is instruction register?**	**BTL-1**	**Remembering**	**PO1,PO2,PO3**
24	**What is program counter?**	**BTL-1**	**Remembering**	**PO1,PO2**
25	**What is processor time?**	**BTL-1**	**Remembering**	**PO1,PO3**
26	**What are clock and clock cycles?**	**BTL-1**	**Remembering**	**PO1,PO2**
27	**Give the CPU performance equation.**	**BTL-1**	**Remembering**	**PO2,PO4**
28	**List out the methods used to improve system performance.**	**BTL-1**	**Remembering**	**PO1,PO3**
29	**Define register mode addressing.**	**BTL-1**	**Remembering**	**PO1,PO2**
30	**Define Based or Displacement mode addressing.**	**BTL-1**	**Remembering**	**PO1,PO2**
31	**Define immediate mode addressing.**	**BTL-1**	**Remembering**	**PO1,PO2,PO3**
	PART – B & C			
1	**Explain in detail the different Instruction types.Compare their merits and demerits.**	**BTL-2**	**Understanding**	**PO1,PO2,PO3**
2	**What are the various logical operations and explain the instructions supporting the logical operations?**	**BTL-2**	**Understanding**	**PO1,PO2**
3	**Define Addressing mode and explain the basic addressing modes with an example**	**BTL-1**	**Remembering**	**PO1,PO2,PO3**
4	**Explain the important measures of the performance of a computer and derive the basic performance equation.**	**BTL-1**	**Remembering**	**PO1,PO3,PO4**
5	**Explain the various components of computer System with neat diagram.**	**BTL-1**	**Remembering**	**PO3,PO4**
6	**Explain the ways to represent an instruction in a computer.**	**BTL-2**	**Understanding**	**PO2,PO3**
7	**Explain in detail about the eight ideas of computer architecture.**	**BTL-2**	**Understanding**	**PO1,PO2,PO3**
8	**Write a note on register direct, indirect and immediate addressing modes with examples.**	**BTL-2**	**Understanding**	**PO2,PO3**
9	**Consider three different processors P1,P2 and P3 executing the same instruction set. P1 has 4GHz clock rate and CPI of 1.5. P2 has 2.5GHz clock rate and CPI f 1. P3 has 4GHz clock rate and has CPI of 2.2.** **(a) Which Processor has highest performance**	**BTL-3**	**Applying**	**PO1,PO2,PO3 ,PO4**

	expressed in instruction per second? **(b) If the processors each execute a program in 10seconds, find the number of cycles and number of instructions.** **(c) Reducing the execution time by 30% leads to increase in 20% of the CPI. What is the clock rate needed to get this reduction?**			

UNIT II ARITHMETIC OPERATIONS				
ALU - Addition and subtraction – Multiplication – Division – Floating Point operations – Sub word parallelism.				
PART – A				
CO Mapping : C310.2				
Q.No	**Questions**	**BT Level**	**Competence**	**PO**
1	**Subtract $(11011)_2$-$(10011)_2$ using 2's complement.**	BTL-4	Analyzing	PO1,PO3,PO4
2	**Divide $(1001010)_2$ by $(1000)_2$**	BTL-4	Analyzing	PO1,PO2,PO4
3	**State the rule for floating point addition.**	BTL-1	Remembering	PO1,PO2
4	**Subtract $(11010)_2$-$(10000)_2$ using 1's complement and 2's complement method.(**	BTL-4	Analyzing	PO1,PO3,PO4
5	**What is Subword Parallelism?**	BTL-1	Remembering	PO1,PO2
6	**Write the Add/subtract rule for floating point numbers.**	BTL-2	Understanding	PO1,PO2
7	**How overflow occurs in subtraction?**	BTL-3	Applying	PO1,PO2
8	**What is half adder?**	BTL-1	Remembering	PO1,PO2
9	**What is full adder?**	BTL-1	Remembering	PO1,PO2
10	**What is signed binary?**	BTL-1	Remembering	PO1,PO3
11	**What is a carry look-ahead adder?**	BTL-1	Remembering	PO1,PO3
12	**Define Booth Algorithm.**	BTL-1	Remembering	PO1,PO3
13	**What are the main features of Booth's algorithm?**	BTL-1	Remembering	PO1,PO2,PO3
14	**Define Integer Division and give its rule.**	BTL-1	Remembering	PO1
15	**Define Truncation.**	BTL-1	Remembering	PO1
16	**Explain how Boolean subtraction is performed?**	BTL-2	Understanding	PO1
17	**Define Chopping.**	BTL-1	Remembering	PO2
18	**Define Von Neumann Rounding.**	BTL-1	Remembering	PO1
19	**How can we speed up the multiplication process?**	BTL-2	Understanding	PO1,PO2
20	**What is bit pair recoding? Give an example.**	BTL-2	Understanding	PO1,PO2
21	**What are the two methods of achieving the 2's complement?**	BTL-1	Remembering	PO1,PO2

22	**What is the advantage of using Booth algorithm?**	**BTL-1**	**Remembering**	**PO1,PO2**
23	**What is Carry Save addition?**	**BTL-1**	**Remembering**	**PO1,PO2,PO3**
24	**Write the algorithm for restoring division.**	**BTL-2**	**Understanding**	**PO1,PO2**
25	**Write the algorithm for non- restoring division.**	**BTL-2**	**Understanding**	**PO1**
26	**Give the IEEE standard for floating point numbers for single precision number.**	**BTL-1**	**Remembering**	**PO1,PO2,PO3 ,PO4**
27	**Give the IEEE standard for floating point numbers for double precision number.**	**BTL-1**	**Remembering**	**PO1,PO2,PO3 ,PO4**
28	**When can you say that a number is normalized?**	**BTL-2**	**Understanding**	**PO2,PO3**
29	**Write the multiply rule for floating point numbers.**	**BTL-2**	**Understanding**	**PO2,PO3,PO 4**
30	**What is guard bit?**	**BTL-1**	**Remembering**	**PO1,PO2**
31	**What are the ways to truncate the guard bits?**	**BTL-2**	**Understanding**	**PO1,PO2,PO3**
32	**What are generate and propagate function?**	**BTL-1**	**Remembering**	**PO1,PO2**
33	**What is excess-127 format?**	**BTL-1**	**Remembering**	**PO1,PO2**
34	**In floating point numbers when so you say that an underflow or overflow has occurred?**	**BTL-2**	**Understanding**	**PO1,PO2,PO3**
	PART – B & C			
1	**Add 0.5_{10} and -0.4375_{10} using floating point addition algorithm.**	**BTL-4**	**Analyzing**	**PO1,PO2,PO3 ,PO4**
2	**Explain restoring division technique with example.**	**BTL-1**	**Remembering**	**PO1,PO2,PO3**
3	**Explain the sequential version of Multiplication algorithm in detail with diagram and examples**	**BTL-1**	**Remembering**	**PO1,PO2,PO3**
4	**(i) Explain Non – restoring division technique with example.** **(ii) What is meant by sub word parallelism? Explain.**	**BTL-1**	**Remembering**	**PO1,PO2,PO4**
5	**Give the block diagram for a floating point adder and subtractor unit and discuss its operation.**	**BTL-2**	**Understanding**	**PO2,PO3,PO 4**
6	**Explain in detail about floating point addition with example.**	**BTL-2**	**Understanding**	**PO1,PO2,PO3**
7	**(i) Briefly explain Carry look ahead adder.** **(ii) Multiply the following pair of signed nos.using Booth's bit –pair recoding of the multiplier A=+13 (multiplicand) and b= -6(multiplier)**	**BTL-2** **BTL-4**	**Understanding** **Analyzing**	**PO1,PO2,PO3**
8	**Show the IEEE754 binary representation of the number -0.75_{10} in single and double precision.**	**BTL-4**	**Analyzing**	**PO2,PO3,PO 4**
9	**Brief on carry look ahead layer and booth multiplier in detail.**	**BTL-2**	**Understanding**	**PO1,PO2**

UNIT III PROCESSOR AND CONTROL UNIT

Basic MIPS implementation – Building data path – Control Implementation scheme – Pipelining – Pipelined data path and control – Handling Data hazards & Control hazards –Exceptions.

PART – A

CO Mapping : C310.3

Q.No	Questions	BT Level	Competence	PO
1	**Mention the types of pipelining.**	BTL-2	Understanding	PO1
2	**Mention the various phase in executing an instruction.**	BTL-2	Understanding	PO1,PO2,PO3
3	**Name the control signals required to perform arithmetic operations.**	BTL-1	Remembering	PO1,PO2
4	**What is meant by data hazard in pipelining?**	BTL-1	Remembering	PO1,PO3
5	**Define exception and interrupt**	BTL-1	Remembering	PO1
6	**What is pipelining?**	BTL-1	Remembering	PO1
7	**Why is branch prediction algorithm needed? Differentiate between the static and dynamic techniques.**	BTL-4	Analyzing	PO1,PO2
8	**What is precise exception in R-type instruction?**	BTL-1	Remembering	PO1,PO2
9	**Define processor cycle in pipelining.**	BTL-1	Remembering	PO1
10	**What is meant by pipeline bubble?**	BTL-1	Remembering	PO1
11	**What is pipeline register delay?**	BTL-1	Remembering	PO1
12	**What are the major characteristics of a pipeline?**	BTL-1	Remembering	PO1,PO2
13	**What is data path?**	BTL-1	Remembering	PO1,PO2,PO3
14	**What is a pipeline hazard and what are its types?**	BTL-1	Remembering	PO1
15	**What is Instruction or control hazard?**	BTL-1	Remembering	PO1
16	**Define structural hazards.**	BTL-1	Remembering	PO1
17	**What is side effect?**	BTL-2	Understanding	PO2
18	**What do you mean by branch penalty?**	BTL-1	Remembering	PO1
19	**What is branch folding?**	BTL-1	Remembering	PO1,PO2
20	**What do you mean by delayed branching?**	BTL-2	Understanding	PO1,PO2
21	**What is branch Target Address?**	BTL-1	Remembering	PO1,PO2
22	**Why pipelining is needed?**	BTL-4	Analyzing	PO1,PO2,PO3 ,PO4
23	**How do control instructions like branch, cause problems in a pipelined processor?**	BTL-5	Evaluating	PO1,PO2,PO3
24	**What is meant by super scalar processor?**	BTL-1	Remembering	PO1,PO2
25	**Define pipeline speedup.**	BTL-2	Understanding	PO1
26	**What is pipelined computer?**	BTL-1	Remembering	PO1,PO2
27	**List the various pipelined processors.**	BTL-1	Remembering	PO2
28	**Classify the pipeline computers.**	BTL-2	Understanding	PO2,PO3
29	**Define Pipeline speedup.**	BTL-1	Remembering	PO3,PO4
30	**What is Vectorizer?**	BTL-1	Remembering	PO2,PO3,PO 4
31	**Write down the expression for speedup factor in a pipelined architecture.**	BTL-2	Understanding	PO2,PO4
32	**What are the problems faced in instruction pipeline?**	BTL-2	Understanding	PO4
33	**What is meant by vectored interrupt?**	BTL-1	Remembering	PO3

	PART – B & C			
1	**Explain in detail about building a datapath**	BTL-1	Remembering	PO2,PO3,PO4
2	**Explain pipeline hazard in detail.**	BTL-1	Remembering	PO3,PO4
3	**(i) Explain the hazards caused by unconditional branching statements.** **(ii) Describe operand forwarding in a pipelined processor with diagram.**	BTL-2 BTL-2	Understanding Understanding	PO2,PO3
4	**Discuss the modified data path to accommodate pipelined executions with diagram.**	BTL-2	Understanding	PO2,PO4
5	**What is hazards? Explain the types of hazards.**	BTL-1	Remembering	PO2,PO3,PO4
6	**Explain pipelined datapath and its control.**	BTL-1	Remembering	PO2,PO3
7	**How exceptions are handled in MIPS?**	BTL-2	Understanding	PO2,PO3
8	**Describe the techniques for handling control hazard in pipelining.**	BTL-2	Understanding	PO1,PO2,PO3
9	**Write short notes on exception handling.**	BTL-1	Remembering	PO1,PO2
10	**Explain how the instruction pipeline works. What are the various situations where an instruction pipeline can stall? How it can be resolved?**	BTL-2	Understanding	PO1,PO2,PO3

UNIT IV PARALLELISM				
Instruction-level-parallelism – Parallel processing challenges – Flynn's classification – Hardware multithreading– Multicore processors.				
PART – A				
CO Mapping : C310.4				
Q.No	**Questions**	**BT Level**	**Competence**	**PO**
1	**What are Fine grained multithreading and Coarse grained multithreading?**	BTL-1	Remembering	PO1
2	**Define Strong scaling and weak scaling.**	BTL-1	Remembering	PO1,PO2,PO3
3	**What is Instruction level parallelism?**	BTL-1	Remembering	PO1,PO2
4	**Compare UMA and NUMA multiprocessors.**	BTL-2	Understanding	PO1
5	**Explain various types of Dependences in ILP.**	BTL-2	Understanding	PO1

6	What is multiprocessors? Mention the categories of multiprocessors?	BTL-1	Remembering	PO1
7	Define Static multiple issue and Dynamic multiple issue.	BTL-1	Remembering	PO1,PO2
8	What is Speculation?	BTL-1	Remembering	PO1,PO2
9	Define Use latency.	BTL-1	Remembering	PO1
10	What is Loop unrolling?	BTL-1	Remembering	PO1
11	Define Register renaming.	BTL-1	Remembering	PO1
12	What is Superscalar and Dynamic pipeline schedule?	BTL-1	Remembering	PO1
13	Define Commit unit.	BTL-1	Remembering	PO1,PO2,PO3
14	What is Reservation station?	BTL-1	Remembering	PO1
15	Define Reorder buffer	BTL-1	Remembering	PO1
16	Define Out of order execution.	BTL-1	Remembering	PO1
17	What is In order commit?	BTL-2	Understanding	PO2
18	Distinguish between shared memory multiprocessor and message-passing multiprocessor.	BTL-1	Remembering	PO1,PO2
19	Define Single Instruction, Single Data stream (SISD)	BTL-1	Remembering	PO1,PO2
20	Define Single Instruction, Multiple Data streams (SIMD) and Multiple Instruction, Single Data stream (MISD).	BTL-1	Remembering	PO1,PO2
21	Define Multiple Instruction, Multiple Data streams (MIMD) and Single program multiple data streams .	BTL-1	Remembering	PO1,PO2
22	Define multithreading.	BTL-1	Remembering	PO1,PO2
23	What is multiple issue? Write any two approaches.	BTL-2	Understanding	PO1,PO2,PO3
24	What is meant by speculation?	BTL-1	Remembering	PO1,PO2
25	Define – Static Multiple Issue	BTL-2	Understanding	PO1
26	Define – Issue Slots and Issue Packet	BTL-1	Remembering	PO1,PO2
27	What is meant by loop unrolling?	BTL-1	Remembering	PO1
28	What is meant by anti-dependence? How is it removed?	BTL-2	Understanding	PO2,PO4
29	What is the use of reservation station and reorder buffer?	BTL-1	Remembering	PO3,PO4
30	Define – VLIW	BTL-1	Remembering	PO2,PO3
31	Define Multicore processors.	BTL-1	Remembering	PO2
32	What are symmetric multi-core processor and asymmetric multi-core processor?	BTL-2	Understanding	PO3
	PART – B & C			
1	Explain in detail hardware Multithreading	BTL-1	Remembering	PO3,PO4
2	Discuss in detail about Flynn's classification.	BTL-1	Remembering	PO2,PO3
3	Explain Instruction level parallelism& challenges	BTL-1	Remembering	PO2,PO3

	of parallel processing.			
4	**Explain Multicore processors**	BTL-1	Remembering	PO3,PO4
5	**Explain challenges in parallel processing.**	BTL-1	Remembering	PO2,PO3
6	**Dwell on the concept of instruction level parallelism with examples.**	BTL-2	Understanding	PO2,PO3,PO4
7	**Write short note on:** **(i) SISD** **(ii) MIMD**	BTL-2	Understanding	PO2,PO4
8	**Discuss about Implicit and Explicit multithreading. Compare and contrast with fine grained and coarse grained multithreading.**	BTL-2	Understanding	PO2,PO3
9	**Dwell on shared memory multiprocessor architecture.**	BTL-2	Understanding	PO2,PO3

UNIT V MEMORY AND I/O SYSTEMS				
Memory hierarchy - Memory technologies – Cache basics – Measuring and improving cache performance - Virtual memory, TLBs - Input/output system, programmed I/O, DMA and interrupts, I/O processors.				
PART – A				
CO Mapping : C310.5				
Q.No	**Questions**	**BT Level**	**Competence**	**PO**
1	**How many total bits required for direct mapped cache with 16KB of data and 4-word blocks, assuming 32-bit address.**	BTL-4	Analyzing	PO1,PO3,PO4
2	**Define virtual memory.**	BTL-2	Understanding	PO1,PO2,PO3
3	**How does a processor handle an interrupt?**	BTL-1	Remembering	PO1,PO2
4	**Define memory interleaving.**	BTL-1	Remembering	PO1
5	**Define Memory Hierarchy.**	BTL-1	Remembering	PO1
6	**Point out how DMA can improve I/O speed.**	BTL-4	Analyzing	PO1,PO4
7	**What is principle of locality?**	BTL-1	Remembering	PO1,PO2
8	**Define temporal locality.**	BTL-1	Remembering	PO1,PO2
9	**Define spatial locality.**	BTL-3	Applying	PO1
10	**Define hit ratio.**	BTL-1	Remembering	PO1
11	**What is TLB? What is its significance?**	BTL-1	Remembering	PO1
12	**How cache memory is used to reduce the**	BTL-1	Remembering	PO1,PO2,PO3

	execution time?			
13	**In many computers the cache block size is in the range 32 to 128 bytes. What would be the main Advantages and disadvantages of making the size of the cache blocks larger or smaller?**	BTL-5	Evaluating	PO1,PO2,PO3 ,PO4
14	**What is the function of a TLB?**	BTL-1	Remembering	PO1
15	**Define locality of reference. What are its types?**	BTL-1	Remembering	PO1
16	**Define Hit and Miss?**	BTL-1	Remembering	PO1
17	**What is cache memory?**	BTL-2	Understanding	PO2
18	**What is Direct mapped cache?**	BTL-1	Remembering	PO1,PO2
19	**Define write through and write buffer.**	BTL-1	Remembering	PO1,PO2
20	**What is write-back?**	BTL-2	Understanding	PO1,PO2
21	**What is memory system?**	BTL-1	Remembering	PO1,PO2
22	**Give the classification of memory.**	BTL-1	Remembering	PO1,PO2
23	**What is Read Access Time?**	BTL-2	Understanding	PO1,PO2,PO3
24	**What is Serial Access Memory?**	BTL-2	Understanding	PO1,PO2
25	**Define Random Access Memory.**	BTL-2	Understanding	PO1
26	**What is Semi Random Access?**	BTL-1	Remembering	PO1,PO2
27	**What is the necessary of virtual memory?**	BTL-1	Remembering	PO1,PO3,PO4
28	**Distinguish between memory mapped I/O and I/O mapped I/O.**	BTL-2	Understanding	PO2,PO3
29	**What is SCSI?**	BTL-2	Understanding	PO1,PO2,PO4
30	**Define USB.**	BTL-1	Remembering	PO1,PO4
31	**What are the units of an interface?**	BTL-2	Understanding	PO1,PO2
32	**Distinguish between isolated and memory mapped I/O?**	BTL-1	Remembering	PO3,PO4
33	**What is the use of DMA?**	BTL-2	Understanding	PO2
34	**What is meant by vectored interrupt?**	BTL-2	Understanding	PO2
35	**Compare Static RAM and Dynamic RAM.**	BTL-1	Remembering	PO3,PO4
	PART – B & C			
1	**Discuss the various mapping schemes used in cache memory**	BTL-2	Understanding	PO2,PO3,PO 4
2	**Explain in detail about memory Technologies**	BTL-2	Understanding	PO2,PO3
3	**What is virtual memory? Explain the steps involved in virtual memory address translation.**	BTL-1	Remembering	PO2,PO3
4	**Explain about DMA controller with neat block diagram.**	BTL-1	Remembering	PO2,PO4
5	**What is an interrupt? Explain the different types of interrupts and the different ways of handling the interrupts.**	BTL-1	Remembering	PO3,PO4
6	**Explain the standard input and output interfaces**	BTL-1	Remembering	PO3,PO4

	required to connect the I/O devices to the bus.			
7	**Explain in detail about programmed I/O and I/O mapped I/O with neat sketch.**	**BTL-1**	**Remembering**	**PO3,PO4**
8	**Write a note on:** **(i) Daisy chaining** **(ii) Polling** **(iii)Independent Priority.**	**BTL-2**	**Understanding**	**PO2,PO3,PO4**
9	**Enumerate the methods for improving performance in cache memory.**	**BTL-1**	**Remembering**	**PO3,PO4**

UNIT I OVERVIEW & INSTRUCTIONS

Eight ideas – Components of a computer system – Technology – Performance – Power wall – Uniprocessors to multiprocessors; Instructions – operations and operands – representing instructions – Logical operations – control operations – Addressing and addressing modes.

PART – A

1. **List the major components of a computer system. (MAY 2017) (NOV/DEC 2017)**
   The basic functional units of a computer are input unit, output unit, memory unit, ALU unit and control unit.

2. **Define addressing modes and its various types. (NOV/DEC 2017)**
   The different ways in which the location of a operand is specified in an instruction is referred to as addressing modes. The various types are Immediate Addressing, Register Addressing, Based or Displacement Addressing, PC-Relative Addressing, Pseudodirect Addressing.

3. **What is indirect addressing mode? (MAY 2017)**
   In this type of execution, multiple functional units are used to create parallel paths through which different instructions can be executed in parallel. So it is possible to start the execution of several instructions in every clock cycle. This mode of operation is called superscalar execution.

4. **Define ALU. What are the various operations performed in ALU? (MAY 2016)**

   ALU is a part of computer that performs all arithmetic and logical operations. It is a component of central processing unit. Arithmetic operations: Addition, subtraction, multiplication, division, increment and decrement; Logical operations: AND, OR, XOR, NOT, compare, shift, rotate.

5. **How to represent instruction in a computer system?(MAY-2016)**
   - Instructions are kept in the computer as a series of high and low electronic signals and may be represented as numbers.
   - Each piece of an instruction can be considered as an individual number, and placing these numbers side by side forms the instruction.

- Since registers are referred to by almost all instructions, there must be a convention to map register names into numbers

MIPS assembly language,

registers `$s0` to `$s7` map onto registers 16 to 23,

registers `$t0` to `$t7` map onto registers 8 to 15.

6. What is auto increment and auto decrement addressing mode? (MAY-2016)

In based or displacement mode addressing, the operand is in a memory location whose address is the sum of a register and a constant in the instruction. Eg. lw $t0,32($s3).

7. What are the eight ideas in computer architecture? (MAY-2015)

- Design for Moore's Law
- Use abstraction to simplify design
- Make the common case fast
- Performance via Parallelism
- Performance via Pipelining
- Performance via Prediction
- Hierarchy of Memory
- Dependability via Redundancy

8. Distinguish pipelining from parallelism. (MAY-2015)

Pipelining reduces speed and increases latency.

Parallel processing increases speed and reduces delay.

9. Define Relative mode addressing.(Nov 2014)

In PC-relative mode addressing, the branch address is the sum of the PC and a constant in the instruction.

10. State Amdahl's Law.(Nov 2014)

Amdahl's Law tells us the improvement expected from specific enhancements. The performance improvement or speedup due to improvement is calculated as follows

$$\text{Speedup} = \frac{\text{Execution time before improvement}}{\text{Execution time after improvement}}$$

11. Define Little Endian arrangement. (Nov 2014)

Little-endian describes the order in which a sequence of bytes is stored in computer memory

12. Define multiprogramming?(A.U.APR/MAY 2013)

Multiprogramming is a technique in several jobs are in main memory at once and the processor is switched from job as needed to keep several jobs advancing while keeping the peripheral devices in use.

13. What is a bus? What are the different buses in a CPU? (APR/MAY 2011)

A group of lines that serve as a connecting path for several devices is called bus .The different buses in a CPU are 1] Data bus 2] Address bus 3] Control bus.

14. What is meant by MAR and MDR? (APR/MAY 2011)

Memory Address Register (MAR) is a register that either stores the memory address from which data will be fetched to the CPU or the address to which data will be sent and stored. MAR holds the memory location of data that needs to be accessed. When reading from memory, data

addressed by MAR is fed into the **MDR U**sed by the CPU.

15. What is meant by stored program concepts?

Stored program concept is an idea of storing the program and data in the memory.

16. What is meant by VLSI technology?

VLSI is the abbreviation for Very Large Scale Integration. In this technology millions of transistors are put inside a single chip as tiny components. The VLSI chips do the function of millions of transistors. These are Used to implement parallel algorithms directly in hardware

17. Define multiprocessing?

Multiprocessing is the ability of an operating system to support more than one process at the same time.

18. Define power wall.

- Old conventional wisdom
- Power is free
- Transistors are expensive
- New conventional wisdom: "Power wall"
- Power expensive
- Transistors "free" (Can put more on chip than can afford to turn on)

19. What is uniprocessor?

A **uniprocessor system** is defined as a computer system that has a single central processing unit that is used to execute computer tasks. As more and more modern software is able to make use of multiprocessing architectures, such as SMP and MPP, the term *uniprocessor* is therefore used to distinguish the class of computers where all processing tasks share a single CPU.

20. What is multicore processor?

A multi-core processor is a single computing component with two or more independent actual central processing units (called "cores"), which are the units that read and execute program instructions. The instructions are ordinary CPU instructions such as add, move data, and branch, but the multiple cores can run multiple instructions at the same time, increasing overall speed for programs amenable to parallel computing.

21. Differentiate between minicomputer and microcomputer.

Minicomputers are small and low cost computers are characterized by Short word size i.e. CPU word sizes of 8 or 16 bits. They have limited hardware and software facilities. They are physically smaller in size. Microcomputer is a smaller, slower and cheaper computer packing all the electronics of the computer in to a handful of IC's, including CPU and memory and IO chips.

22. What is workstation?

The more powerful desktop computers intended for scientific and engineering applications are referred as workstations.

23. What is instruction register?

The instruction register (IR) holds the instruction that is currently being executed. Its output is available to the control circuits which generate the timing signals that control the various processing elements involved in executing the instruction.

24. What is program counter?

The program counter (PC) keeps track of the execution of a program. It contains the memory address of the next instruction to be fetched and executed.

25. What is processor time?

The sum of the periods during which the processor is active is called the processor time.

26. What are clock and clock cycles?

The timing signals that control the processor circuits are called as clocks. The clock defines regular time intervals called clock cycles.

27. Give the CPU performance equation.

CPU execution time for a program =Instruction Count **X**Clock cycles per instruction **X**Clock cycle time.

28. List out the methods used to improve system performance.

The methods used to improve system performance are

- Processor clock
- Basic Performance Equation
- Pipelining
- Clock rate
- Instruction set
- Compiler

29. Define register mode addressing.

In register mode addressing, the name of the register is used to specify the operand. Eg. Add $s3, $s5,$s6.

30. Define Based or Displacement mode addressing.

In based or displacement mode addressing, the operand is in a memory location whose address is the sum of a register and a constant in the instruction. Eg. lw $t0,32($s3).

31. Define immediate mode addressing.

In immediate mode addressing, the operand is given explicitly in the instruction. Eg. Add $s0, $s1,20.

PART – B & C

Q.No	Questions
1	**Explain in detail the different Instruction types.Compare their merits and demerits. (NOV/DEC 2017)** Refer David A. Patterson and John L. Hennessey, "Computer organization and design", Morgan kauffman / elsevier, Fifth edition, 2014 page no.104.
2	**What are the various logical operations and explain the instructions supporting the logical operations? (NOV/DEC 2017)** Refer David A. Patterson and John L. Hennessey, "Computer organization and design", Morgan kauffman / elsevier, Fifth edition, 2014 page no.100**.**
3	**Define Addressing mode and explain the basic addressing modes with an example. (APRIL/MAY2015, APRIL/MAY 2016, MAY/JUNE 2017)** Refer David A. Patterson and John L. Hennessey, "Computer organization and design", Morgan kauffman / elsevier, Fifth edition, 2014 page no. 130.
4	**Explain the important measures of the performance of a computer and derive the basic**

	performance equation. (MAY/JUNE 2017) Refer David A. Patterson and John L. Hennessey, "Computer organization and design", Morgan kauffman / elsevier, Fifth edition, 2014 page no.106.
5	**Explain the various components of computer System with neat diagram.** **(NOV/DEC2014) (MAY-2016)** Refer David A. Patterson and John L. Hennessey, "Computer organization and design", Morgan kauffman / elsevier, Fifth edition, 2014 page no.14.
6	**Explain the ways to represent an instruction in a computer. (MAY-2015)** Refer David A. Patterson and John L. Hennessey, "Computer organization and design", Morgan kauffman / elsevier, Fifth edition, 2014 page no.93.
7	**Explain in detail about the eight ideas of computer architecture.** Refer David A. Patterson and John L. Hennessey, "Computer organization and design", Morgan kauffman / elsevier, Fifth edition, 2014 page no.10.
8	**Write a note on register direct, indirect and immediate addressing modes with examples.** Refer David A. Patterson and John L. Hennessey, "Computer organization and design", Morgan kauffman / elsevier, Fifth edition, 2014 page no. 130.
9	**Consider three different processors P1,P2 and P3 executing the same instruction set. P1 has 4GHz clock rate and CPI of 1.5. P2 has 2.5GHz clock rate and CPI f 1. P3 has 4GHz clock rate and has CPI of 2.2.** **(a) Which Processor has highest performance expressed in instruction per second?** **(b) If the processors each execute a program in 10seconds, find the number of cycles and number of instructions.** **(c) Reducing the execution time by 30% leads to increase in 20% of the CPI. What is the clock rate needed to get this reduction?** Refer David A. Patterson and John L. Hennessey, "Computer organization and design", Morgan kauffman / elsevier, Fifth edition, 2014 page no.99.

UNIT II ARITHMETIC OPERATIONS
ALU - Addition and subtraction – Multiplication – Division – Floating Point operations – Sub word parallelism.

PART – A

1. Subtract $(11011)_2$-$(10011)_2$ using 2's complement. (NOV/DEC-2017)

$(01000)_2$

2. Divide $(1001010)_2$ by $(1000)_2$. (NOV/DEC-2017)

$(000101)_2$

3. State the rule for floating point addition.(MAY-2017)

Choose the number with the smaller exponent and shift its mantissa right a number of steps equal to the difference in exponents. Set the exponent of the result equal to the larger exponent. Perform the addition on the mantissa and determine the sign of the result. Normalize the resulting value if necessary.

4. Subtract $(11010)_2$-$(10000)_2$ using 1's complement and 2's complement method.(MAY/JUNE-2017)

$(001010)_2$

5. What is Subword Parallelism? (MAY-2015,2016)

Subword parallelism is a technique that enables the full use of word-oriented data paths when dealing with lower precision data. It is a form of low-cost, small-scale SIMD parallelism.

6. Write the Add/subtract rule for floating point numbers. (MAY-2016)

1) Choose the number with the smaller exponent and shift its mantissa right a number of steps equal to the difference in exponents.

2) Set the exponent of the result equal to the larger exponent.
3) Perform addition/subtraction on the mantissa and determine the sign of the result
4) Normalize the resulting value, if necessary.

7. How overflow occurs in subtraction? (MAY-2015)

Overflow occurs in subtraction when we subtract a negative number from a positive number and get a negative result, or when we subtract a positive number from a negative number and get a positive result.

Operation	Operand A	Operand B	Result indicating overflow
$A + B$	≥ 0	≥ 0	< 0
$A + B$	< 0	< 0	≥ 0
$A - B$	≥ 0	< 0	< 0
$A - B$	< 0	≥ 0	≥ 0

8. What is half adder?

A half adder is a logic circuit with two inputs and two outputs, which adds two bits at a time, producing a sum and a carry.

9. What is full adder?

A full adder is logic circuit with three inputs and two outputs, which adds three bits at a time giving a sum and a carry.

10. What is signed binary?

A system in which the leading bit represents the sign and the remaining bits the magnitude of the number is called signed binary. This is also known as sign magnitude.

11. What is a carry look-ahead adder?

The input carry needed by a stage is directly computed from carry signals obtained from all the

preceding stages i-1,i-2,…..0, rather than waiting for normal carries to supply slowly from stage to stage. An adder that uses this principle is a called carry look-ahead adder.

12. Define Booth Algorithm.

Booth's multiplication algorithm is a multiplication algorithm that multiplies two signed binary numbers in two's complement notation. Booth's algorithm can be implemented by repeatedly adding (with ordinary unsigned binary addition) one of two predetermined values A and S to a product P, then performing a rightward arithmetic shift on P.

13. What are the main features of Booth's algorithm?

- It handles both positive and negative multipliers uniformly.
- It achieves some efficiency in the number of addition required when the multiplier has a few large blocks of 1s.

14. Define Integer Division and give its rule.

Integers are the set of whole numbers and their opposites. The sign of an integer is positive if the number is greater than zero, and the sign is negative if the number is less than zero. The set of all integers represented by the set {... -4, -3, -2, -1, 0, 1, 2, 3, 4...}Negative integers: {. . . -4, -3, -2, -1} Positive integers: {1, 2, 3, 4 ...}{0} is neither positive nor negative, neutral. DIVISION RULE: The quotient of two integers with same sign is positive. The quotient of two integers with opposite signs is negative.

15. Define Truncation.

To retain maximum accuracy, all extra bits during operation (called *guard bits*) are kept (e.g., multiplication). If we assume $n = 3$bits are used in final representation of a number, $n = 3$extra guard bits are kept during operation. By the end of the operation, the resulting $2n = 6$bits need to be truncated to $n = 3$bits by one of the three methods.

16. Explain how Boolean subtraction is performed?

Negate the subtrahend (i.e. in a-b, the subtrahend is b) then perform addition(2's complement).

17. Define Chopping.

There are several ways to truncate. The simplest way is to remove the guard bits and make no changes in the retained bits. This is called Chopping. Chopping discards the least significant bits and retains the 24 most significant digits. This is easy to implement, and biased, since all values are rounded towards a lower mantissa value. The maximum rounding error is $0 \leq e < +1$ LSB.

18. Define Von Neumann Rounding.

If at least one of the guard bits is 1, the least significant bit of the retained bits is set to 1 otherwise nothing is changed in retained bits and simply guard bits are dropped.

19. How can we speed up the multiplication process?

There are two techniques to speed up the multiplication process:

1) The first technique guarantees that the maximum number of summands that must be added is n/2 for n-bit operands.
2)The second technique reduces the time needed to add the summand.

20. What is bit pair recoding? Give an example.

Bit pair recoding halves the maximum number of summands. Group the Booth-recoded multiplier bits in pairs and observe the following: The pair (+1 -1) is equivalent to to the pair (0 +1). That is instead of adding -1 times the multiplicand m at shift position i to +1 M at position i+1, the same result is obtained by adding +1 M at position i.

Eg: 11010 – Bit Pair recoding value is 0 -1 -2

21. What are the two methods of achieving the 2's complement?

a. Take the 1's complement of the number and add 1.

b. Leave all least significant 0's and the first unchanged and then complement the remaining bits.

22. What is the advantage of using Booth algorithm?

1) It handles both positive and negative multiplier uniformly.

2) It achieves efficiency in the number of additions required when the multiplier has a few large blocks of 1's.

3) The speed gained by skipping 1's depends on the data.

23. What is Carry Save addition?

Using carry save addition, the delay can be reduced further still. The idea is to take 3 numbers that we want to add together, x+y+z, and convert it into 2 numbers c+s such that x+y+z=c+s, and do this in O (1) time. The reason why addition cannot be performed in O (1) time is because the carry information must be propagated. In carry save addition, we refrain from directly passing on the carry information until the very last step.

24. Write the algorithm for restoring division.

Do the following for n times:

1) Shift A and Q left one binary position.
2) Subtract M and A and place the answer back in A.
3) If the sign of A is 1, set q0 to 0 and add M back to A. Where A- Accumulator, M- Divisor, Q- Dividend.

Step 1: Do the following for n times:

1) If the sign of A is 0, shift A and Q left one bit position and subtract M from A; otherwise, shift A and Q left and add M to A.
2) Now, if the sign of A is 0, set q0 to 1; otherwise, set q0 to0.

Step 2: if the sign of A is 1, add M to A.

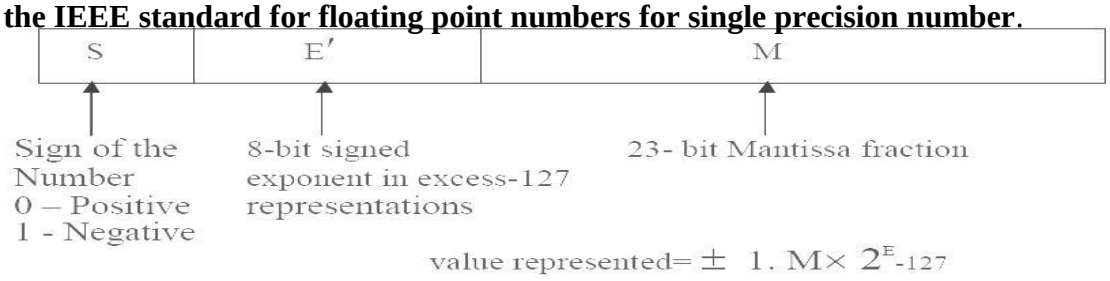
25. Write the algorithm for restoring division.

Non- Restoring Division Algorithm

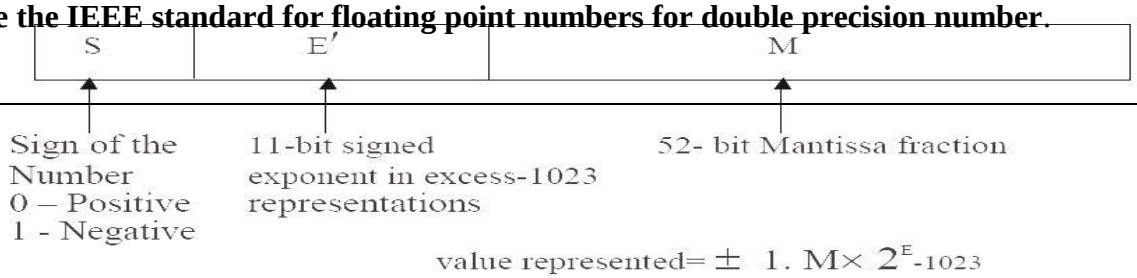
Step 1: Do the following n times: If the sign of A is 0, shift A and Q left one bit position and subtract M from A; otherwise, shift A and Q left and add M to A. Now, if the sign of A is 0, set q0 to 1; otherwise, set q0 to 0.

Step 2: If the Sign of A is 1, add M to A.

26. Give the IEEE standard for floating point numbers for single precision number.



27. Give the IEEE standard for floating point numbers for double precision number.



28. When can you say that a number is normalized?

When the decimal point is placed to the right of the first (nonzero) significant digit, the number is said to be normalized.

The end values 0 to 255 of the excess-127 exponent E are used to represent

special values such as:

a) When E = 0 and the mantissa fraction M is zero the value exact 0 is represented.

1. When E = 255 and M=0, the value is represented.
2. When E = 0 and M 0, denormal values are represented.
3. When E = 2555 and M 0, the value represented is called Not a number.

29. Write the multiply rule for floating point numbers.

1) Add the exponent and subtract 127.

2) Multiply the mantissa and determine the sign of the result

3) Normalize the resulting value, if necessary.

30. What is guard bit?

Although the mantissa of initial operands are limited to 24 bits, it is important to retain extra bits, called as guard bits.

31. What are the ways to truncate the guard bits?

There are several ways to truncate the guard its:

1) Chopping

2) Von Neumann rounding

3) Rounding

32. What are generate and propagate function?

The generate function is given by

Gi=xiyi and

The propagate function is given as

Pi=xi+yi.

33. What is excess-127 format?

Instead of the signed exponent E, the value actually stored in the exponent field is and unsigned integer E. In some cases, the binary point is variable and is automatically adjusted as computation proceeds. In such case, the binary point is said to float and the numbers are called floating point

numbers.

34. In floating point numbers when so you say that an underflow or overflow has occurred? (MAY-2015)

In single precision numbers when an exponent is less than -126 then we say that an underflow has occurred. In single precision numbers when an exponent is less than +127 then we say that an overflow has occurred.

PART – B & C

Q.No	Questions
1	**Add 0.5_{10} and -0.4375_{10} using floating point addition algorithm. (NOV/DEC-2017)** Refer David A. Patterson and John L. Hennessey, "Computer organization and design", Morgan kauffman / elsevier, Fifth edition, 2014 page no. 233.
2	**Explain restoring division technique with example. .(NOV/DEC-2017)** Refer David A. Patterson and John L. Hennessey, "Computer organization and design", Morgan kauffman / elsevier, Fifth edition, 2014 page no.230.
3	**Explain the sequential version of Multiplication algorithm in detail with diagram and examples. (APRIL/MAY2015,2016,2017)** Refer David A. Patterson and John L. Hennessey, "Computer organization and design", Morgan kauffman / elsevier, Fifth edition, 2014 page no.222
4	**(i) Explain Non – restoring division technique with example. (MAY-2017)** Refer David A. Patterson and John L. Hennessey, "Computer organization and design", Morgan kauffman / elsevier, Fifth edition, 2014 page no.232. **(ii) What is meant by sub word parallelism? Explain. (MAY-2017)** Refer David A. Patterson and John L. Hennessey, "Computer organization and design", Morgan kauffman / elsevier, Fifth edition, 2014 page no. 238.
5	**Give the block diagram for a floating point adder and subtractor unit and discuss its operation. (MAY-2016, 2017)** Refer David A. Patterson and John L. Hennessey, "Computer organization and design", Morgan kauffman / elsevier, Fifth edition, 2014 page no. 232.
6	**Explain in detail about floating point addition with example. (APRIL/MAY2015)** Refer David A. Patterson and John L. Hennessey, "Computer organization and design",

	Morgan kauffman / elsevier, Fifth edition, 2014 page no.234.
7	**(i) Briefly explain Carry look ahead adder.** **(ii) Multiply the following pair of signed nos.using Booth's bit –pair recoding of the multiplier A=+13 (multiplicand) and b= -6(multiplier)** Refer David A. Patterson and John L. Hennessey, "Computer organization and design", Morgan kauffman / elsevier, Fifth edition, 2014 page no.216.
8	**Show the IEEE754 binary representation of the number -0.75$_{10}$ in single and double precision.** Refer David A. Patterson and John L. Hennessey, "Computer organization and design", Morgan kauffman / elsevier, Fifth edition, 2014 page no. 239.
9	**Brief on carry look ahead layer and booth multiplier in detail.** Refer David A. Patterson and John L. Hennessey, "Computer organization and design", Morgan kauffman / elsevier, Fifth edition, 2014 page no. 211.

UNIT III PROCESSOR AND CONTROL UNIT

Basic MIPS implementation – Building data path – Control Implementation scheme – Pipelining – Pipelined data path and control – Handling Data hazards & Control hazards –Exceptions.

PART – A

1. Mention the types of pipelining. (NOV/DEC2017)

- Instruction pipeline
- Arithmetic pipeline

2.Mention the various phase in executing an instruction. (NOV/DEC 2017)

Fetch Instruction

Decode instruction and fetch operands

Perform ALU operation

Access memory

Write back result to register file

Update PC

3. Name the control signals required to perform arithmetic operations. (MAY-2017)

Signal name	Effect when deasserted	Effect when asserted
RegDst	The register destination number for the Write register comes from the rt field (bits 20:16).	The register destination number for the Write register comes from the rd field (bits 15:11).
RegWrite	None.	The register on the Write register input is written with the value on the Write data input.
ALUSrc	The second ALU operand comes from the second register file output (Read data 2).	The second ALU operand is the sign-extended, lower 16 bits of the instruction.
PCSrc	The PC is replaced by the output of the adder that computes the value of PC + 4.	The PC is replaced by the output of the adder that computes the branch target.
MemRead	None.	Data memory contents designated by the address input are put on the Read data output.
MemWrite	None.	Data memory contents designated by the address input are replaced by the value on the Write data input.
MemtoReg	The value fed to the register Write data input comes from the ALU.	The value fed to the register Write data input comes from the data memory.

4. What is meant by data hazard in pipelining? (Nov/Dec 2013)(May-2017)

Any condition in which either the source or the destination operands of an instruction are not available at the time expected in the pipeline is called data hazard.

5. Define exception and interrupt. (May-2016)

Exception:

The term exception is used to refer to any event that causes an interruption.

Interrupt:

An exception that comes from outside of the processor. There are two types of interrupt.

1. Imprecise interrupt and 2.Precise interrupt

6. What is pipelining? (May-2016)

The technique of overlapping the execution of successive instruction for substantial improvement in performance is called pipelining.

7. Why is branch prediction algorithm needed? Differentiate between the static and dynamic techniques. (May 2013,2015)

The branch instruction will introduce branch penalty which would reduce the gain in performance expected from pipelining. Branch instructions can be handled in several ways to reduce their negative impact on the rate of execution of instructions. Thus the branch prediction algorithm is needed.

Static Branch prediction

The static branch prediction, assumes that the branch will not take place and to continue to fetch instructions in sequential address order.

Dynamic Branch prediction

The idea is that the processor hardware assesses the likelihood of a given branch being taken by keeping track of branch decisions every time that instruction is executed. The execution history used in predicting the outcome of a given branch instruction is the result of the most recent

execution of that instruction.

8. What is precise exception in R-type instruction? (May-2015)

A precise exception is one in which all instructions prior to the faulting instruction are complete and instruction following the faulting instruction, including the faulty instruction; do not change the state of the machine.

9. Define processor cycle in pipelining.

The time required between moving an instruction one step down the pipeline is a processor cycle.

10. What is meant by pipeline bubble?

To resolve the hazard the pipeline is stall for 1 clock cycle. A stall is commonly called a pipeline bubble, since it floats through the pipeline taking space but carrying no useful work.

11. What is pipeline register delay?

Adding registers between pipeline stages me adding logic between stages and setup and hold times for proper operations. This delay is known as pipeline register delay.

12. What are the major characteristics of a pipeline?

The major characteristics of a pipeline are:

1. Pipelining cannot be implemented on a single task, as it works by splitting multiple tasks into a number of subtasks and operating on them simultaneously.
2. The speedup or efficiency achieved by suing a pipeline depends on the number of pipe stages and the number of available tasks that can be subdivided.

13. What is data path?

As instruction execution progress data are transferred from one instruction to another, often passing through the ALU to perform some arithmetic or logical operations. The registers, ALU, and the interconnecting bus are collectively referred as the data path.

14. What is a pipeline hazard and what are its types?

Any condition that causes the pipeline to stall is called hazard. They are also called as stalls or bubbles. The various pipeline hazards are:

Data hazard Structural
Hazard Control Hazard.

15. What is Instruction or control hazard?

The pipeline may be stalled because of a delay in the availability of an instruction. For example, this may be a result of a miss in the cache, requiring the instruction to be fetched from the main memory. Such hazards are often called control hazards or instruction hazard.

16. Define structural hazards.

This is the situation when two instruction require the use of a given hardware resource at the same

time. The most common case in which this hazard may arise is in access to memory.

17. What is side effect?

When a location other than one explicitly named in an instruction as a destination operand is affected, the instruction is said to have a side effect.

18. What do you mean by branch penalty?

The time lost as a result of a branch instruction is often referred to as branch penalty.

19. What is branch folding?

When the instruction fetch unit executes the branch instruction concurrently with the execution of the other instruction, then this technique is called branch folding.

20. What do you mean by delayed branching?

Delayed branching is used to minimize the penalty incurred as a result of conditional branch instruction. The location following the branch instruction is called delay slot. The instructions in the delay slots are always fetched and they are arranged such that they are fully executed whether or not branch is taken. That is branching takes place one instruction later than where the branch instruction appears in the instruction sequence in the memory hence the name delayed branching.

21. What is branch Target Address?

The address specified in a branch, which becomes the new program counter, if the branch is taken. In MIPS the branch target address is given by the sum of the offset field of the instruction and the address of the instruction following the branch.

22. Why pipelining is needed?

Pipelining is a technique of decomposing a sequential process in to sub processes with each sub process being executed in a special dedicated segment that operates concurrently with all other program.

23. How do control instructions like branch, cause problems in a pipelined processor?

Pipelined processor gives the best throughput for sequenced line instruction. In branch instruction, as it has to calculate the target address, whether the instruction jump from one memory location to other. In the meantime, before calculating the larger, the next sequence instructions are got into the pipelines, which are rolled back, when target is calculated.

24. What is meant by super scalar processor?

Super scalar processors are designed to exploit more instruction level parallelism in user programs. This means that multiple functional units are used. With such an arrangement it is possible to start the execution of several instructions in every clock cycle. This mode of operation is called super scalar execution.

25. Define pipeline speedup.

Speed up is the ratio of the average instruction time without pipelining to the average instruction time with pipelining. Average instruction time without pipelining Speedup= Average instruction time with pipelining

26. What is pipelined computer?

When hardware is divided in to a number of sub units so as to perform the sub operations in an

overlapped fashion is called as a pipelined computer.

27. List the various pipelined processors.

8086, 8088, 80286, 80386. STAR 100, CRAY 1 and CYBER 205 etc

28. Classify the pipeline computers.

Based on level of processing → processor pipeline, instruction pipeline, arithmetic pipelines

Based on number of functions→ Uni-functional and multi functional pipelines.

Based on the configuration → Static and Dynamic pipelines and linear and non linear pipelines

Based on type of input→ Scalar and vector pipelines.

29. Define Pipeline speedup.

The ideal speedup from a pipeline is equal to the number of stages in the pipeline.

$$\frac{\text{Time per instruction on unpipelined machine}}{\text{Number of pipe stages}}$$

30. What is Vectorizer?

The process to replace a block of sequential code by vector instructions is called vectorization. The system software, which generates parallelism, is called as vectorizing compiler.

31. Write down the expression for speedup factor in a pipelined architecture.

The speedup for a pipeline computer is $S = (k + n - 1)\ tp$

Where,K → number of segments in a pipeline,N → number of instructions to be executed. Tp → cycle time.

32. What are the problems faced in instruction pipeline.

Resource conflicts → Caused by access to the memory by two at the same time. Most of the conflicts can be resolved by using separate instruction and data memories.

Data dependency → Arises when an instruction depends on the results of the previous instruction but this result is not yet available.

Branch difficulties → Arises from branch and other instruction that change the value of PC (Program Counter).

33. What is meant by vectored interrupt?

An interrupt for which the address to which control is transferred is determined by the cause of the exception.

PART – B & C

Q.No	Questions
1	**Explain in detail about building a datapath. (NOV/DEC2014) (NOV/DEC 2017)**

	Refer David A. Patterson and John L. Hennessey, "Computer organization and design", Morgan kauffman / elsevier, Fifth edition, 2014 page no.293.
2	**Explain pipeline hazard in detail. (NOV/DEC 2017)** Refer David A. Patterson and John L. Hennessey, "Computer organization and design", Morgan kauffman / elsevier, Fifth edition, 2014 page no.364.
3	**(i) Explain the hazards caused by unconditional branching statements. (May-2017)** **(ii) Describe operand forwarding in a pipelined processor with diagram. (May-2017)** Refer David A. Patterson and John L. Hennessey, "Computer organization and design", Morgan kauffman / elsevier, Fifth edition, 2014 page no.288.
4	**Discuss the modified data path to accommodate pipelined executions with diagram. (May-2017)** Refer David A. Patterson and John L. Hennessey, "Computer organization and design", Morgan kauffman / elsevier, Fifth edition, 2014 page no.296.
5	**What is hazards? Explain the types of hazards. (NOV/DEC2014) (MAY-2015,2016)** Refer David A. Patterson and John L. Hennessey, "Computer organization and design", Morgan kauffman / elsevier, Fifth edition, 2014 page no.349.
6	**Explain pipelined datapath and its control. (May 2016)** Refer David A. Patterson and John L. Hennessey, "Computer organization and design", Morgan kauffman / elsevier, Fifth edition, 2014 page no.330.
7	**How exceptions are handled in MIPS? (APRIL/MAY2015)** Refer David A. Patterson and John L. Hennessey, "Computer organization and design", Morgan kauffman / elsevier, Fifth edition, 2014 page no.370.
8	**Describe the techniques for handling control hazard in pipelining. (May 2013)** Refer David A. Patterson and John L. Hennessey, "Computer organization and design", Morgan kauffman / elsevier, Fifth edition, 2014 page no.361.
9	**Write short notes on exception handling.** Refer David A. Patterson and John L. Hennessey, "Computer organization and design", Morgan kauffman / elsevier, Fifth edition, 2014 page no.362.
10	**Explain how the instruction pipeline works. What are the various situations where an instruction pipeline can stall? How it can be resolved?** Refer David A. Patterson and John L. Hennessey, "Computer organization and design",

	Morgan kauffman / elsevier, Fifth edition, 2014 page no.299.

UNIT IV PARALLELISM

Instruction-level-parallelism – Parallel processing challenges – Flynn's classification – Hardware multithreading– Multicore processors

PART – A

1. **What are Fine grained multithreading and Coarse grained multithreading? (NOV/DEC 2017)(May-2016)(May-2017)**

Fine grained multithreading

Switches between threads on each instruction, causing the execution of multiples threads to be interleaved,

- Usually done in a round-robin fashion, skipping any stalled threads
- CPU must be able to switch threads every clock

Coarse grained multithreading

Switches threads only on costly stalls, such as L2 cache misses

2. **Define Strong scaling and weak scaling. (NOV/DEC-2017)(May-2015)**

Strong scaling

Speed-up achieved on a multi-processor without increasing the size of the problem.

Weak scaling.

Speed-up achieved on a multi-processor while increasing the size of the problem proportionally to the increase in the number of processors.

3. **What is Instruction level parallelism? (May-2016)(May-2017)**

ILP is a measure of how many of the operations in a computer program can be performed simultaneously. The potential overlap among instructions is called instruction level parallelism.

4. **Compare UMA and NUMA multiprocessors. (May-2015)**

UNIFORM MEMORY ACCESS (UMA)

A multiprocessor in which latency to any word in main memory is about the same no matter which processor requests the access.

NONUNIFORM MEMORY ACCESS (NUMA)

A type of single address space multiprocessor in which some memory accesses are much faster than others depending on which processor asks for which word.

5. Explain various types of Dependences in ILP.

- Data Dependences
- Name Dependences
- Control Dependences

6. What is multiprocessors? Mention the categories of multiprocessors?

Multiprocessor is the use of two or more central processing units (CPUs) within a single computer system. It is used to increase performance and improve availability. The different categories are SISD, SIMD, MIMD.

7. Define Static multiple issue and Dynamic multiple issue.

Static multiple issue -An approach to implementing a multiple-issue processor where many decisions are made by the compiler before execution.

Dynamic multiple issue -An approach to implementing a multiple-issue processor where many decisions are made during execution by the processor.

8. What is Speculation?

An approach whereby the compiler or processor guesses the outcome of an instruction to remove it as dependence in executing other instructions.

9. Define Use latency.

Number of clock cycles between a load instruction and an instruction that can use the result of the load with-out stalling the pipeline.

10. What is Loop unrolling?

A technique to get more performance from loops that access arrays, in which multiple copies of the loop body are made and instructions from different iterations are scheduled together.

11. Define Register renaming.

The renaming of registers by the compiler or hardware to remove anti-dependences.

12. What is Superscalar and Dynamic pipeline schedule?

Superscalar-An advanced pipelining technique that enables the processor to execute more than one instruction per clock cycle by selecting them during execution.

Dynamic pipeline schedule-Hardware support for reordering the order of instruction execution so as to avoid stalls.

13. Define Commit unit.

The unit in a dynamic or out-of-order execution pipeline that decides when it is safe to release the result of an operation to programmer visible registers and memory.

14. What is Reservation station?

A buffer within a functional unit that holds the operands and the operation.

15. Define Reorder buffer?

The buffer that holds results in a dynamically scheduled processor until it is safe to store the results to memory or a register.

16. Define Out of order execution.

A situation in pipelined execution when an instruction blocked from executing does not cause the following instructions to wait.

17. What is In order commit?

A commit in which the results of pipelined execution are written to the programmer visible state in the same order that instructions are fetched.

18. Distinguish between shared memory multiprocessor and message-passing multiprocessor.

- A multiprocessor with a shared address space, that address space can be used to communicate data implicitly via load and store operations is shared memory multiprocessor.
- A multiprocessor with a multiple address space, communication of data is done by explicitly passing message among processor is message-passing multiprocessor.

19. Define Single Instruction, Single Data stream (SISD)

A sequential computer which exploits no parallelism in either the instruction or data streams. Single control unit (CU) fetches single Instruction Stream (IS) from memory. The CU then generates appropriate control signals to direct single processing element (PE) to operate on single Data Stream (DS) i.e. one operation at a time.

Examples of SISD architecture are the traditional uniprocessor machines like a PC.

20. Define Single Instruction, Multiple Data streams (SIMD) and Multiple Instruction, Single Data stream (MISD).

Single Instruction, Multiple Data streams (SIMD)

A computer which exploits multiple data streams against a single instruction stream to perform operations which may be naturally parallelized. For example, an array processor or GPU.

Multiple Instruction, Single Data stream (MISD)

Multiple instructions operate on a single data stream. Uncommon architecture which is generally used for fault tolerance. Heterogeneous systems operate on the same data stream and must agree on the result. Examples include the Space Shuttle flight control computer.

21. Define Multiple Instruction, Multiple Data streams (MIMD) and Single program multiple data streams .

Multiple Instruction, Multiple Data streams (MIMD)

Multiple autonomous processors simultaneously executing different instructions on different data. Distributed systems are generally recognized to be MIMD architectures; either exploiting a single shared memory space or a distributed memory space. A multi-coresuperscalar processor is an MIMD processor.

Single program multiple data streams :

Multiple autonomous processors simultaneously executing the same program on different data.

22. Define multithreading.

Multiple threads to share the functional units of 1 processor via overlapping processor must

duplicate independent state of each thread e.g., a separate copy of register file, a separate PC, and for running independent programs, a separate page table memory shared through the virtual memory mechanisms, which already support multiple processes

23. What is multiple issue? Write any two approaches.

Multiple issue is a scheme whereby multiple instructions are launched in one clock cycle. It is a method for increasing the potential amount of instruction-level parallelism. It is done by replicating the internal components of the computer so that it can launch multiple instructions in every pipeline stage. The two approaches are: 1. Static multiple issue (at compile time) 2. Dynamic multiple issue (at run time)

24. What is meant by speculation?

One of the most important methods for finding and exploiting more ILP is speculation. It is an approach whereby the compiler or processor guesses the outcome of an instruction to remove it as dependence in executing other instructions. For example, we might speculate on the outcome of a branch, so that instructions after the branch could be executed earlier.

25. Define – Static Multiple Issue

Static multiple issue is an approach to implement a multiple-issue processor where many decisions are made by the compiler before execution.

26. Define – Issue Slots and Issue Packet

Issue slots are the positions from which instructions could be issued in a given clock cycle. By analogy, these correspond to positions at the starting blocks for a sprint. Issue packet is the set of instructions that issues together in one clock cycle; the packet may be determined statically by the compiler or dynamically by the processor.

27. What is meant by loop unrolling?

An important compiler technique to get more performance from loops is loop unrolling, where multiple copies of the loop body are made. After unrolling, there is more ILP available by overlapping instructions from different iterations.

28. What is meant by anti-dependence? How is it removed?

Anti-dependence is an ordering forced by the reuse of a name, typically a register, rather than by a true dependence that carries a value between two instructions. It is also called as name dependence. Register renaming is the technique used to remove anti-dependence in which the registers are renamed by the compiler or hardware.

29. What is the use of reservation station and reorder buffer?

Reservation station is a buffer within a functional unit that holds the operands and the operation. Reorder buffer is the buffer that holds results in a dynamically scheduled processor until it is safe to store the results to memory or a register.

30. Define – VLIW

Very Long Instruction Word (VLIW) is a style of instruction set architecture that launches many operations that are defined to be independent in a single wide instruction, typically with many

separate opcode fields.

31. Define Multicore processors.

A multi-core processor is a processing system composed of two or more independent cores. The cores are typically integrated onto a single integrated circuit die or they may be integrated onto multiple dies in a single chip package.

32. What are symmetric multi-core processor and asymmetric multi-core processor?

A symmetric multi-core processor is one that has multiple cores on a single chip, and all of those cores are identical. Example: Intel Core

In an asymmetric multi-core processor, the chip has multiple cores onboard, but the cores might be different designs. Each core will have different capabilities

PART – B & C

Q.No	Questions
1	**Explain in detail hardware Multithreading. (NOV/DEC2014) (May-2015,2016,2017) (NOV/DEC-2017)** Refer David A. Patterson and John L. Hennessey, "Computer organization and design", Morgan kauffman / elsevier, Fifth edition, 2014 page no.631.
2	**Discuss in detail about Flynn's classification. (APR/MAY 2015,2016) (NOV/DEC 2017)** Refer David A. Patterson and John L. Hennessey, "Computer organization and design", Morgan kauffman / elsevier, Fifth edition, 2014 page no.634.
3	**Explain Instruction level parallelism& challenges of parallel processing. (NOV/DEC2014)(May-2017)** Refer David A. Patterson and John L. Hennessey, "Computer organization and design", Morgan kauffman / elsevier, Fifth edition, 2014 page no.620.
4	**Explain Multicore processors. (NOV/DEC2014) (May-2016)** Refer David A. Patterson and John L. Hennessey, "Computer organization and design", Morgan kauffman / elsevier, Fifth edition, 2014 page no.650.
5	**Explain challenges in parallel processing.** Refer David A. Patterson and John L. Hennessey, "Computer organization and design", Morgan kauffman / elsevier, Fifth edition, 2014 page no.622.
6	**Dwell on the concept of instruction level parallelism with examples.** Refer David A. Patterson and John L. Hennessey, "Computer organization and design",

	Morgan kauffman / elsevier, Fifth edition, 2014 page no.629.
7	**Write short note on:** **(i) SISD** **(ii) MIMD** Refer David A. Patterson and John L. Hennessey, "Computer organization and design", Morgan kauffman / elsevier, Fifth edition, 2014 page no.634.
8	**Discuss about Implicit and Explicit multithreading. Compare and contrast with fine grained and coarse grained multithreading.** Refer David A. Patterson and John L. Hennessey, "Computer organization and design", Morgan kauffman / elsevier, Fifth edition, 2014 page no.631.
9	**Dwell on shared memory multiprocessor architecture.** Refer David A. Patterson and John L. Hennessey, "Computer organization and design", Morgan kauffman / elsevier, Fifth edition, 2014 page no.650.

UNIT V MEMORY AND I/O SYSTEMS

Memory hierarchy - Memory technologies – Cache basics – Measuring and improving cache performance - Virtual memory, TLBs - Input/output system, programmed I/O, DMA and interrupts, I/O processors.

PART – A

1. How many total bits required for direct mapped cache with 16KB of data and 4-word blocks, assuming 32-bit address. (Nov/Dec-2017)

4096

2. Define virtual memory. (Nov/Dec-2017)(May-2016)

The data is to be stored in physical memory locations that have addresses different from those specified by the program. The memory control circuitry translates the address specified by the program into an address that can be used to access the physical memory

3. How does a processor handle an interrupt?(May-2017)

Assume that an interrupt request arises during execution of instruction i. steps to handle interrupt by the processor is as follow:

Processor completes execution of instruction i

Processor saves the PC value, program status on to stack.

It loads the PC with starting address of ISR

After ISR is executed, the processor resumes the main program execution by reloading PC with (i+1)th instruction address

4. Define memory interleaving. (May-2017)

In order to carry out two or more simultaneous access to memory, the memory must be partitioned in to separate modules. The advantage of a modular memory is that it allows the interleaving i.e. consecutive addresses are assigned to different memory module.

5. Define Memory Hierarchy. (May-2016,2015)

A structure that uses multiple levels of memory with different speeds and sizes. The faster memories are more expensive per bit than the slower memories.

6. Point out how DMA can improve I/O speed. (May-2015)

DMA interface controller can take the control and responsibility of transferring data without the intervention of CPU. The CPU and IO controller interacts with each other only when the control of bus is requested.

7. What is principle of locality?

The principle of locality states that programs access a relatively small portion of their address space at any instant of time.

8. Define temporal locality.

The principle stating that a data location is referenced then it will tend to be referenced again soon.

9. Define spatial locality.

The locality principle stating that if a data location is referenced, data locations with nearby addresses will tend to be referenced soon.

10. Define hit ratio.

When a processor refers a data item from a cache, if the referenced item is in the cache, then such a reference is called Hit. If the referenced data is not in the cache, then it is called Miss, Hit ratio is defined as the ratio of number of Hits to number of references.

Hit ratio =Total Number of references

11. What is TLB? What is its significance?

Translation look aside buffer is a small cache incorporated in memory management unit. It consists of page table entries that correspond to most recently accessed pages. Significance The TLB enables faster address computing. It contains 64 to 256 entries

12. How cache memory is used to reduce the execution time.

If active portions of the program and data are placed in a fast small memory, the average memory access time can be reduced, thus reducing the total execution time of the program. Such a fast small memory is called as cache memory

13. In many computers the cache block size is in the range 32 to 128 bytes. What would be the main Advantages and disadvantages of making the size of the cache blocks larger or

smaller?

Larger the size of the cache fewer be the cache misses if most of the data in the block are actually used. It will be wasteful if much of the data are not used before the cache block is moved from cache. Smaller size means more misses

14. What is the function of a TLB? (Translation Look-aside Buffer)

A small cache, called the Translation Look aside Buffer (TLB) is interpolated into the memory management unit, which consists of the page table entries that corresponding to the most recently accessed paper.

15. Define locality of reference. What are its types?

During the course of execution of a program memory references by the processor for both the instruction and the data tends to cluster. There are two types:

1. Spatial Locality 2. Temporal Locality

16. Define Hit and Miss?

The performance of cache memory is frequently measured in terms of a quantity called hit ratio. When the CPU refers to memory and finds the word in cache, it is said to produce a hit. If the word is not found in cache, then it is in main memory and it counts as a miss.

17. What is cache memory?

It is a fast memory that is inserted between the larger slower main memory and the processor. It holds the currently active segments of a program and their data.

18. What is Direct mapped cache?

A cache structure in which each memory location is mapped to exactly one location in the cache.

19. Define write through and write buffer.

A scheme in which writes always update both the cache and the next lower level of the memory hierarchy, ensuring the data is always consistent between the two.

Write buffer-A queue that holds data while the data is waiting to be written to memory.

20. What is write-back?

A scheme that handles writes by updating values only to the block in the cache, then writing the modified block to the lower level of the hierarchy when the block is replaced.

21. What is memory system?

Every computer contains several types of devices to store the instructions and data required for its operation. These storage devices plus the algorithm-implemented by hardware and/or software-needed to manage the stored information from the memory system of computer.

22. Give the classification of memory.

They can be placed into 4 groups.

• CPU registers • Main memory

• Secondary memory • Cache

23. What is Read Access Time?

A basic performance measure is the average time to read a fixed amount of information, for instance, one word, from the memory. This parameter is called the read access time.

24. What is Serial Access Memory?

Memories whose storage locations can be accessed only in a certain predetermined sequence called serial access time.

25. Define Random Access Memory.

It storage locations can be accessed in any order and access time is independent of the location being accessed, the memory is termed a random-access memory.

26. What is Semi Random Access?

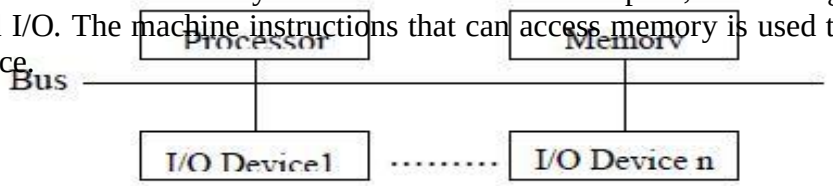
Memory devices such as magnetic hard disks and CD-ROMs contain many rotating storage tracks. If each track has its own read write head, the tracks can be accessed randomly, but access within each track is serial. In such cases the access mode is semi random.

27. What is the necessary of virtual memory?

Virtual memory is an important concept related to memory management. It is used to increase the apparent size of main memory at a very low cost. Data are addressed in a virtual address space that can be as large as the addressing capability of CPU.

28. Distinguish between memory mapped I/O and I/O mapped I/O.

When I/O devices and the memory share the same address space, the arrangement is called memory mapped I/O. The machine instructions that can access memory is used to trfer data to or from an I/O device.



I/O mapped I/O:

Here the I/O devices the memories have different address space. It has special I/O instructions. The advantage of a separate I/O address space is that I/O devices deals with fewer address lines.

29.What is SCSI?

Small **C**omputer System Interface, a parallel interface standard. SCSI interfaces provide for faster data transmission rates (up to 80 megabytes per second) than standard serial and parallel ports. In addition, you can attach many devices to a single SCSI port, so that SCSI is really an I/O bus rather than simply an interface.

30.Define USB.

Universal Serial Bus, an external bus standard that supports data transfer rates of 12 Mbps. A single USB port can be used to connect up to 127 peripheral devices, such as mice, modems, and keyboards.

USB also supports Plug-and-Play installation and hot plugging.

31. What are the units of an interface?

DATAIN, DATAOUT, SIN, SOUT

32.Distinguish between isolated and memory mapped I/O?

The **isolated I/O** method isolates memory and I/O addresses so that memory address values are not affected by interface address assignment since each has its own address space.

In **memory mapped I/O**, there are no specific input or output instructions. The CPU can manipulate I/O data residing in interface registers with the same instructions that are used to manipulate memory words.

33. What is the use of DMA?

DMA (Direct Memory Access) provides I/O transfer of data directly to and from the memory unit and the peripheral**.**

34.What is meant by vectored interrupt?

Vectored Interrupts are type of I/O interrupts in which the device that generates the interrupt request (also called IRQ in some text books) identifies itself directly to the processor.

35.Compare Static RAM and Dynamic RAM.

Static RAM is more expensive, requires four times the amount of space for a given amount of data than dynamic RAM, but, unlike dynamic RAM, does not need to be power-refreshed and is therefore faster to access. Dynamic RAM uses a kind of capacitor that needs frequent power refreshing to retain its charge. Because reading a DRAM discharges its contents, a power refresh is required after each read. Apart from reading, just to maintain the charge that holds its content in place, DRAM must be refreshed about every 15 microseconds. DRAM is the least expensive kind of RAM.

PART – B & C

Q.No	Questions
1	**Discuss the various mapping schemes used in cache memory. (NOV/DEC2014) (May-2016)(May-2017) (Nov/Dec-2017)** Refer David A. Patterson and John L. Hennessey, "Computer organization and design", Morgan kauffman / elsevier, Fifth edition, 2014 page no.461.
2	**Explain in detail about memory Technologies. (APRIL/MAY2015) (Nov/Dec-2017)** Refer David A. Patterson and John L. Hennessey, "Computer organization and design", Morgan kauffman / elsevier, Fifth edition, 2014 page no.492.
3	**What is virtual memory? Explain the steps involved in virtual memory address translation. (MAY2015)(May-2017)** Refer David A. Patterson and John L. Hennessey, "Computer organization and design",

	Morgan kauffman / elsevier, Fifth edition, 2014 page no.478.
4	**Explain about DMA controller with neat block diagram. . (MAY 2016)(May-2017)** Refer David A. Patterson and John L. Hennessey, "Computer organization and design", Morgan kauffman / elsevier, Fifth edition, 2014 page no.578.
5	**What is an interrupt? Explain the different types of interrupts and the different ways of handling the interrupts. (Dec 2012)** Refer David A. Patterson and John L. ennessey, "Computer organization and design", Morgan kauffman / elsevier, Fifth edition, 2014 page no.442.
6	**Explain the standard input and output interfaces required to connect the I/O devices to the bus.** Refer David A. Patterson and John L. Hennessey, "Computer organization and design", Morgan kauffman / elsevier, Fifth edition, 2014 page no.584.
7	**Explain in detail about programmed I/O and I/O mapped I/O with neat sketch.** Refer David A. Patterson and John L. Hennessey, "Computer organization and design", Morgan kauffman / elsevier, Fifth edition, 2014 page no.599.
8	**Write a note on:** **(i) Daisy chaining** **(ii) Polling** **(iii)Independent Priority.** Refer David A. Patterson and John L. Hennessey, "Computer organization and design", Morgan kauffman / elsevier, Fifth edition, 2014 page no.442.
9	**Enumerate the methods for improving performance in cache memory.** Refer David A. Patterson and John L. Hennessey, "Computer organization and design", Morgan kauffman / elsevier, Fifth edition, 2014 page no.461.