JEPPIAAR ENGINEERING COLLEGE

Jeppiaar Nagar, Rajiv Gandhi Salai – 600 119

DEPARTMENT OF

ELECTRONICS AND COMMUNICATION ENGINEERING

QUESTION BANK

VI SEMESTER

EC6601 – VLSI DESIGN

Regulation – 2013(Batch: 2015-2019)

Academic Year 2017 – 18

Prepared by

Mr.G.BALACHANDRAN, Assistant Professor /ECE

JEPPIAAR ENGINEERING COLLEGE

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DEPARTMENT OF ELECTRONICS AND COMMUNICATION ENGINEERING

QUESTION BANK

SUBJECT : EC6601 – VLSI Design

YEAR /SEM: III /VI

UNIT I MOS TRANSISTOR PRINCIPLE

NMOS and PMOS transistors, Process parameters for MOS and CMOS, Electrical properties of CMOS circuits and device modeling, Scaling principles and fundamental limits, CMOS inverter scaling, propagation delays, Stick diagram, Layout diagrams.

PART – A

CO Mapping : C312.1

Q.No	Questions	BT Level	Competence	PO
1	What is CMOS technology?	BTL-1	Remembering	PO1
2	What are the advantages of CMOS over NMOS technology?	BTL-2	Understanding	PO1,PO2
3	What is mean by Body effect and body bias effect?	BTL-1	Remembering	PO1
4	What is mean by NMOS transistor?	BTL-1	Remembering	PO1
5	What is mean by process parameter?	BTL-1	Remembering	PO1
6	Write the Electrical properties of CMOS circuits and device modeling?	BTL-2	Understanding	PO1,PO2, PO3,PO4
7	What are the advantages of CMOS technology?	BTL-2	Understanding	PO1,PO2
8	What are the disadvantages of CMOS technology?	BTL-2	Understanding	PO1,PO2
9	What is Design rule?	BTL-1	Remembering	PO1,PO2
10	What is stick diagram?	BTL-1	Remembering	PO1
11	What is micron design rule?	BTL-1	Remembering	PO1,PO2
12	What is Lambda design rule?	BTL-1	Remembering	PO1,PO2
13	What is DRC?	BTL-1	Remembering	PO1
14	Mention MOS transistor characteristics?	BTL-2	Understanding	PO1
15	Compare enhancement and depletion mode devices.	BTL-5	Evaluating	PO1,PO2, PO3,PO4
16	What is threshold voltage?	BTL-1	Remembering	PO1
17	What is noise margin?	BTL-1	Remembering	PO1
18	Compare NMOS and PMOS.	BTL-5	Evaluating	PO1,PO2, PO3,PO4
19	What is Impact Ionization?	BTL-1	Remembering	PO1
20	Difference between Lambda rules and micron rules ?	BTL-4	Analyzing	PO1,PO2
21	What is Moore's Law?	BTL-1	Remembering	PO1
22	What are the steps involved in IC fabrication?	BTL-2	Understanding	PO1,PO2
23	Write down different IC fabrication process?	BTL-2	Understanding	PO1,PO2, PO3,PO4
24	Mention MOS transistor characteristics?	BTL-2	Understanding	PO1
25	What is the need of demarcation line?	BTL-1	Remembering	PO1

26	What are the two types of oxidation methods?	**BTL-2**	**Understanding**	**PO1,PO2**
27	What is Diffusion?	**BTL-1**	**Remembering**	**PO1**
28	What is meant by Epitaxy?	**BTL-1**	**Remembering**	**PO1**
29	What are the materials used for masking?	**BTL-2**	**Understanding**	**PO1,PO2**
30	What is meant channel length modulation in NMOS transistor?	**BTL-1**	**Remembering**	**PO1**
	PART – B			
1	Explain about NMOS ,PMOS transistors steps involved in n-well fabrication process? (AU NOV/DEC– 16)	**BTL-2**	**Understanding**	**PO1,PO2**
2	Define the Process parameters for MOS and CMOS?	**BTL-2**	**Understanding**	**PO1,PO2**
3	Write the Electrical properties of CMOS circuits and device modeling? (AU NOV/DEC– 17,APRIL/MAY – 17) (AU APRIL/MAY – 16)	**BTL-2**	**Understanding**	**PO1,PO2, PO3,PO4**
4	Basic principles Scaling and fundamental limits? (AU NOV/DEC– 17) (AU APRIL/MAY – 17) (AU APRIL/MAY – 16)	**BTL-1**	**Remembering**	**PO1,PO2**
5	Write the CMOS inverter scaling, propagation delays?	**BTL-2**	**Understanding**	**PO1,PO2, PO3,PO4**
6	Draw the basic gates Stick diagram, Layout diagrams?(AU NOV/DEC– 17,APRIL/MAY – 17) (AU NOV/DEC– 16)	**BTL-4**	**Analyzing**	**PO1,PO2**

UNIT II COMBINATIONAL LOGIC CIRCUITS

Examples of Combinational Logic Design, Elmore's constant, Pass transistor Logic, Transmission gates, static and dynamic CMOS design, Power dissipation – Low power design principles.

PART – A

CO Mapping : C312.2

Q.No	Questions	BT Level	Competence	PO
1	Define Static CMOS Design?	**BTL-1**	**Remembering**	**PO1,PO2,PO3**
2	Draw Complementary logic gate as a combination of a PUN (pull-up network) and a PDN (pull-down network).	**BTL-4**	**Analyzing**	**PO1,PO2**
3	Define Propagation Delay of Complementary CMOS Gates? (AU APRIL/MAY – 17)	**BTL-1**	**Remembering**	**PO1,PO2,PO3**
4	Define Transistor Sizing?	**BTL-1**	**Remembering**	**PO1,PO2,PO3**
5	Define Power Consumption in CMOS Logic Gates?	**BTL-1**	**Remembering**	**PO1,PO2,PO3**
6	Design Techniques to Reduce Switching Activity?	**BTL-1**	**Remembering**	**PO1,PO2,PO3**
7	Define Logic Restructuring?	**BTL-1**	**Remembering**	**PO1,PO2,PO3**
8	What are ratioed circuits?	**BTL-2**	**Understanding**	**PO1,PO2**
9	What is CPL?	**BTL-1**	**Remembering**	**PO1,PO2**
10	What are the advantages of pseudo-nMOS logic?	**BTL-2**	**Understanding**	**PO1,PO2**
11	What are the disadvantages of pseudo-nMOS logic	**BTL-2**	**Understanding**	**PO1,PO2**
12	What is pass transistor?	**BTL-1**	**Remembering**	**PO1,PO2**
13	List the advantages of pass transistor.	**BTL-1**	**Remembering**	**PO1,PO2**

14	Define threshold drop.	BTL-1	Remembering	PO1,PO2,PO3
15	What is history effect?	BTL-1	Remembering	PO1,PO2
16	Define Differential Pass Transistor Logic?	BTL-1	Remembering	PO1,PO2,PO3
17	Define Dynamic CMOS Design?	BTL-1	Remembering	PO1,PO2,PO3
18	Define Issues in Dynamic Design?	BTL-1	Remembering	PO1,PO2,PO3
19	Define Charge Leakage?	BTL-1	Remembering	PO1,PO2,PO3
20	Define Domino Logic?	BTL-1	Remembering	PO1,PO2,PO3
21	Draw Simple dual rail (differential) Domino logic gate? (AU NOV/DEC– 17)	BTL-4	Analyzing	PO1,PO2
22	Define Noise margin?	BTL-1	Remembering	PO1,PO2,PO3
23	What is transmission Gate? (AU NOV/DEC– 17)	BTL-1	Remembering	PO1,PO2
24	Why don't we use just one nMOS or pMOS transistor as a transmission gate?	BTL-4	Analyzing	PO1,PO2
25	Write the applications of transmission gate? (AU APRIL/MAY – 17)	BTL-2	Understanding	PO1,PO2, PO3,PO4
26	What is tristate inverter?	BTL-1	Remembering	PO1,PO2
27	Define pseudo-nMOS logic?	BTL-1	Remembering	PO1,PO2,PO3
28	What is MTCMOS?	BTL-1	Remembering	PO1,PO2
29	What are the two categories of SOI devices?	BTL-2	Understanding	PO1,PO2
30	What is fully depleted SOI?	BTL-1	Remembering	PO1,PO2
31	Define Elmore Constant? (AU APRIL/MAY – 17) (AU NOV/DEC– 17) (AU APRIL/MAY – 16)	BTL-1	Remembering	PO1,PO2,PO3
32	Define floating body?	BTL-1	Remembering	PO1,PO2,PO3
	PART – B			
1	Explain the Examples of Combinational Logic Design?	BTL-2	Understanding	PO1,PO2
2	Explain the Elmore's constant & Pass transistor Logic? (AU NOV/DEC– 17)	BTL-2	Understanding	PO1,PO2
3	Define Transmission gates? (AU NOV/DEC– 17) (AU APRIL/MAY – 17) (AU APRIL/MAY – 16)	BTL-1	Remembering	PO1,PO2,PO3
4	Explain the static CMOS design? (AU NOV/DEC– 17) (AU APRIL/MAY – 16)	BTL-2	Understanding	PO1,PO2
5	Explain the dynamic CMOS design? (AU APRIL/MAY – 17) (AU NOV/DEC– 16)	BTL-2	Understanding	PO1,PO2
6	Explain the Power dissipation? (AU NOV/DEC– 17) (AU APRIL/MAY – 17) (AU NOV/DEC– 16) (AU APRIL/MAY – 16)	BTL-2	Understanding	PO1,PO2
7	Define the Low power design principles? (AU NOV/DEC– 17)	BTL-1	Remembering	PO1,PO2,PO3

UNIT III SEQUENTIAL LOGIC CIRCUITS

Static and Dynamic Latches and Registers, Timing issues, pipelines, clock strategies, Memory architecture and

memory control circuits, Low power memory circuits, Synchronous and Asynchronous design				
PART – A				
CO Mapping : C312.3				
Q.No	**Questions**	**BT Level**	**Competence**	**PO**
1	what is mean by Bistability Principle?	BTL-1	Remembering	PO1,PO2
2	Draw the diagram of CMOS clocked SR flip-flop? (AU APRIL/MAY – 16)	BTL-4	Analyzing	PO1,PO2
3	Define the Multiplexer-Based Latches?	BTL-1	Remembering	PO1,PO2,PO3
4	Define the Negative and positive latches based on multiplexers?	BTL-1	Remembering	PO1,PO2,PO3
5	Define the Master-Slave Edge-Triggered Register? (AU APRIL/MAY – 16)	BTL-1	Remembering	PO1,PO2,PO3
6	Define clock jitter? (AU NOV/DEC– 17)	BTL-1	Remembering	PO1,PO2,PO3
7	Define the Low-Voltage Static Latches?	BTL-1	Remembering	PO1,PO2,PO3
8	What is mean Dynamic Latches and Registers?	BTL-1	Remembering	PO1,PO2
9	Define The C2MOS Register?	BTL-1	Remembering	PO1,PO2,PO3
10	Define the Sense-Amplifier Based Registers?	BTL-1	Remembering	PO1,PO2,PO3
11	Define the Sense-Amplifier Based Registers?	BTL-1	Remembering	PO1,PO2,PO3
12	Define the Pipelining? (AU APRIL/MAY – 17) (AU NOV/DEC– 16)	BTL-1	Remembering	PO1,PO2,PO3
13	Write The Schmitt Trigger properties?	BTL-2	Understanding	PO1,PO2, PO3,PO4
14	What is the use Monostable Sequential Circuits?	BTL-1	Remembering	PO1,PO2
15	Define the Latches versus Registers?	BTL-1	Remembering	PO1,PO2,PO3
16	List the methods of sequencing static circuits.	BTL-1	Remembering	PO1,PO2
17	What is called pulsed latch?	BTL-1	Remembering	PO1,PO2
18	Define propagation delay.	BTL-1	Remembering	PO1,PO2,PO3
19	Define contamination delay.	BTL-1	Remembering	PO1,PO2,PO3
20	What are the two types of reset?	BTL-2	Understanding	PO1,PO2
21	What is Differential flip-flops?	BTL-1	Remembering	PO1,PO2

22	What is synchronizer? (AU APRIL/MAY – 17)	BTL-1	Remembering	PO1,PO2
23	What is CMOS Domino logic?	BTL-1	Remembering	PO1,PO2
24	What are the properties of domino logic?	BTL-2	Understanding	PO1,PO2
25	What is Dual-rail domino logic	BTL-1	Remembering	PO1,PO2
26	Define Memory architecture?	BTL-1	Remembering	PO1,PO2,PO3
27	Define dynamic memory?	BTL-1	Remembering	PO1,PO2,PO3
28	What is Differential flip-flops?	BTL-1	Remembering	PO1,PO2
29	Compare and contrast synchronous design and asynchronous design? (AU APRIL/MAY – 17)	BTL-5	Evaluating	PO1,PO2, PO3,PO4
30	Give contamination delay expression	BTL-2	Understanding	PO1,PO2
	PART B			
1	Explain the Static and Dynamic Latches and Registers?TSPC register/NORA-CMOS latches (AU APRIL/MAY – 17) (AU NOV/DEC– 16) (AU APRIL/MAY – 16)	BTL-2	Understanding	PO1,PO2
2	Define timing issues, pipe line and clock strategies? (AU NOV/DEC– 17) (AU APRIL/MAY – 17) (AU APRIL/MAY – 16)	BTL-1	Remembering	PO1,PO2,PO3
3	Explain the Memory architecture?	BTL-2	Understanding	PO1,PO2
4	Briefly explain memory control circuits?	BTL-2	Understanding	PO1,PO2
5	Explain the Low power memory circuits?	BTL-2	Understanding	PO1,PO2
6	What is the mean by Synchronous? Give example. (AU NOV/DEC– 17)	BTL-1	Remembering	PO1,PO2
7	What is the Asynchronous? Give example	BTL-1	Remembering	PO1,PO2

UNIT IV DESIGNING ARITHMETIC BUILDING BLOCKS
Data path circuits, Architectures for ripple carry adders, carry look ahead adders, High speed adders, accumulators, Multipliers, dividers, Barrel shifters, speed and area tradeoff.
PART – A

CO Mapping : C312.4				
Q.No	**Questions**	**BT Level**	**Competence**	PO
1	What is Verilog HDL?	**BTL-1**	**Remembering**	**PO1,PO2**
2	What are the major capabilities of Verilog HDL?	**BTL-2**	**Understanding**	**PO1,PO2**
3	What is Design Methodology?	**BTL-1**	**Remembering**	**PO1,PO2**
4	What is gate level modeling?	**BTL-1**	**Remembering**	**PO1,PO2**
5	What is dataflow modeling?	**BTL-1**	**Remembering**	**PO1,PO2**
6	What is Behavioral level modeling?	**BTL-1**	**Remembering**	**PO1,PO2**
7	What is Test Bench?	**BTL-1**	**Remembering**	**PO1,PO2**
8	What is a Module?	**BTL-1**	**Remembering**	**PO1,PO2**
9	What is the difference between a module and instance?	**BTL-4**	**Analyzing**	**PO1,PO2**
10	Write the syntax of a module	**BTL-2**	**Understanding**	**PO1,PO2, PO3,PO4**
11	What is a Port?	**BTL-1**	**Remembering**	**PO1,PO2**
12	What are the different types of port in verilog HDL?	**BTL-1**	**Remembering**	**PO1,PO2**
13	What is an Identifier?	**BTL-1**	**Remembering**	**PO1,PO2**
14	Give the application of High speed adder? (AU APRIL/MAY – 17)	**BTL-2**	**Understanding**	**PO1,PO2**
15	What is Net data type?	**BTL-1**	**Remembering**	**PO1,PO2**
16	Give some examples for system task in verilog	**BTL-2**	**Understanding**	**PO1,PO2**
17	What is complier directive?	**BTL-1**	**Remembering**	**PO1,PO2**
18	What are the different types operators in verilog HDL?	**BTL-2**	**Understanding**	**PO1,PO2**
19	What is an initial statement?	**BTL-1**	**Remembering**	**PO1,PO2**
20	What is an always statement?	**BTL-1**	**Remembering**	**PO1,PO2**
21	Define the latency? (AU NOV/DEC– 17)	**BTL-1**	**Remembering**	**PO1,PO2,PO3**
22	Draw 4bit ripple carry adder?	**BTL-4**	**Analyzing**	**PO1,PO2**
23	Define Lookahead carry unit?	**BTL-1**	**Remembering**	**PO1,PO2,PO3**
24	Define Carry-save adders?	**BTL-1**	**Remembering**	**PO1,PO2,PO3**
25	Define Carry – Skip Adder	**BTL-1**	**Remembering**	**PO1,PO2,PO3**
26	Draw Lookahead carry unit?	**BTL-4**	**Analyzing**	**PO1,PO2**
27	Define multiplier? (AU NOV/DEC– 16)	**BTL-1**	**Remembering**	**PO1,PO2,PO3**
28	Define barrel shifter? (AU NOV/DEC– 16)	**BTL-1**	**Remembering**	**PO1,PO2,PO3**
29	List out the components of data path(AU APR/MAY– 17)	**BTL-1**	**Remembering**	**PO1,PO2**
30	Define Data path circuits?	**BTL-1**	**Remembering**	**PO1,PO2,PO3**
	PART B			
1	Explain the Data path circuits ? (AU APRIL/MAY – 17)	**BTL-2**	**Understanding**	**PO1,PO2**
2	Explain the Architectures for ripple carry adders? Example. (AU NOV/DEC– 17) (AU NOV/DEC– 16)	**BTL-2**	**Understanding**	**PO1,PO2**
3	Explain the carry look ahead adders & program? (AU APRIL/MAY – 17)	**BTL-2**	**Understanding**	**PO1,PO2**
4	Write the High speed adders? (AU NOV/DEC– 17) (AU APRIL/MAY – 16)	**BTL-2**	**Understanding**	**PO1,PO2, PO3,PO4**

5	Define the accumulators program?	**BTL-1**	**Remembering**	**PO1,PO2,PO3**
6	Define Multipliers and give example? (AU NOV/DEC– 17) (AU APRIL/MAY – 17) (AU NOV/DEC– 16) (AU APRIL/MAY – 16)	**BTL-1**	**Remembering**	**PO1,PO2,PO3**
7	What is mean by dividers and explain?	**BTL-2**	**Understanding**	**PO1,PO2**
8	Explain the Barrel shifters? (AU NOV/DEC– 16)	**BTL-2**	**Understanding**	**PO1,PO2**
9	Explain speed and area tradeoff? (AU APRIL/MAY – 17)	**BTL-2**	**Understanding**	**PO1,PO2**

UNIT V IMPLEMENTATION STRATEGIES

Full custom and Semi custom design, Standard cell design and cell libraries, FPGA building block architectures, FPGA interconnect routing procedures

PART – A

CO Mapping : C312.5

Q.No	Questions	BT Level	Competence	PO
1	What is mean by full custom?	**BTL-1**	**Remembering**	**PO1,PO2**
2	Give the different types of ASIC?	**BTL-2**	**Understanding**	**PO1,PO2**
3	What is the full custom ASIC design? (AU APRIL/MAY – 16)	**BTL-1**	**Remembering**	**PO1,PO2**
4	What is the standard cell-based ASIC design? (AU APRIL/MAY – 17) (AU NOV/DEC– 16)	**BTL-1**	**Remembering**	**PO1,PO2**
5	Differentiate between channeled & channel less gate array	**BTL-4**	**Analyzing**	**PO1,PO2**
6	What is a FPGA?	**BTL-1**	**Remembering**	**PO1,PO2**
7	What are the different methods of programming of PALs?	**BTL-2**	**Understanding**	**PO1,PO2**
8	What are the different levels of design abstraction at physical design?	**BTL-2**	**Understanding**	**PO1,PO2**
9	What is an anti fuse? (AU NOV/DEC– 17)	**BTL-1**	**Remembering**	**PO1,PO2**
10	What are Programmable Interconnects? Macros	**BTL-2**	**Understanding**	**PO1,PO2**
11	Give the steps in ASIC design flow.	**BTL-2**	**Understanding**	**PO1,PO2**
12	Give the XILINX Configurable Logic Block? (AU APRIL/MAY – 17)	**BTL-2**	**Understanding**	**PO1,PO2**
13	Give the XILINX FPGA architecture?	**BTL-2**	**Understanding**	**PO1,PO2**
14	Define standard cell based IC vs custom design IC?	**BTL-1**	**Remembering**	**PO1,PO2,PO3**
15	Define Standard cells design flow?	**BTL-1**	**Remembering**	**PO1,PO2,PO3**
16	Draw Island-Style FPGA?	**BTL-4**	**Analyzing**	**PO1,PO2**
17	How Logic blocks of an FPGA can be implemented?	**BTL-4**	**Analyzing**	**PO1,PO2,PO3**
18	Define SSI, MSI, LSI and VLSI.	**BTL-1**	**Remembering**	**PO1,PO2,PO3**
19	What are the different tools available in a typical CAD tool set.	**BTL-2**	**Understanding**	**PO1,PO2**

20	Types of IC Fabrication Technologies?			
21	What is DFT?	**BTL-1**	**Remembering**	**PO1,PO2**
22	What is Built-in Self-Test?	**BTL-1**	**Remembering**	**PO1,PO2**
23	What are the types of testing carry out in Built-in Self-Test?	**BTL-2**	**Understanding**	**PO1,PO2**
24	What is LFSR?	**BTL-1**	**Remembering**	**PO1,PO2**
25	What is Pseudo-random testing?	**BTL-1**	**Remembering**	**PO1,PO2**
26	Define Design for Testability?	**BTL-1**	**Remembering**	**PO1,PO2,PO3**
27	Define Scan Design Techniques?	**BTL-1**	**Remembering**	**PO1,PO2,PO3**
28	Define Scan Design Rules?	**BTL-1**	**Remembering**	**PO1,PO2,PO3**
29	What is Boundary scan testing?	**BTL-1**	**Remembering**	**PO1,PO2**
30	What is Testers?	**BTL-1**	**Remembering**	**PO1,PO2**
31	What are test fixtures?	**BTL-1**	**Remembering**	**PO1,PO2**
32	What is shmooing?	**BTL-1**	**Remembering**	**PO1,PO2**
33	What is ULSI? (AU NOV/DEC– 17)	**BTL-1**	**Remembering**	**PO1,PO2**
PART B				
1	Explain the Full custom and semi custom design? (AU NOV/DEC– 17) (AU APRIL/MAY – 17) (AU APRIL/MAY – 16)	**BTL-2**	**Understanding**	**PO1,PO2**
2	Explain the Semi custom design? (AU NOV/DEC– 17) (AU NOV/DEC– 16) (AU APRIL/MAY – 16)	**BTL-2**	**Understanding**	**PO1,PO2**
3	Explain the Standard cell design and cell libraries?	**BTL-2**	**Understanding**	**PO1,PO2**
4	Explain the FPGA building block architectures? (AU NOV/DEC– 17) (AU APRIL/MAY – 17) (AU NOV/DEC– 16)	**BTL-2**	**Understanding**	**PO1,PO2**
5	Explain the FPGA interconnect routing procedures? (AU NOV/DEC– 17) (AU APRIL/MAY – 17) (AU APRIL/MAY – 16)	**BTL-2**	**Understanding**	**PO1,PO2**

COURSE DELIVERY PLAN-THEORY

Faculty Name :Balachandran.G	**Programme/Branch:B.E/ECE**
Academic Year:2017-2018	**Year/Semester/Batch:III/VI/2015-2019**
Subject Code/Subject Name: EC6601/VLSI Design	**Regulation:2013**

A. Details of the relevant POs & PSOs supported by the course	
PO1	**Engineering Knowledge:** Apply the knowledge of mathematics, science, engineering fundamentals, and electronics engineering specialization to the solution of complex engineering problems.
PO2	**Problem analysis:** Identify, formulate, review research literature, and analyze complex engineering problems reaching substantiated conclusions using first principles of mathematics, natural sciences, and engineering sciences.
PO3	**Design/development of solutions:** Design solutions for complex engineering problems and design system components or processes that meet the specified needs with appropriate consideration for the public health and safety, and the cultural, societal, and environmental considerations.
PO4	**Conduct investigations of complex problems:** Use research-based knowledge and research methods including design of experiments, analysis and interpretation of data, and synthesis of the information to provide valid conclusions.
PO5	**Modern tool usage:** Create, select, and apply appropriate techniques, resources, and modern engineering and IT tools including prediction and modeling to complex engineering activities with an understanding of the limitations.
PO6	**The engineer and society:** Apply reasoning informed by the contextual knowledge to assess societal, health, safety, legal and cultural issues and the consequent responsibilities relevant to the professional engineering practice.
PO10	**Communication:** Communicate effectively on complex engineering activities with the engineering community and with society at large, such as, being able to comprehend and write effective reports and design documentation, make effective presentations, and give and receive clear instructions.
PSO I	Competence in using modern electronic tools in hardware and software co-design for networking and communication applications.
PSO II	Promote excellence in professional career and higher education by gaining knowledge in the field of Electronics and Communication Engineering
PSO III	Understand social needs and environmental concerns with ethical responsibility to become a successful professional.

B. Details of COs Mapping with PO/PSOs identified for the course

Course Outcome	Course Description	Program Outcomes/Program Specific Outcome														
		PO1	PO2	PO3	PO4	PO5	PO6	PO7	PO8	PO9	PO10	PO11	PO12	PSO1	PSO2	PSO3
C312.1	**Estimate** the characteristics of CMOS circuits	3	3	3	3	3	-	-	-	-	1	1	2	2	3	2
C312.2	**Analyze** the delay models and power dissipation for combinational circuits	3	3	2	3	2	-	-	-	-	1	1	3	3	3	2
C312.3	**Explain** sequential logic circuits and its memory architecture	2	2	2	2	2	-	-	-	-	1	1	3	3	3	2
C312.4	**Classify** different architectures for arithmetic building blocks	2	2	2	2	2	-	-	-	-	1	1	2	3	3	2
C312.5	**Summarize** the techniques of chip design using programmable devices architecture and routing procedures of FPGA	2	3	2	2	3	-	-	-	-	1	1	3	3	3	2

C. Syllabus of the course

UNIT I MOS TRANSISTOR PRINCIPLE 9

NMOS and PMOS transistors, Process parameters for MOS and CMOS, Electrical properties of CMOS circuits and device modeling, Scaling principles and fundamental limits, CMOS inverter scaling, propagation delays, Stick diagram, Layout diagrams

UNIT II COMBINATIONAL LOGIC CIRCUITS 9

Examples of Combinational Logic Design, Elmore's constant, Pass transistor Logic, Transmission gates, static and dynamic CMOS design, Power dissipation – Low power design principles

UNIT III SEQUENTIAL LOGIC CIRCUITS 9

Static and Dynamic Latches and Registers, Timing issues, pipelines, clock strategies, Memory architecture and memory control circuits, Low power memory circuits, Synchronous and Asynchronous design

UNIT IV DESIGNING ARITHMETIC BUILDING BLOCKS 9

Data path circuits, Architectures for ripple carry adders, carry look ahead adders, High speed adders, accumulators, Multipliers, dividers, Barrel shifters, speed and area tradeoff

UNIT V IMPLEMENTATION STRATEGIES 9

Full custom and Semi custom design, Standard cell design and cell libraries, FPGA building block architectures, FPGA interconnect routing procedures

D. Content Beyond Syllabus:

1. Fabrication of nwell CMOS Process

2. System Verilog, :Design Features – Verification Features – Verification & Synthesis Software- Programming

3. Basics of VLSI testing

F. Delivery Resources:

Text Book(s):

T1. Jan Rabaey, Anantha Chandrakasan, B.Nikolic, "Digital Integrated Circuits: A Design Perspective", Second Edition, Prentice Hall of India, 2003.. (Unit I,II,III,IV)

T2. M.J. Smith, "Application Specific Integrated Circuits", Addisson Wesley, 1997 (Unit V)

Reference Book(s):

R1. N.Weste, K.Eshraghian, "Principles of CMOS VLSI Design", Second Edition, Addision Wesley 1993.

R2. R.Jacob Baker, Harry W.LI., David E.Boyee, "CMOS Circuit Design, Layout and Simulation", Prentice Hall of India 2005

R3. A.Pucknell, Kamran Eshraghian, "BASIC VLSI Design", Third Edition, Prentice Hall of India, 2007.

On line learning materials (and Others if any):

1. https://www.youtube.com/watch?v=t2Iba9CG6qE
2. https://www.youtube.com/watch?v=fqiYu6IOtmU

UNIT I MOS TRANSISTOR PRINCIPLE				
Topic to be Covered	Delivery Resources			Delivery Method
	Text Book with Pg.No	Reference Book (if any with Pg.No)	Online Resource (Web Link of the Specific Topic)	
NMOS and PMOS transistors	R3.P.No.6		https://www.youtube.com/watch?v=CpK-3w8zURI	PPT,BB
Process parameters for MOS and CMOS	R3.P.No.14		https://www.youtube.com/watch?v=vbWNy2ZpXLM	BB
Electrical properties of CMOS circuits	R3.P.No.25		https://www.youtube.com/watch?v=DwOB84IZbeU	BB
Device modeling preliminaries	R3.P.No.30		https://www.youtube.com/watch?v=sxuncS0ztis&list=PLa4KQhDlGd7RqJ-9u-AVyDlQe8pe1zOFb	BB
Scaling principles and fundamental limits	R3.P.No.113		https://www.youtube.com/watch?v=PUf64V_Auzw	BB
CMOS inverter scaling	R3.P.No.137		https://www.youtube.com/watch?v=fqiYu6IOtmU&t=20s	BB
propagation delays	R3.P.No.140		https://www.youtube.com/watch?v=m_U0RjcU4jU	BB
Stick diagram	R3.P.No.57		https://www.youtube.com/watch?v=x68G7FUP9k4	PPT,BB
Course Outcome: C312.1: **CO1: understand basic CMOS circuits and properties of CMOS transistors and able to draw stick diagram and layout of CMOS circuits** **CO6: Explain the basic CMOS circuits and the CMOS process technology. Discuss the techniques of chip design using programmable devices. Model the digital system using Hardware Description Language**				
No of hours in the syllabus :9				
No of hours planned :9				
No of hours taught :9				

UNIT II COMBINATIONAL LOGIC CIRCUITS				
Topic to be Covered	Delivery Resources			Delivery Method
	Text Book with Pg.No	Reference Book (if any with Pg.No)	Online Resource (Web Link of the Specific Topic)	
Examples of Combinational Logic Design	T1.P.No.230		https://www.youtube.com/watch?v=s UutDs7FFeA&list=PL3A30A40F0C6932D1&index=3	BB
Elmore's constant	T1.P.No.259			BB
Pass transistor	T1.P.No.262		https://www.youtube.com/watch?v=q8adOpQx7tc	BB

Logic				
Transmission gates	T1.P.No.267		https://www.youtube.com/watch?v=q8adOpQx7tc	PPT,BB
static CMOS design	T1.P.No.232		https://www.youtube.com/watch?v=GNebtGab2V0	BB
Dynamic CMOS design	T1.P.No.272		https://www.youtube.com/watch?v=u-s5PL-qbZA	BB

Course Outcome: C312.2:

CO1: understand basic CMOS circuits and properties of CMOS transistors and able to draw stick diagram and layout of CMOS circuits

CO2: Explain how CMOS realization for combinational logic design and analyze the delay models for combinational circuits and understand power dissipation and low power design principles in CMOS circuits

No of hours in the syllabus :9

No of hours planned :9

No of hours taught :9

UNIT III SEQUENTIAL LOGIC CIRCUITS

Topic to be Covered	Delivery Resources			Delivery Method
	Text Book with Pg.No	Reference Book (if any with Pg.No)	Online Resource (Web Link of the Specific Topic)	
Static Latches and Registers	T1.P.No.300		https://www.youtube.com/watch?v=ibQBb5yEDlQ	BB
Dynamic Latches and Registers	T1.P.No.306		https://www.youtube.com/watch?v=q8adOpQx7tc&t=16s	BB
Timing issues	T1.P.No.325		https://www.youtube.com/watch?v=pEj6LR-C84Y	BB
pipelines	T1.P.No.330		https://www.youtube.com/watch?v=AXgfeV568c8	BB
clock strategies	T1.P.No.236			BB
Memory architecture	T1.P.No.627		https://www.youtube.com/watch?v=u_B_pCkAgak	BB
Memory control circuits	T1.P.No.634		https://www.youtube.com/watch?v=KrqyvpU9Cu0	BB
Low power memory circuits	T1.P.No.701		https://www.youtube.com/watch?v=ruClwamT-R0&list=PLTEh-62_zAfHmJE-pcjgREKiKyPSgjkxj	BB
Synchronous and Asynchronous	T1.P.No.46		https://www.youtube.com/watch?v=LHAbLXfRYXk	BB

design				

Course Outcome: C312.3: CO3: Analyze sequential logic circuits and understand memory architecture and low power memory circuits.
No of hours in the syllabus :9
No of hours planned :9
No of hours taught :9

UNIT IV DESIGNING ARITHMETIC BUILDING BLOCKS				
Topic to be Covered	Delivery Resources			Delivery Method
	Text Book with Pg.No	Reference Book (if any with Pg.No)	Online Resource (Web Link of the Specific Topic)	
Data path circuits	T1.P.No.560		https://www.youtube.com/watch?v=ceuXLsuZhLE	BB
Architectures for ripple carry adders	T1.P.No.562		https://www.youtube.com/watch?v=36hCizOk4PA	BB
carry look ahead adders	T1.P.No.578		https://www.youtube.com/watch?v=36hCizOk4PA	BB
High speed adders	T1.P.No.564		https://www.youtube.com/watch?v=TZ7IkOeTnOM	BB
Accumulators	R3.P.No.236		https://www.youtube.com/watch?v=gruZTqln1cY	BB
Multipliers	T1.P.No.586		https://www.youtube.com/watch?v=5-PI4T25OXI	BB
Course Outcome: C312.4: CO4: Able to understand different architectures for adders and analyze the speed and area trade off and also understand accumulators, multipliers, dividers and barrel shifters				
No of hours in the syllabus :9				
No of hours planned :9				
No of hours taught :9				

UNIT V IMPLEMENTATION STRATEGIES				
Topic to be Covered	Delivery Resources			Delivery Method
	Text Book with Pg.No	Reference Book (if any with Pg.No)	Online Resource (Web Link of the Specific Topic)	
Semi custom design	T2.P.No.19		https://www.youtube.com/watch?v=LhMpVoTA4ME	BB
Full custom design	T2.P.No.20		https://www.youtube.com/watch?v=LhMpVoTA4ME	BB
Standard cell design	T2.P.No.21			BB
cell libraries	T2.P.No.25			BB

FPGA building block architectures	T2.P.No.30		https://www.youtube.com/watch?v=gUsHwi4M4xE	BB
FPGA interconnect routing procedures machine communication	T2.P.No.184		https://www.youtube.com/watch?v=CLUoWkJUnN0	BB
Course Outcome: C312.5: CO5: Able to understand the techniques of chip design using programmable devices and understand the architecture and routing procedures of FPGA CO6: Explain the basic CMOS circuits and the CMOS process technology.Discuss the techniques of chip design using programmable devices.Model the digital system using Hardware Description Language				
No of hours in the syllabus :9				
No of hours planned :9				
No of hours taught :9				